

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f256l-80i-pf

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC32MX5XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

		Pin Nun	nber ⁽¹⁾				
Pin Name	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA	Pin Type	Buffer Type	Description
AC2TX	_	7	E4	B4	0		Alternate CAN2 bus transmit pin
ERXD0	61	41	J7	B23	I	ST	Ethernet Receive Data 0 ⁽²⁾
ERXD1	60	42	L7	A28	I	ST	Ethernet Receive Data 1 ⁽²⁾
ERXD2	59	43	K7	B24	I	ST	Ethernet Receive Data 2 ⁽²⁾
ERXD3	58	44	L8	A29	I	ST	Ethernet Receive Data 3 ⁽²⁾
ERXERR	64	35	J5	B20	I	ST	Ethernet receive error input ⁽²⁾
ERXDV	62	12	F2	A8	I	ST	Ethernet receive data valid ⁽²⁾
ECRSDV	62	12	F2	A8	I	ST	Ethernet carrier sense data valid ⁽²⁾
ERXCLK	63	14	F3	A9	I	ST	Ethernet receive clock ⁽²⁾
EREFCLK	63	14	F3	A9	I	ST	Ethernet reference clock ⁽²⁾
ETXD0	2	88	A6	A60	0	—	Ethernet Transmit Data 0 ⁽²⁾
ETXD1	3	87	B6	B49	0	—	Ethernet Transmit Data 1 ⁽²⁾
ETXD2	43	79	A9	B43	0	—	Ethernet Transmit Data 2 ⁽²⁾
ETXD3	42	80	D8	A54	0	—	Ethernet Transmit Data 3 ⁽²⁾
ETXERR	54	89	E6	B50	0	—	Ethernet transmit error ⁽²⁾
ETXEN	1	83	D7	B45	0	_	Ethernet transmit enable ⁽²⁾
ETXCLK	55	84	C7	A56	I	ST	Ethernet transmit clock ⁽²⁾
ECOL	44	10	E3	A7	I	ST	Ethernet collision detect ⁽²⁾
ECRS	45	11	F4	B6	I	ST	Ethernet carrier sense ⁽²⁾
EMDC	30	71	C11	A46	0	_	Ethernet management data clock ⁽²⁾
EMDIO	49	68	E9	B37	I/O	_	Ethernet management data ⁽²⁾
AERXD0	43	18	G1	A11	I	ST	Alternate Ethernet Receive Data 0 ⁽²⁾
AERXD1	42	19	G2	B10	I	ST	Alternate Ethernet Receive Data 1 ⁽²⁾
AERXD2	—	28	L2	A21	I	ST	Alternate Ethernet Receive Data 2 ⁽²⁾
AERXD3	—	29	K3	B17	I	ST	Alternate Ethernet Receive Data 3 ⁽²⁾
AERXERR	55	1	B2	A2	I	ST	Alternate Ethernet receive error input ⁽²⁾
AERXDV	—	12	F2	A8	I	ST	Alternate Ethernet receive data valid ⁽²⁾
AECRSDV	44	12	F2	A8	Т	ST	Alternate Ethernet carrier sense data valid ⁽²⁾
AERXCLK	_	14	F3	A9	I	ST	Alternate Ethernet receive clock ⁽²⁾
AEREFCLK	45	14	F3	A9	I	ST	Alternate Ethernet reference clock ⁽²⁾
AETXD0	59	47	L9	B26	0		Alternate Ethernet Transmit Data 0 ⁽²⁾
AETXD1	58	48	K9	A31	0		Alternate Ethernet Transmit Data 1 ⁽²⁾
AETXD2	_	44	L8	A29	0		Alternate Ethernet Transmit Data 2 ⁽²⁾
AETXD3	—	43	K7	B24	0		Alternate Ethernet Transmit Data 3 ⁽²⁾
AETXERR	_	35	J5	B20	0		Alternate Ethernet transmit error ⁽²⁾
AETXEN	54	67	E8	A44	0	—	Alternate Ethernet transmit enable ⁽²⁾
AETXCLK	_	66	E11	B36	I	ST	Alternate Ethernet transmit clock ⁽²⁾
AECOL	—	42	L7	A28	I	ST	Alternate Ethernet collision detect ⁽²⁾
Lawand. C		• • • • • • • • • • • • • • • • • • •			٨		D Davies

Legend: CMOS = CMOS compatible input or output ST = Schmitt Trigger input with CMOS levels

Analog = Analog input P = PowerO = Output I = Input

TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the "Device Pin Tables" section for device pin availability.

2: See 25.0 "Ethernet Controller" for more information.

FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX534F064H AND PIC32MX534F064L DEVICES



x = Bit is unknown

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	R/W-x R/W-x		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
31.24				CHEHIT<	:31:24>					
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
23.10				CHEHIT<	:23:16>					
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
10.0				CHEHIT	<15:8>					
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
7.0				CHEHIT	<7:0>					
Legend	:									
R = Rea	dable bit		W = Writable	e bit	U = Unimplemented bit, read as '0'					

REGISTER 9-10: CHEHIT: CACHE HIT STATISTICS REGISTER

bit 31-0 CHEHIT<31:0>: Cache Hit Count bits

- - - - -

-n = Value at POR

Incremented each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

'0' = Bit is cleared

REGISTER 9-11:	CHEMIS: CA	CHE MISS	STATISTICS	S REGISTE	ĸ
					_

'1' = Bit is set

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	R/W-x	R/W-x	R/W-x R/W-x R/W		R/W-x	R/W-x	R/W-x	R/W-x				
31.24				CHEMIS<	<31:24>							
22:46	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
23.10				CHEMIS<	<23:16>							
45.0	R/W-x	R/W-x	R/W-x	R/W-x R/W-x		R/W-x	R/W-x	R/W-x				
15:8	CHEMIS<15:8>											
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
7:0				CHEMIS	6<7:0>							
Legend:	:											
R = Rea	dable bit		W = Writable	e bit	U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared							x = Bit is unl	known				

bit 31-0 CHEMIS<31:0>: Cache Miss Count bits

Incremented each time the processor issues an instruction fetch from a cacheable region that misses the prefetch cache. Non-cacheable accesses do not modify this value.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0						
21.24	U-0	U-0	U-0	U-0 U-0		U-0	U-0	U-0						
31.24		—	—	—	_	—	—							
22.16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1						
23.10	CHAIRQ<7:0> ⁽¹⁾													
15.0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1						
0.61				CHSIRQ	<7:0> ⁽¹⁾									
7.0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0						
7.0	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	_	_	_						

REGISTER 10-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 Unimplemented: Read as '0'

bit 23-16	CHAIRQ<7:0>: Channel Transfer Abort IRQ bits ⁽¹⁾
	11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
	•
	•
	•
	00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag 00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag
bit 15-8	CHSIRQ<7:0>: Channel Transfer Start IRQ bits ⁽¹⁾
	11111111 = Interrupt 255 will initiate a DMA transfer
	•
	•
	•
	00000001 = Interrupt 1 will initiate a DMA transfer 00000000 = Interrupt 0 will initiate a DMA transfer
bit 7	CFORCE: DMA Forced Transfer bit
	 1 = A DMA transfer is forced to begin when this bit is written to a '1' 0 = This bit always reads '0'
bit 6	CABORT: DMA Abort Transfer bit
	 1 = A DMA transfer is aborted when this bit is written to a '1' 0 = This bit always reads '0'
bit 5	PATEN: Channel Pattern Match Abort Enable bit
	1 = Abort transfer and clear CHEN on pattern match0 = Pattern match is disabled
bit 4	SIRQEN: Channel Start IRQ Enable bit
	 1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs 0 = Interrupt number CHSIRQ is ignored and does not start a transfer
bit 3	AIRQEN: Channel Abort IRQ Enable bit
	 1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs 0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer
bit 2-0	Unimplemented: Read as '0'

Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
 - 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
 - 0 = No interrupt is pending
- bit 4 CHDHIF: Channel Destination Half Full Interrupt Flag bit
 - 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
 0 = No interrupt is pending

bit 3 CHBCIF: Channel Block Transfer Complete Interrupt Flag bit

- 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
- 0 = No interrupt is pending

bit 2 CHCCIF: Channel Cell Transfer Complete Interrupt Flag bit

- 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
- 0 = No interrupt is pending
- bit 1 CHTAIF: Channel Transfer Abort Interrupt Flag bit
 - 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
 - 0 = No interrupt is pending

bit 0 CHERIF: Channel Address Error Interrupt Flag bit

- 1 = A channel address error has been detected (either the source or the destination address is invalid)
- 0 = No interrupt is pending

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0 U-0		U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—		—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10		_	_	_		_	_	
15.0	U-0 U-0		U-0	U-0	U-0	U-0	U-0	U-0
15.0	—			—		—	—	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

REGISTER 11-4: U10TGCON: USB OTG CONTROL REGISTER

Legend:

bit 7

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

DPPULUP: D+ Pull-Up Enable bit 1 = D+ data line pull-up resistor is enabled 0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

- 1 = D- data line pull-up resistor is enabled
 0 = D- data line pull-up resistor is disabled
- bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
 - 1 = D+ data line pull-down resistor is enabled
 - 0 = D+ data line pull-down resistor is disabled

bit 4 DMPULDWN: D- Pull-Down Enable bit

- 1 = D- data line pull-down resistor is enabled
- 0 = D- data line pull-down resistor is disabled

bit 3 VBUSON: VBUS Power-on bit

- 1 = VBUS line is powered
- 0 = VBUS line is not powered
- bit 2 **OTGEN:** OTG Functionality Enable bit
 - 1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
 - 0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 VBUSCHG: VBUS Charge Enable bit

- 1 = VBUS line is charged through a pull-up resistor
- 0 = VBUS line is not charged through a resistor

bit 0 VBUSDIS: VBUS Discharge Enable bit

- 1 = VBUS line is discharged through a pull-down resistor
- 0 = VBUS line is not discharged through a resistor

TABLE 12-9: PORTF REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F512H, PIC32MX775F512H, PIC32MX775F512H, PIC32MX795F512H, DEVICES

ess		Ô								Bi	its								\$
Virtual Add (BF88_#	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6140	TDICE	31:16	_	_	-	—	-	_	_	—	-	_	—	—	_	_	_	_	0000
6140	IRIOF	15:0	_	_	_	_	_	_	_	_	_	_	TRISF5	TRISF4	TRISF3	_	TRISF1	TRISF0	003B
6150	DODTE	31:16		_	_		_	-	_			—	_		_				0000
6150	PURIF	15:0		_	_		_		_			—	RF5	RF4	RF3		RF1	RF0	xxxx
6160		31:16	_		—	-	—	-		-	_	—	_	-		-	_	-	0000
0100	LAIF	15:0	-	_	_		_	-	_			—	LATF5	LATF4	LATF3		LATF1	LATF0	xxxx
6170	ODCE	31:16		_	_		_		_			—	_		_				0000
0170	ODCF	15:0	_	_	_	_	_	_	_	_	_	_	ODCF5	ODCF4	ODCF3	_	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 12-10: PORTF REGISTER MAP PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX764F128L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

ess										В	ts								6
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6140	TDICE	31:16	-	_	-	-	-	_	-	-	-	_	-	_	_	-	_	_	0000
6140	IRISE	15:0	-	_	TRISF13	TRISF12	_	-	_	TRISF8	_	_	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	313F
6150	DODTE	31:16	_	_	_	_	_	_	_	_		_	—	_	_	_	_	_	0000
0150	FURIF	15:0	_	—	RF13	RF12	_	_	_	RF8		—	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160		31:16	—	—	—	—	—	—	—	_	_	—	—	—	—	—	—		0000
0100	LAIF	15:0	_	_	LATF13	LATF12	—	_	—	LATF8	-	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCE	31:16		_	—	_	-	_	_			_	—	_	_	—	_	_	0000
0170	ODCF	15:0	_	_	ODCF13	ODCF12	_	_	_	ODCF8	_		ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

15.0 WATCHDOG TIMER (WDT)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 8. "Watchdog Timer and Power-up Timer" in the "PIC32 (DS60001114) Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

This section describes the operation of the WDT and Power-up Timer of the PIC32MX5XX/6XX/7XX.

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle mode



FIGURE 15-1: WATCHDOG TIMER AND POWER-UP TIMER BLOCK DIAGRAM

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	ON ⁽¹⁾	—	SIDL	ADRML	ADRMUX<1:0>		PTWREN	PTRDEN
7.0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7:0	CSF<	1:0> ⁽²⁾	ALP ⁽²⁾	_	CS1P ⁽²⁾	_	WRSP	RDSP

REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾
 - 1 = PMP is enabled
 - 0 = PMP is disabled, no off-chip access performed
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation when device enters Idle mode

bit 12-11 ADRMUX<1:0>: Address/Data Multiplexing Selection bits

- 11 = All 16 bits of address are multiplexed on PMD<15:0> pins
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
- 00 = Address and data appear on separate pins
- bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
 - 1 = PMP module uses TTL input buffers
 - 0 = PMP module uses Schmitt Trigger input buffer
- bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
 - 1 = PMWR/PMENB port is enabled
 - 0 = PMWR/PMENB port is disabled
- bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
 - 1 = PMRD/PMWR port is enabled
 - 0 = PMRD/PMWR port is disabled
- bit 7-6 CSF<1:0>: Chip Select Function bits⁽²⁾
 - 11 = Reserved
 - 10 = PMCS2 and PMCS1 function as Chip Select
 - 01 = PMCS2 functions as Chip Select, PMCS1 functions as address bit 14
 - 00 = PMCS2 and PMCS1 function as address bits 15 and $14^{(2)}$
- bit 5 ALP: Address Latch Polarity bit⁽²⁾
 - 1 = Active-high (PMALL and PMALH)
 - $0 = \text{Active-low} (\overline{\text{PMALL}} \text{ and } \overline{\text{PMALH}})$
- bit 4 Unimplemented: Read as '0'
 - **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - 2: These bits have no effect when their corresponding pins are used as address lines.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0						
31:24	—	—	—	—	—	—	—	_
	U-0	U-0						
23:16	—	—	—	—	—	—	—	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	FORM<2:0>		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
7:0	SSRC<2:0>			CLRASAM	_	ASAM	SAMP ⁽²⁾	DONE ⁽³⁾

REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit⁽¹⁾
 - 1 = ADC module is operating
 - 0 = ADC module is not operating
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode
- bit 12-11 Unimplemented: Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits

- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing the SAMP bit ends sampling and starts conversion
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write a '0' to end sampling and start conversion. If SSRC<2:0> ≠ '000', this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

PIC32MX5XX/6XX/7XX

EGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3									
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
		—	—	_	—		—	_	
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	—	—	—	_	—	—	—		
	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	ADRC	—	—			SAMC<4:0> ⁽¹⁾			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0	
7.0				ADCS<	7:0> ⁽²⁾				

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re-	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15	ADRC: ADC Conversion Clock Source bit
	1 = Clock derived from FRC
	0 = Clock derived from Peripheral Bus Clock (PBCLK)
bit 14-13	Unimplemented: Read as '0'

```
bit 12-8 SAMC<4:0>: Auto-Sample Time bits<sup>(1)</sup>
          11111 = 31 TAD
          00001 = 1 TAD
          00000 = 0 TAD (Not allowed)
         ADCS<7:0>: ADC Conversion Clock Select bits(2)
bit 7-0
          11111111 =TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD
```

```
00000001 =TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD
00000000 =TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD
```

- **Note 1:** This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
 - 2: This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	CH0NB	—	—	—	CH0SB<3:0>			
00.40	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	CH0NA	—	—	—	CH0SA<3:0>			
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—		—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_	_	_		_

REGISTER 23-4: AD1CHS: ADC INPUT SELECT REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	CHONB: Negative Input Select bit for Sample B
	1 = Channel 0 negative input is AN1
	0 = Channel 0 negative input is VREFL
bit 30-28	Unimplemented: Read as '0'
bit 27-24	CH0SB<3:0>: Positive Input Select bits for Sample B
	1111 = Channel 0 positive input is AN15
	•
	•
	•
	0001 = Channel 0 positive input is AN1
	0000 = Channel 0 positive input is AN0
bit 23	CHONA: Negative Input Select bit for Sample A Multiplexer Setting
	1 = Channel 0 negative input is AN1
	0 = Channel 0 negative input is VREFL
bit 22-20	Unimplemented: Read as '0'
bit 19-16	CH0SA<3:0>: Positive Input Select bits for Sample A Multiplexer Setting
	1111 = Channel 0 positive input is AN15
	•
	•
	•
	0001 = Channel 0 positive input is AN1
	0000 = Channel 0 positive input is AN0
bit 15-0	Unimplemented: Read as '0'

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ST:24 FLTEN7 M		MSEL	7<1:0>	FSEL7<4:0>			<u> </u>		
22:46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	FLTEN6	MSEL6<1:0>		FSEL6<4:0>					
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
10.0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>					
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	FLTEN4	MSEL	4<1:0>	FSEL4<4:0>					

REGISTER 24-11: CIFLTCON1: CAN FILTER CONTROL REGISTER 1

Legend:

R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31	FLTEN7: Filter 7 Enable bit
	1 = Filter is enabled0 = Filter is disabled
bit 30-29	MSEL7<1:0>: Filter 7 Mask Select bits
	 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 28-24	FSEL7<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN6: Filter 6 Enable bit
	1 = Filter is enabled0 = Filter is disabled
bit 22-21	MSEL6<1:0>: Filter 6 Mask Select bits
	 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 20-16	FSEL6<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31

uffer 31 11110 = Message matching filter is stored in FIFO buffer 30

•

•

00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 24-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' (n = 0 THROUGH 31)

- bit 6 TXABAT: Message Aborted bit⁽²⁾ 1 = Message was aborted 0 = Message completed successfully bit 5 TXLARB: Message Lost Arbitration bit⁽³⁾ 1 = Message lost arbitration while being sent 0 = Message did not lose arbitration while being sent TXERR: Error Detected During Transmission bit⁽³⁾ bit 4 1 = A bus error occured while the message was being sent 0 = A bus error did not occur while the message was being sent bit 3 **TXREQ:** Message Send Request TXEN = 1: (FIFO configured as a Transmit FIFO) Setting this bit to '1' requests sending a message. The bit will automatically clear when all the messages queued in the FIFO are successfully sent. Clearing the bit to '0' while set ('1') will request a message abort. TXEN = 0: (FIFO configured as a receive FIFO) This bit has no effect. bit 2 RTREN: Auto RTR Enable bit 1 = When a remote transmit is received, TXREQ will be set 0 = When a remote transmit is received, TXREQ will be unaffected bit 1-0 TXPR<1:0>: Message Transmit Priority bits 11 = Highest message priority 10 = High intermediate message priority 01 = Low intermediate message priority 00 = Lowest message priority Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).
 - 2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
 - 3: This bit is reset on any read of this register or when the FIFO is reset.

PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—		—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—		—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RXBUFSZ<6:4>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
		RXBUF	SZ<3:0>		_	_	_	

REGISTER 25-2: ETHCON2: ETHERNET CONTROLLER CONTROL REGISTER 2

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, I	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 Unimplemented: Read as '0'

bit 10-4 RXBUFSZ<6:0>: RX Data Buffer Size for All RX Descriptors (in 16-byte increments) bits
111111 = RX data Buffer size for descriptors is 2032 bytes
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.
.

Note 1: This register is only used for RX operations.
 2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

REGISTER 25-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	_	_	_		—	
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—		_	_		—	
15.9	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	HTEN	MPEN	_	NOTPM		PMMODE	<3:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CRCERREN	CRCOKEN	RUNTERREN	RUNTEN	UCEN	NOTMEEN	MCEN	BCEN

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **HTEN:** Enable Hash Table Filtering bit
 - 1 = Enable Hash Table Filtering
 - 0 = Disable Hash Table Filtering
- bit 14 **MPEN:** Magic Packet[™] Enable bit 1 = Enable Magic Packet Filtering 0 = Disable Magic Packet Filtering
- bit 13 Unimplemented: Read as '0'
- bit 12 **NOTPM:** Pattern Match Inversion bit
 - 1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
 - 0 = The Pattern Match Checksum must match for a successful Pattern Match to occur

This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

- bit 11-8 PMMODE<3:0>: Pattern Match Mode bits
 - 1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)^(1,3)
 - 1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)^(1,2)
 - 0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)⁽¹⁾
 - 0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)⁽¹⁾
 - 0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)⁽¹⁾
 - 0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)⁽¹⁾
 - 0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)⁽¹⁾
 - 0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)⁽¹⁾
 - 0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)⁽¹⁾
 - 0000 = Pattern Match is disabled; pattern match is always unsuccessful

Note 1: XOR = True when either one or the other conditions are true, but not both.

- 2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
- 3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
00.40	R/P	r-1	r-1	R/P	R/P	R/P	R/P	R/P
23:16	FWDTEN	—	—	WDTPS<4:0>				
45.0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
15:8	FCKSM	/<1:0>	FPBDI	IV<1:0> — OSCIOFNC POSCMOD<			OD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	_	FSOSCEN	_	— — FNOSC<2:0>			

REGISTER 29-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 Reserved: Write '1'

bit 23 FWDTEN: Watchdog Timer Enable bit

1 = The WDT is enabled and cannot be disabled by software 0 = The WDT is not enabled; it can be enabled in software

- bit 22-21 Reserved: Write '1'
- bit 20-16 WDTPS<4:0>: Watchdog Timer Postscale Select bits

10100 = 1:1048576 10011 = 1:524288 10010 = 1:262144 10001 = 1:131072 10000 = 1:65536 01111 = 1:32768 01110 = 1:16384 01101 = 1:8192 01100 = 1:4096 01011 = 1:204801010 = 1:1024 01001 = 1:51201000 = 1:256 00111 = 1:128 00110 = 1:6400101 = 1:32 00100 = 1:1600011 = 1:800010 = 1:4 00001 = 1:2 00000 = 1:1

All other combinations not shown result in operation = 10100

bit 15-14 FCKSM<1:0>: Clock Switching and Monitor Selection Configuration bits

1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled

01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled

00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

29.2 On-Chip Voltage Regulator

All PIC32MX5XX/6XX/7XX devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX-5XX/6XX/7XX family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 29-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 32.1 "DC Characteristics"**.

Note: It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

29.2.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

29.2.2 ON-CHIP REGULATOR AND BOR

PIC32MX5XX/6XX/7XX devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset (BOR). This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specified in **Section 32.1 "DC Characteristics"**.

FIGURE 29-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



29.3 **Programming and Diagnostics**

PIC32MX5XX/6XX/7XX devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming[™] (ICSP[™]) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 29-2:

PROGRAMMING, DEBUGGING, AND TRACE PORTS BLOCK DIAGRAM



64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

Revision J (September 2016)

This revision includes typographical and formatting updates throughout the data sheet text. In addition, all SFR Register maps were moved from the Memory chapter to their respective peripheral chapters.

All other major updates are referenced by their respective section in Table B-7.

TABLE B-7:	MAJOR	SECTION	UPDATES

Section Name	Update Description
"32-bit Microcontrollers (up to 512	Updated Communication Interfaces for LIN support to 2.1.
KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet"	Updated Qualification and Class B Support to AEC-Q100 REVH.
2.0 "Guidelines for Getting Started with 32-bit MCUs"	The Recommended Minimum Connection diagram was updated (see Figure 2-1).
	The Example of $\overline{\text{MCLR}}$ Pin Connections diagram was updated (see Figure 2-2).
	2.11 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations" was added.
4.0 "Memory Organization"	The SFR Memory Map was added (see Table 4-1).
7.0 "Interrupt Controller"	The UART interrupt sources were updated in the Interrupt IRQ, Vector, and Bit location table (see Table 7-1).
8.0 "Oscillator Configuration"	Updated the bit value definitions for the TUN<5:0> bits in the OCSTUN register (see Register 8-2).
15.0 "Watchdog Timer (WDT)"	The content in this chapter was relocated from the Special Features chapter to its own chapter.
18.0 "Serial Peripheral Interface (SPI)"	The register map tables were combined (see Table 18-1).
19.0 "Inter-Integrated Circuit (I ² C)"	The register map tables were combined (see Table 19-1).
	The PMADDR register was updated (see Register 21-3).
21.0 "Parallel Master Port (PMP)"	The bit value definitions for the ADRMUX<1:0> and CSF<1:0> bits in the PMCON register were updated (see Register 21-1).
29.0 "Special Features"	Removed the duplicate bit value definition for '010' in the DEVCFG2 register (see Register 29-3).
	Note 1 was added to the Programming, Debugging, and Trace Ports block diagram (see Figure 29-2).
	The DDPCON register was relocated (see Register 29-6).
	The Device ID, Revision, and Configuration Summary was updated (see Table 29-2).