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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f256l-80v-pt

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## TABLE 9: PIN NAMES FOR 100-PIN USB, ETHERNET, AND CAN DEVICES (CONTINUED)

## **100-PIN TQFP (TOP VIEW)**

PIC32MX764F128L PIC32MX775F256L PIC32MX775F512L PIC32MX795F512L

100

Pin #	Full Pin Name	Pin #	Full Pin Name
71	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	86	VDD
72	SDO1/OC1/INT0/RD0	87	C1RX/ETXD1/PMD11/RF0
73	SOSCI/CN1/RC13	88	C1TX/ETXD0/PMD10/RF1
74	SOSCO/T1CK/CN0/RC14	89	C2TX <sup>(1)</sup> /ETXERR/PMD9/RG1
75	Vss	90	C2RX <sup>(1)</sup> /PMD8/RG0
76	OC2/RD1	91	TRCLK/RA6
77	OC3/RD2	92	TRD3/RA7
78	OC4/RD3	93	PMD0/RE0
79	ETXD2/IC5/PMD12/RD12	94	PMD1/RE1
80	ETXD3/PMD13/CN19/RD13	95	TRD2/RG14
81	OC5/PMWR/CN13/RD4	96	TRD1/RG12
82	PMRD/CN14/RD5	97	TRD0/RG13
83	ETXEN/PMD14/CN15/RD6	98	PMD2/RE2
84	ETXCLK/PMD15/CN16/RD7	99	PMD3/RE3
85	VCAP/VDDCORE	100	PMD4/RE4

Note 1: This pin is not available on PIC32MX764F128L devices.

2: Shaded pins are 5V tolerant.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	_	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—		—	—	
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	
15:8	BMXDKPBA<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
				BMXDK	PBA<7:0>				

### REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

#### Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** DRM Kernel Program Base Address Read-Only bits Value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15.9	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS09	IFS08
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	IFS07	IFS06	IFS05	IFS04	IFS03	IFS02	IFS01	IFS00

#### REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

#### Legend:

= Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

#### bit 31-0 IFS31-IFS00: Interrupt Flag Status bits

- 1 = Interrupt request has occurred
- 0 = Interrupt request has not occurred

**Note:** This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

### REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC09	IEC08
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	IEC07	IEC06	IEC05	IEC04	IEC03	IEC02	IEC01	IEC00

## Legend:

0					
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-0 IEC31-IEC00: Interrupt Enable bits

1 = Interrupt is enabled

0 = Interrupt is disabled

**Note:** This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

## PIC32MX5XX/6XX/7XX

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
15:8	ON <sup>(1)</sup>	—	—	SUSPEND	DMABUSY	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_		_	_	_

#### REGISTER 10-1: DMACON: DMA CONTROLLER CONTROL REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

#### bit 31-16 Unimplemented: Read as '0'

- ON: DMA On bit<sup>(1)</sup> bit 15
  - 1 = DMA module is enabled
  - 0 = DMA module is disabled
- bit 14-13 Unimplemented: Read as '0'
- bit 12 SUSPEND: DMA Suspend bit
  - 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
  - 0 = DMA operates normally
- bit 11 DMABUSY: DMA Module Busy bit
  - 1 = DMA module is active
  - 0 = DMA module is disabled and not actively transferring data
- bit 10-0 Unimplemented: Read as '0'
- Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
15:8	CHBUSY	—	—	_	—	—	—	CHCHNS <sup>(1)</sup>
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN <sup>(2)</sup>	CHAED	CHCHN	CHAEN	—	CHEDET	CHPF	RI<1:0>

## REGISTER 10-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## bit 31-16 Unimplemented: Read as '0'

- bit 15 **CHBUSY:** Channel Busy bit 1 = Channel is active or has been enabled 0 = Channel is inactive or has been disabled
- bit 14-9 **Unimplemented:** Read as '0'
- bit 8 CHCHNS: Chain Channel Selection bit<sup>(1)</sup>
  - 1 Choin to channel lower in natural priority (CH1 will be enabled by C
    - 1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
       0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)
- bit 7 CHEN: Channel Enable bit<sup>(2)</sup>
  - 1 = Channel is enabled
    - 0 =Channel is disabled
- bit 6 CHAED: Channel Allow Events If Disabled bit
  - 1 = Channel start/abort events will be registered, even if the channel is disabled
  - 0 = Channel start/abort events will be ignored if the channel is disabled

#### bit CHCHN: Channel Chain Enable bit

- 1 = Allow channel to be chained
- 0 = Do not allow channel to be chained

#### bit 4 CHAEN: Channel Automatic Enable bit

- 1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
- 0 = Channel is disabled on block transfer complete
- bit 3 Unimplemented: Read as '0'
- bit 2 CHEDET: Channel Event Detected bit
  - 1 = An event has been detected
  - 0 = No events have been detected

#### bit 1-0 CHPRI<1:0>: Channel Priority bits

- 11 = Channel has priority 3 (highest)
- 10 = Channel has priority 2
- 01 = Channel has priority 1
- 00 = Channel has priority 0
- **Note 1:** The chain selection bit takes effect when chaining is enabled (CHCHN = 1).
  - 2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

## TABLE 11-1: USB REGISTER MAP (CONTINUED)

ess			Bits																
Virtual Addr (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5280	LI1ERMI (3)	31:16	_	_	—	—	—	_	—	_	—	—	_	—	_	_	—	—	0000
5200	OTINIE	15:0	—	—	—	—	—	—	—	—				FRML<	7:0>				0000
5290	U1FRMH <sup>(3)</sup>	31:16	—	_	—	—	_	—	—	_	_	—	—	—	_	_	—	—	0000
0200	0	15:0	—	_	_	-	-	_	—	—	_	—	_	—	_		FRMH<2:0>		0000
52A0	U1TOK	31:16	—	_	—	—	_	—	—	_	_	—	_	—	_	—	—	—	0000
02/10	onok	15:0	—	—	—	—	—	_	—	—		PID<	:3:0>			EP	<3:0>		0000
52P0		31:16	—	-	—	—	—	_	—	—	_	—	—	—	_	_	—	—	0000
5260	0130F	15:0	-		-	_	_		_	_				CNT<7	<b>'</b> :0>				0000
5000		31:16			-	-	_		_	_		—	—	—			_	_	0000
5200	UIBDIP2	15:0	-		-	_	_		_	_				BDTPTRF	H<7:0>				0000
5200		31:16		-	—	_	_		_	_	_	—	_	—	-	-	—	—	0000
52D0	UIBDIP3	15:0	_			_	—			_				BDTPTRU	J<7:0>				0000
5250		31:16		-	—	_	_		_	_	_	—	_	—	-	-	—	—	0000
52EU	UTCINFGT	15:0	Ι	_	_	-	-	_	_	_	UTEYE	UOEMON	_	USBSIDL	_	_	_	UASUSPND	0001
5200		31:16	-	_	-	-	_	_	-	_	_	—	_	—	—	_	—	_	0000
5300	UTEPU	15:0	Ι	_	_	-	-	_	_	_	LSPD	RETRYDIS	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5040		31:16	-	_	-	-	-	_	_	_	_	-	_	_	_	_	_	_	0000
5310	UTEPT	15:0	—	_	_	_	_	_	_		—	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	-	_	-	-	-	_	_	_	_	-	_	_	_	_	_	_	0000
5320	UTEP2	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	—	_	_	_	_	_	_		—	—	_	—	_	_	—	—	0000
5330	UTEP3	15:0	Ι	_	_	-	-	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5240		31:16	-	_	-	-	-	_	_	_	_	-	_	_	_	_	_	_	0000
5540	UIEP4	15:0	-	_	-	-	_	_	-	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5250		31:16	Ι	_	_	-	-	_	_	_	_	—	_	—	_	_	_	_	0000
5350	UIEP5	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	_	_	_	_	_	_	_	_	—	_	_	—	_	_	—	_	0000
5360	UIEPo	15:0	-	_	-	-	-	_	_	_	_	-	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5070		31:16	_	_	_	_	_	_	_		_	_	_	—	_	_	_	_	0000
5370	U1EP7	15:0	_		_	_	_		_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	_	_	_	_	_	—	—	_	_	_	_	—	—	—	—	—	0000
5380	U1EP8	15:0	_	_	_	_	_	_	_	_	_		_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
		31:16		_	_	_	_	_	—	—	_	_	_	—	—	_		_	0000
5390	U1EP9	15:0	_	_	_	_	_	—	—	—	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

 5390
 U1EP9

 Legend:
 x =

 Note
 1:
 All n

end: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	_
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	ON <sup>(1,2)</sup>	—	—	—	—	—	—	_
7.0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
7:0	_		S	WDTWINEN	WDTCLR			

## REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Legend:	y = Values set from Configuration bits on POR					
R = Readable bit	W = Writable bit	bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-16 Unimplemented: Read as '0'

bit 0

- bit 15 **ON:** Watchdog Timer Enable bit<sup>(1,2)</sup>
  - 1 = Enables the WDT if it is not enabled by the device configuration 0 = Disable the WDT if it was enabled in software
- bit 14-7 **Unimplemented:** Read as '0'
- bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits On reset, these bits are set to the values of the WDTPS <4:0> Configuration bits.
- bit 1 WDTWINEN: Watchdog Timer Window Enable bit
  - 1 = Enable windowed Watchdog Timer
  - 0 = Disable windowed Watchdog Timer
  - WDTCLR: Watchdog Timer Reset bit
    - 1 = Writing a '1' will clear the WDT
    - 0 = Software cannot force this bit to a '0'
- Note 1: A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
  - 2: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	ON <sup>(1)</sup> —		SIDL	ADRML	JX<1:0>	PMPTTL	PTWREN	PTRDEN
7.0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7:0	CSF<	1:0> <sup>(2)</sup>	ALP <sup>(2)</sup>	_	CS1P <sup>(2)</sup>	_	WRSP	RDSP

## REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Parallel Master Port Enable bit<sup>(1)</sup>
  - 1 = PMP is enabled
  - 0 = PMP is disabled, no off-chip access performed
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
  - 1 = Discontinue module operation when device enters Idle mode
  - 0 = Continue module operation when device enters Idle mode

#### bit 12-11 ADRMUX<1:0>: Address/Data Multiplexing Selection bits

- 11 = All 16 bits of address are multiplexed on PMD<15:0> pins
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
- 00 = Address and data appear on separate pins
- bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
  - 1 = PMP module uses TTL input buffers
  - 0 = PMP module uses Schmitt Trigger input buffer
- bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
  - 1 = PMWR/PMENB port is enabled
  - 0 = PMWR/PMENB port is disabled
- bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
  - 1 = PMRD/PMWR port is enabled
  - 0 = PMRD/PMWR port is disabled
- bit 7-6 CSF<1:0>: Chip Select Function bits<sup>(2)</sup>
  - 11 = Reserved
  - 10 = PMCS2 and PMCS1 function as Chip Select
  - 01 = PMCS2 functions as Chip Select, PMCS1 functions as address bit 14
  - 00 = PMCS2 and PMCS1 function as address bits 15 and  $14^{(2)}$
- bit 5 ALP: Address Latch Polarity bit<sup>(2)</sup>
  - 1 = Active-high (PMALL and PMALH)
  - $0 = \text{Active-low} (\overline{\text{PMALL}} \text{ and } \overline{\text{PMALH}})$
- bit 4 Unimplemented: Read as '0'
  - **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
    - 2: These bits have no effect when their corresponding pins are used as address lines.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
15:8	ON <sup>(1)</sup> —		SIDL	—	—	F	ORM<2:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
		SSRC<2:0>		CLRASAM	_	ASAM	SAMP <sup>(2)</sup>	DONE <sup>(3)</sup>

#### REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit<sup>(1)</sup>
  - 1 = ADC module is operating
  - 0 = ADC module is not operating
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
  - 1 = Discontinue module operation when device enters Idle mode
  - 0 = Continue module operation in Idle mode
- bit 12-11 Unimplemented: Read as '0'

#### bit 10-8 **FORM<2:0>:** Data Output Format bits

- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

#### bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing the SAMP bit ends sampling and starts conversion
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write a '0' to end sampling and start conversion. If SSRC<2:0> ≠ '000', this bit is automatically cleared by hardware to end sampling and start conversion.
  - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

## TABLE 24-2:CAN2 REGISTER SUMMARY FOR PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX775F512L, PIC32MX775F512L, AND PIC32MX795F512L, DEVICES

ess										Bi	ts								
Virtual Addr (RF88 #)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
<u> </u>		31:16	—	_	_	_	ABAT		REQOP<2:0	>	(	OPMOD<2:0	>	CANCAP	—	_	_	_	0480
000	0 C2CON	15:0	ON	_	SIDLE	_	CANBUSY	_	—	_	—	_	—		I	DNCNT<4:0	>		0000
C01	COCEG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	S	SEG2PH<2:0	)>	0000
001	02010	15:0	SEG2PHTS	SAM	5	SEG1PH<2:0	)>		PRSEG<2:0	>	SJW	<1:0>		-	BRP	<5:0>			0000
C02	C2INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
002	02.111	15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	_	-	_	-	—			MODIF	CTMRIF	RBIF	TBIF	0000
C03	0 C2VEC	31:16	—	—	_	—	—	—	—	—	—		_	—	—	—	—	—	0000
		15:0	—	—	_			FILHIT<4:0:	>		-				ICODE<6:0>	>		T	0040
C04	0 C2TREC	31:16		—	—	-		—	—	-	-	—	ТХВО	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0							FIFOIDAF					RERRC	NI<7:0>				0000
C05	0 C2FSTAT	15.0	FIFOIP31	FIFOIP30															0000
		31.16	RXOVE31	RXOVE30	RXOVE29	RXOVF28	RXOVF27	RXOVE26	RXOVE25	RXOVF24	RXOVE23	RXOVF22	RXOVE21	RXOVF20	RXOVF19	RXOVF18	RXOVE17	RXOVE16	0000
C06	0 C2RXOVF	15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
		31:16								CANTS	<15:0>	1				1			0000
C07	D C2TMR	15:0							CA	NTSPRE<15	:0>								0000
000	00001/140	31:16						SID<10:0>							MIDE	_	EID<'	17:16>	xxxx
C08	U C2RXMU	15:0								EID<1	15:0>								xxxx
C04		31:16						SID<10:0>							MIDE	_	EID<'	17:16>	xxxx
CUA	0 CZKAWI	15:0								EID<1	15:0>				-				xxxx
COB	C2RXM2	31:16						SID<10:0>							MIDE	—	EID<'	17:16>	xxxx
005	02104112	15:0								EID<1	15:0>				1				xxxx
C0B	0 C2RXM3	31:16						SID<10:0>							MIDE	—	EID<'	17:16>	xxxx
		15:0				1				EID<1	15:0>			ł					xxxx
COC	0 C2FLTCON0	31:16	FLTEN3	MSEL	3<1:0>			FSEL3<4:0:	>		FLTEN2	MSEL	2<1:0>			FSEL2<4:0>	>		0000
		15:0	FLTEN1	MSEL	1<1:0>			FSEL1<4:0:	>		FLTEN0	MSEL	0<1:0>			FSEL0<4:0>	>		0000
C0D	0 C2FLTCON1	31:16	FLTEN7	MSEL	7<1:0>			FSEL7<4:0:	>		FLTEN6	MSEL	6<1:0>			FSEL6<4:0>	>		0000
	-	15:0	FLTEN5	MSEL	5<1:0>			FSEL5<4:0:	>		FLTEN4	MSEL	4<1:0>			FSEL4<4:0>	>		0000
C0E	0 C2FLTCON2	31:16	FLIEN11	MSEL	11<1:0>			FSEL11<4:0	>		FLIEN10	MSEL	10<1:0>		ŀ	-SEL10<4:0	>		0000
	+	15:0         FLIEN9         MSEL9<1:0>         FSEL9<4:0>         FLIEN8         MSEL8<1:0>         FSEL8<4:0>         0000																	
C0F	0 C2FLTCON3	31:16	FLIEN15	MSEL	10<1:0>			FSEL15<4:0	>		FLIEN14	MSEL	14<1:0>			-SEL14<4:0	>		0000
1		15:0	FLIEN13	MSEL1	13<1:0>	1		FSEL13<4:0	1>		FLIEN12	MSEL	12<1:0>		ł	-SEL12<4:0	>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

## PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31.24	FLTEN31	MSEL3	81<1:0>			FSEL31<4:0>	•			
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	FLTEN30	MSEL3	80<1:0>	FSEL30<4:0>						
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
10.6	FLTEN29	MSEL2	29<1:0>			FSEL29<4:0>	•			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7.0	FLTEN28	MSEL2	28<1:0>	FSEL28<4:0>						

## REGISTER 24-17: CIFLTCON7: CAN FILTER CONTROL REGISTER 7

## Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

h ii 04	ELTENDA: Eller 04 Enchla bit
bit 31	FLIEN31: Flitter 31 Enable bit
	1 = Filter is enabled 0 = Filter is disabled
hit 20.20	MSEL 21-1:0-: Eilter 21 Mask Salaet hits
bit 30-29	11 - Accentance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 28-24	FSEL31<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN30: Filter 30Enable bit
	1 = Filter is enabled
bit 22-21	MSEL30<1:0>: Filter 30Mask Select bits
	11 = Acceptance Mask 3 selected
	01 = Acceptance Mask 2 selected
	00 = Acceptance Mask 0 selected
bit 20-16	FSEL30<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

## REGISTER 25-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 25/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	-	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	-	—	—	—	—
	U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
15:8	—	EXCESS DFR	BPNOBK OFF	NOBK OFF	—	—	LONGPRE	PUREPRE
	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
7:0	AUTO PAD <sup>(1,2)</sup>	VLAN PAD <sup>(1,2)</sup>	PAD ENABLE <sup>(1,3)</sup>	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 Unimplemented: Read as '0'

bit 14 **EXCESSDER:** Excess Defer bit

1 = The MAC will defer to carrier indefinitely as per the Standard

0 = The MAC will abort when the excessive deferral limit is reached

#### bit 13 **BPNOBKOFF:** Backpressure/No Backoff bit

- 1 = The MAC after incidentally causing a collision during backpressure will immediately retransmit without backoff reducing the chance of further collisions and ensuring transmit packets get sent
- 0 = The MAC will not remove the backoff

#### bit 12 NOBKOFF: No Backoff bit

- 1 = Following a collision, the MAC will immediately retransmit rather than using the Binary Exponential Backoff algorithm as specified in the Standard
- 0 = Following a collision, the MAC will use the Binary Exponential Backoff algorithm

#### bit 11-10 Unimplemented: Read as '0'

- bit 9 LONGPRE: Long Preamble Enforcement bit
  - 1 = The MAC only allows receive packets which contain preamble fields less than 12 bytes in length
  - 0 = The MAC allows any length preamble as per the Standard

#### bit 8 **PUREPRE:** Pure Preamble Enforcement bit

- 1 = The MAC will verify the content of the preamble to ensure it contains 0x55 and is error-free. A packet with errors in its preamble is discarded
- 0 = The MAC does not perform any preamble checking
- bit 7 AUTOPAD: Automatic Detect Pad Enable bit<sup>(1,2)</sup>
  - 1 = The MAC will automatically detect the type of frame, either tagged or untagged, by comparing the two octets following the source address with 0x8100 (VLAN Protocol ID) and pad accordingly
  - 0 = The MAC does not perform automatic detection

#### Note 1: Table 25-6 provides a description of the pad function based on the configuration of this register.

- 2: This bit is ignored if the PADENABLE bit is cleared.
- 3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

## REGISTER 29-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

- bit 3 ICESEL: In-Circuit Emulator/Debugger Communication Channel Select bit
  - 1 = PGEC2/PGED2 pair is used
  - 0 = PGEC1/PGED1 pair is used
- bit 2 Reserved: Write '1'
- bit 1-0 DEBUG<1:0>: Background Debugger Enable bits (forced to '11' if code-protect is enabled)
  - 11 = Debugger is disabled
  - 10 = Debugger is enabled
  - 01 = Reserved (same as '11' setting)
  - 00 = Reserved (same as '11' setting)

## 31.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 31.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 31.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 31.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>).

## 31.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

## 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]



Microchip Technology Drawing C04-149C Sheet 1 of 2

## Revision E (July 2010)

Minor corrections were incorporated throughout the document.

## **Revision F (December 2010)**

The revision includes the following global update:

VCAP/VDDCORE has been changed to: VCAP/VCORE

Other major changes are referenced by their respective chapter/section in Table B-4:

## TABLE B-4: SECTION UPDATES

Section Name	Update Description
High-Performance, USB, CAN and	Removed the following Analog Feature: FV tolerant input pins
Ethernet 32-bit Flash Microcontrollers	(digital pins only)
	Updated the term LIN 1.2 support as LIN support for the peripheral feature: Six UART modules with: RS-232, RS-485, and LIN support
1.0 "Device Overview"	Updated the value of 64-pin QFN/TQFP pin number for the following pin names: PMA0, PMA1 and ECRSDV
4.0 "Memory Organization"	The following register map tables were updated:
	• Table 4-2:
	<ul> <li>Changed bits 24/8 to I2C5BIF in IFS1</li> </ul>
	<ul> <li>Changed bits 24/8-24/10 to SRIPL&lt;2:0&gt; in INTSTAT</li> </ul>
	<ul> <li>Changed bits 25/9/-24/8 to U5IS&lt;1:0&gt; in IPC12</li> </ul>
	- Added note 2
	Table 4-3 through Table 4-7:
	<ul> <li>Changed bits 24/8-24/10 to SRIPL&lt;2:0&gt; in INTSTAT</li> </ul>
	<ul> <li>Changed bits 25/9-24/8 to U5IS&lt;1:0&gt; in IPC12</li> </ul>
	• Table 4-3:
	<ul> <li>Changed bits 24/8 to I2C5BIF in IFS1</li> </ul>
	- Added note 2
	• Table 4-4:
	<ul> <li>Changed bits 24/8 to I2C5BIF in IFS1</li> </ul>
	<ul> <li>Changed bits 24/8 to I2C5BIE in IEC1</li> </ul>
	<ul> <li>Added note 2 references</li> </ul>
	• Table 4-5:
	<ul> <li>Changed bits 24/8 to I2C5BIF in IFS1</li> </ul>
	<ul> <li>Changed bits 24/8 to I2C5BIE in IEC1</li> </ul>
	- Added note 2 references
	• Table 4-6:
	<ul> <li>Changed bit 24/8 to I2C5BIF in IFS1</li> </ul>
	<ul> <li>Updated the bit value of bit 24/8 as I2C5BIE for the IEC1 register.</li> </ul>
	- Added note 2
	• Table 4-7:
	<ul> <li>Changed bit 25/9 to I2C5SIF in IFS1</li> </ul>
	- Changed bit 24/8 as I2C5BIF in IFS1
	- Changed bit 25/9 as I2C5SIE in IEC1
	- Changed bit 24/8 as I2C5BIE in IEC1
	- Added note 2 references
	Added note 2 to Table 4-8
	<ul> <li>Updated the All Resets values for the following registers in Table 4-11: I2C3CON, I2C4CON, I2C5CON and I2C1CON.</li> </ul>
	<ul> <li>Updated the All Resets values for the I2C2CON register in Table 4-12</li> </ul>

## TABLE B-4: SECTION UPDATES (CONTINUED)

Section Name	Update Description
7.0 "Interrupt Controller"	<ul> <li>Updated the following Interrupt Sources in Table 7-1:</li> </ul>
	- Changed IC2AM – I2C4 Master Event to: IC4M – I2C4 Master Event
	<ul> <li>Changed IC3AM – I2C5 Master Event to: IC5M – I2C4 Master Event</li> </ul>
	- Changed U1E – UART1A Error to: U1E – UART1 Error
	- Changed U4E – UART1B Error to: U4E – UART4 Error
	- Changed U1RX – UART1A Receiver to: U1RX – UART1 Receiver
	- Changed U4RX – UART1B Receiver to: U4RX – UART4 Receiver
	- Changed U11X – UART1A Transmitter to: U11X – UART1 Transmitter
	- Changed U41X - UARTIB Transmitter to: U41X - UART4 Transmitter
	- Changed U6RX – UART2B End to: U6RX – UART6 Receiver
	Changed U6TX – UART2B Receiver to: U6TX – UART6 Transmitter
	- Changed USE – UART3B Error to: USE – UART5 Error
	- Changed U5RX – UART3B Receiver to: U5RX – UART5 Receiver
	- Changed U5TX – UART3B Transmitter to: U5TX – UART5 Transmitter
1.0 "Oscillator Configuration"	Updated Figure 1-1
1.0 "Output Compare"	Updated Figure 1-1
1.0 "Ethernet Controller"	Added a note on using the Ethernet controller pins (see note above
	Table 1-3)
1.0 "Comparator Voltage Reference	Updated the note in Figure 1-1
(CVREF)"	
1.0 "Special Features"	Updated the bit description for bit 10 in Register 1-2
	Added notes 1 and 2 to Register 1-4
1.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings:
	<ul> <li>Voltage on any 5V tolerant pin with respect to Vss when VDD &lt; 2.3V - 0.3V to +3.6V was updated</li> </ul>
	<ul> <li>Voltage on VBUS with respect to VSS - 0.3V to +5.5V was added</li> </ul>
	Updated the maximum value of DC16 as 2.1 in Table 1-4
	Updated the Typical values for the following parameters: DC20b, DC20c, DC21c, DC22c and DC23c (see Table 1-5)
	Updated Table 1-11:
	<ul> <li>Removed the following DC Characteristics: Programming temperature 0°C ≤ TA ≤ +70°C (25°C recommended)</li> </ul>
	• Updated the Minimum value for the Parameter number D131 as 2.3
	<ul> <li>Removed the Conditions for the following Parameter numbers: D130, D131, D132, D135, D136 and D137</li> </ul>
	Updated the condition for the parameter number D130a and D132a
	Updated the Minimum, Typical and Maximum values for parameter D305 in Table 1-13
	Added note 2 to Table 1-18
	Updated the Minimum and Maximum values for parameter F20b (see Table 1-19)
	Updated the following figures:
	• Figure 1-4
	• Figure 1-9
	• Figure 1-22
	• Figure 1-23
Appendix A: "Migrating from PIC32MX3XX/4XX to PIC32MX5XX/ 6XX/7XX Devices"	Removed the A.3 Pin Assignments sub-section.

## **Revision H (March 2013)**

This revision includes the following global updates:

- Where applicable, control register tables have been added to the document
- All references to VCORE were removed
- All occurrences of XBGA have been updated to: TFBGA

## TABLE B-6: MAJOR SECTION UPDATES

• All occurrences of VUSB have been updated to: VUSB3V3

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other significant changes are referenced by their respective section in Table B-6.

Section Name	Update Description
"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet"	Updated Core features. Added the VTLA to the Packages table. Added Note 5 to the Feature tables (see Table 1, Table 2, and Table 3).
Section 2.0 "Guidelines for Getting Started with 32-bit MCUs"	The Recommended Minimum Connection was updated (see Figure 2-1).
Section 5.0 "Flash Program Memory"	A note regarding Flash page size and row size was added.
Section 8.0 "Oscillator Configuration"	The RP resistor was added and Note 1 was updated in the Oscillator Diagram (see Figure 8-1).
Section 31.0 "Electrical Characteristics"	Added Note 1 to Operating MIPS vs. Voltage (see Table 31-1). Added the VTLA package to Thermal Packaging Characteristics (see Table 31-3). Added Note 2 to DC Temperature and Voltage Specifications (see Table 31-4). Updated Note 2 in the Operating Current DC Characteristics (see Table 31-5). Updated Note 1 in the Idle Current DC Characteristics (see Table 31-6). Updated Note 1 in the Power-Down Current DC Characteristics (see Table 31-7). Updated the I/O Pin Output Specifications (see Table 31-9). Added Note 2 to the BOR Electrical Characteristics (see Table 31-10). Added Note 3 to the Comparator Specifications (see Table 31-13). Parameter D320 (VCORE) was removed (see Table 31-15). Updated the Minimum value for parameter OS50 (see Table 31-18). Parameter SY01 (TPWRT) was removed (see Table 31-22). Note 1 was added and the conditions for parameters ET3, ET4, ET7, and ET9 were updated in the Ethernet Module Specifications (see Table 31-35). Added Note 3 to the 10-bit ADC Conversion Rate Parameter (see Table 31-37). Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 31-38). The following figures were added: Figure 31-19: "MDIO Sourced by the PIC32 Device" Figure 31-21: "Transmit Signal Timing Relationships at the MII" Figure 31-22: "Receive Signal Timing Relationships at the MII"
Device Characteristics Graphs"	
Section 33.0 "Packaging Information"	Added the 124-lead VTLA package information (see Section 33.1 "Package Marking Information" and Section 33.2 "Package Details").
"Product Identification System"	Added the TL definition for VTLA packages.

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