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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f256lt-80v-pf

TABLE 6: PIN NAMES FOR 64-PIN USB, ETHERNET, AND CAN DEVICES

64-PIN QFN ⁽³⁾ AND TQFP (TOP VIEW)			
PIC32MX764F128H PIC32MX775F256H PIC32MX775F512H PIC32MX795F512H			
		64	1
		QFN ⁽³⁾	TQFP ¹
Pin #	Full Pin Name	Pin #	Full Pin Name
1	ETXEN/PMD5/RE5	33	USBID/RF3
2	ETXD0/PMD6/RE6	34	V _{BUS}
3	ETXD1/PMD7/RE7	35	V _{USB3V3}
4	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	36	D-/RG3
5	SDA4/SDI2/U3RX/PMA4/CN9/RG7	37	D+/RG2
6	SCL4/SDO2/U3TX/PMA3/CN10/RG8	38	V _{DD}
7	MCLR	39	OSC1/CLKI/RC12
8	SS2/U6RX/U3CTS/PMA2/CN11/RG9	40	OSC2/CLKO/RC15
9	V _{SS}	41	V _{SS}
10	V _{DD}	42	RTCC/AERXD1/ETXD3/IC1/INT1/RD8
11	AN5/C1IN+/V _{BUS} ON/CN7/RB5	43	AERXD0/ETXD2/SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9
12	AN4/C1IN-/CN6/RB4	44	ECOL/AECRS _{SDV} /SCL1/IC3/PMCS2/PMA15/INT3/RD10
13	AN3/C2IN+/CN5/RB3	45	ECRS/AEREFCLK/IC4/PMCS1/PMA14/INT4/RD11
14	AN2/C2IN-/CN4/RB2	46	OC1/INT0/RD0
15	PGEC1/AN1/VREF-/CVREF-/CN3/RB1	47	SOSCI/CN1/RC13
16	PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0	48	SOSCO/T1CK/CN0/RC14
17	PGEC2/AN6/OCFA/RB6	49	EMDIO/AEMDIO/SCK3/U4TX/U1RTS/OC2/RD1
18	PGED2/AN7/RB7	50	SDA3/SDI3/U1RX/OC3/RD2
19	AV _{DD}	51	SCL3/SDO3/U1TX/OC4/RD3
20	AV _{SS}	52	OC5/IC5/PMWR/CN13/RD4
21	AN8/C2TX ⁽²⁾ /SS4/U5RX/U2CTS/C1OUT/RB8	53	PMRD/CN14/RD5
22	AN9/C2OUT/PMA7/RB9	54	AETXEN/ETXERR/CN15/RD6
23	TMS/AN10/CVREFOUT/PMA13/RB10	55	ETXCLK/AERXERR/CN16/RD7
24	TDO/AN11/PMA12/RB11	56	V _{CAP}
25	V _{SS}	57	V _{DD}
26	V _{DD}	58	C1RX/AETXD1/ERXD3/RF0
27	TCK/AN12/PMA11/RB12	59	C1TX/AETXD0/ERXD2/RF1
28	TDI/AN13/PMA10/RB13	60	ERXD1/PMD0/RE0
29	AN14/C2RX ⁽²⁾ /SCK4/U5TX/U2RTS/PMALH/PMA1/RB14	61	ERXD0/PMD1/RE1
30	AN15/EMDC/AEMDC/OCFB/PMALL/PMA0/CN12/RB15	62	ERXDV/ECRS _{SDV} /PMD2/RE2
31	AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4	63	ERXCLK/EREFCLKPMD3/RE3
32	AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5	64	ERXERR/PMD4/RE4

- Note**
- 1: Shaded pins are 5V tolerant.
 - 2: This pin is not available on PIC32MX765F128H devices.
 - 3: The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to V_{SS} externally.

PIC32MX5XX/6XX/7XX

TABLE 8: PIN NAMES FOR 100-PIN USB AND ETHERNET DEVICES

100-PIN TQFP (TOP VIEW)			
PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L		100	1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AERXERR/RG15	36	Vss
2	VDD	37	VDD
3	PMD5/RE5	38	TCK/RA1
4	PMD6/RE6	39	SCK4/U5TX/U2RTS/RF13
5	PMD7/RE7	40	SS4/U5RX/U2CTS/RF12
6	T2CK/RC1	41	AN12/ERXD0/AECRS/PMA11/RB12
7	T3CK/RC2	42	AN13/ERXD1/AECOL/PMA10/RB13
8	T4CK/RC3	43	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14
9	T5CK/SDI1/RC4	44	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
10	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6	45	Vss
11	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7	46	VDD
12	ERXDVI/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8	47	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
13	MCLR	48	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
14	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9	49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
15	Vss	50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
16	VDD	51	USBID/RF3
17	TMS/RA0	52	SDA3/SDI3/U1RX/RF2
18	AERXD0/INT1/RE8	53	SCL3/SDO3/U1TX/RF8
19	AERXD1/INT2/RE9	54	VBUS
20	AN5/C1IN+/VBUSN/CN7/RB5	55	VUSB3V3
21	AN4/C1IN-/CN6/RB4	56	D-/RG3
22	AN3/C2IN+/CN5/RB3	57	D+/RG2
23	AN2/C2IN-/CN4/RB2	58	SCL2/RA2
24	PGEC1/AN1/CN3/RB1	59	SDA2/RA3
25	PGED1/AN0/CN2/RB0	60	TDI/RA4
26	PGEC2/AN6/OCFA/RB6	61	TDO/RA5
27	PGED2/AN7/RB7	62	VDD
28	VREF-/CVREF-/AERXD2/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/AERXD3/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	Vss
31	AVss	66	AETXCLK/SCL1/INT3/RA14
32	AN8/C1OUT/RB8	67	AETXEN/SDA1/INT4/RA15
33	AN9/C2OUT/RB9	68	RTCC/EMDIO/AEMDIO/IC1/RD8
34	AN10/CVREFOUT/PMA13/RB10	69	SS1/IC2/RD9
35	AN11/ERXERR/AETXERR/PMA12/RB11	70	SCK1/IC3/PMCS2/PMA15/RD10

Note 1: Shaded pins are 5V tolerant.

TABLE 9: PIN NAMES FOR 100-PIN USB, ETHERNET, AND CAN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MX764F128L
 PIC32MX775F256L
 PIC32MX775F512L
 PIC32MX795F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
71	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	86	VDD
72	SDO1/OC1/INT0/RD0	87	C1RX/ETXD1/PMD11/RF0
73	SOSCI/CN1/RC13	88	C1TX/ETXD0/PMD10/RF1
74	SOSCO/T1CK/CN0/RC14	89	C2TX ⁽¹⁾ /ETXERR/PMD9/RG1
75	VSS	90	C2RX ⁽¹⁾ /PMD8/RG0
76	OC2/RD1	91	TRCLK/RA6
77	OC3/RD2	92	TRD3/RA7
78	OC4/RD3	93	PMD0/RE0
79	ETXD2/IC5/PMD12/RD12	94	PMD1/RE1
80	ETXD3/PMD13/CN19/RD13	95	TRD2/RG14
81	OC5/PMWR/CN13/RD4	96	TRD1/RG12
82	PMRD/CN14/RD5	97	TRD0/RG13
83	ETXEN/PMD14/CN15/RD6	98	PMD2/RE2
84	ETXCLK/PMD15/CN16/RD7	99	PMD3/RE3
85	VCAP/VDDCORE	100	PMD4/RE4

Note 1: This pin is not available on PIC32MX764F128L devices.
 2: Shaded pins are 5V tolerant.

5.1 Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
F400	NVMCON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	—	—	—	—	—	—	NVMOP<3:0>				0000
F410	NVMKEY	31:16	NVMKEY<31:0>															0000
		15:0																0000
F420	NVMADDR ⁽¹⁾	31:16	NVMADDR<31:0>															0000
		15:0																0000
F430	NVMDATA	31:16	NVMDATA<31:0>															0000
		15:0																0000
F440	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>															0000
		15:0																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

PIC32MX5XX/6XX/7XX

NOTES:

REGISTER 11-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit

1 = ID interrupt enabled

0 = ID interrupt disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit

1 = 1 millisecond timer interrupt enabled

0 = 1 millisecond timer interrupt disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit

1 = Line state interrupt enabled

0 = Line state interrupt disabled

bit 4 **ACTVIE:** Bus ACTIVITY Interrupt Enable bit

1 = ACTIVITY interrupt enabled

0 = ACTIVITY interrupt disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit

1 = Session valid interrupt enabled

0 = Session valid interrupt disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit

1 = B-session end interrupt enabled

0 = B-session end interrupt disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit

1 = A-VBUS valid interrupt enabled

0 = A-VBUS valid interrupt disabled

REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit⁽¹⁾

1 = Module is enabled

0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit

1 = Halt in Idle mode

0 = Continue to operate in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)

1 = Capture rising edge first

0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit

1 = 32-bit timer resource capture

0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')

1 = Timer2 is the counter source for capture

0 = Timer3 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits

11 = Interrupt on every fourth capture event

10 = Interrupt on every third capture event

01 = Interrupt on every second capture event

00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)

1 = Input capture overflow is occurred

0 = No input capture overflow is occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)

1 = Input capture buffer is not empty; at least one more capture value can be read

0 = Input capture buffer is empty

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0> ⁽²⁾		ALP ⁽²⁾	—	CS1P ⁽²⁾	—	WRSP	RDSP

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾

1 = PMP is enabled

0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation when device enters Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits

11 = All 16 bits of address are multiplexed on PMD<15:0> pins

10 = All 16 bits of address are multiplexed on PMD<7:0> pins

01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>

00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit

1 = PMP module uses TTL input buffers

0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit

1 = PMWR/PMENB port is enabled

0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit

1 = PMRD/PMWR port is enabled

0 = PMRD/PMWR port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits⁽²⁾

11 = Reserved

10 = PMCS2 and PMCS1 function as Chip Select

01 = PMCS2 functions as Chip Select, PMCS1 functions as address bit 14

00 = PMCS2 and PMCS1 function as address bits 15 and 14⁽²⁾

bit 5 **ALP:** Address Latch Polarity bit⁽²⁾

1 = Active-high (PMALL and PMALH)

0 = Active-low (PMALL and PMALH)

bit 4 **Unimplemented:** Read as '0'

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

24.1 Control Registers

TABLE 24-1: CAN1 REGISTER SUMMARY FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B000	C1CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
B010	C1CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>					0000	
B020	C1INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
B030	C1VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>				—	ICODE<6:0>						0040		
B040	C1TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
B050	C1FSTAT	31:16	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
B060	C1RXOVF	31:16	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
B070	C1TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
B080	C1RXM0	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
B090	C1RXM1	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
B0A0	C1RXM2	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
B0B0	C1RXM3	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
B0C0	C1FLTCON0	31:16	FLTEN3	MSEL3<1:0>			FSEL3<4:0>				FLTEN2	MSEL2<1:0>			FSEL2<4:0>				0000
		15:0	FLTEN1	MSEL1<1:0>			FSEL1<4:0>				FLTEN0	MSEL0<1:0>			FSEL0<4:0>				0000
B0D0	C1FLTCON1	31:16	FLTEN7	MSEL7<1:0>			FSEL7<4:0>				FLTEN6	MSEL6<1:0>			FSEL6<4:0>				0000
		15:0	FLTEN5	MSEL5<1:0>			FSEL5<4:0>				FLTEN4	MSEL4<1:0>			FSEL4<4:0>				0000
B0E0	C1FLTCON2	31:16	FLTEN11	MSEL11<1:0>			FSEL11<4:0>				FLTEN10	MSEL10<1:0>			FSEL10<4:0>				0000
		15:0	FLTEN9	MSEL9<1:0>			FSEL9<4:0>				FLTEN8	MSEL8<1:0>			FSEL8<4:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)

- bit 13 **SIDLE:** CAN Stop in Idle bit
 1 = CAN Stops operation when system enters Idle mode
 0 = CAN continues operation when system enters Idle mode
- bit 12 **Unimplemented:** Read as '0'
- bit 11 **CANBUSY:** CAN Module is Busy bit
 1 = The CAN module is active
 0 = The CAN module is completely disabled
- bit 10-5 **Unimplemented:** Read as '0'
- bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
 10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
 10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
 •
 •
 •
 00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
 00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 24-11: CifLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)

- bit 15 **FLTEN5**: Filter 17 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 14-13 **MSEL5<1:0>**: Filter 5 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL5<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 .
 .
 .
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN4**: Filter 4 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 6-5 **MSEL4<1:0>**: Filter 4 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL4<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 .
 .
 .
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 25-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	B2BIPKTGP<6:0>						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 25-26: EMAC1IPGR: ETHERNET CONTROLLER MAC NON-BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
	—	NB2BIPKTGP1<6:0>						
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	NB2BIPKTGP2<6:0>						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14-8 **NB2BIPKTGP1<6:0>:** Non-Back-to-Back Interpacket Gap Part 1 bits

This is a programmable field representing the optional carrierSense window referenced in section 4.2.3.2.1 "Deference" of the IEEE 80.23 Specification. If the carrier is detected during the timing of IPGR1, the MAC defers to the carrier. If, however, the carrier comes after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision, thus ensuring fair access to the medium. Its range of values is 0x0 to IPGR2. Its recommend value is 0xC (12d).

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **NB2BIPKTGP2<6:0>:** Non-Back-to-Back Interpacket Gap Part 2 bits

This is a programmable field representing the non-back-to-back Inter-Packet-Gap. Its recommended value is 0x12 (18d), which represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

30.0 INSTRUCTION SET

The PIC32MX5XX/6XX/7XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core Extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to “MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set” at www.imgtec.com for more information.
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TABLE 32-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
DI10	V _{IL}	Input Low Voltage I/O Pins: with TTL Buffer with Schmitt Trigger Buffer	V _{SS}	—	0.15 V _{DD}	V	(Note 4) (Note 4) SMBus disabled (Note 4) SMBus enabled (Note 4)
DI15		MCLR ⁽²⁾	V _{SS}	—	0.2 V _{DD}	V	
DI16		OSC1 (XT mode)	V _{SS}	—	0.2 V _{DD}	V	
DI17		OSC1 (HS mode)	V _{SS}	—	0.2 V _{DD}	V	
DI18		SDAx, SCLx	V _{SS}	—	0.3 V _{DD}	V	
DI19		SDAx, SCLx	V _{SS}	—	0.8	V	
DI20	V _{IH}	Input High Voltage I/O Pins not 5V-tolerant ⁽⁵⁾	0.65 V _{DD}	—	V _{DD}	V	(Note 4,6) (Note 4,6) SMBus disabled (Note 4,6) SMBus enabled, 2.3V ≤ V _{PIN} ≤ 5.5 (Note 4,6)
		I/O Pins 5V-tolerant with PMP ⁽⁵⁾	0.25 V _{DD} + 0.8V	—	5.5	V	
DI28		I/O Pins 5V-tolerant ⁽⁵⁾ SDAx, SCLx	0.65 V _{DD} 0.65 V _{DD}	—	5.5 5.5	V V	
DI29		SDAx, SCLx	2.1	—	5.5	V	
DI30	ICNPU	Change Notification Pull-up Current	—	—	-50	μA	V _{DD} = 3.3V, V _{PIN} = V _{SS} (Note 3,6)
DI31	ICNPD	Change Notification Pull-down Current⁽⁴⁾	—	50	—	μA	V _{DD} = 3.3V, V _{PIN} = V _{DD}

- Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** This parameter is characterized, but not tested in manufacturing.
- 5:** See the “Device Pin Tables” section for the 5V-tolerant pins.
- 6:** The V_{IH} specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic “high” internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.
- 7:** V_{IL} source < (V_{SS} - 0.3). Characterized but not tested.
- 8:** V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- 9:** Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- 10:** Injection currents > |0| can affect the ADC results by approximately 4 to 6 counts (i.e., V_{IH} Source > (V_{DD} + 0.3) or V_{IL} source < (V_{SS} - 0.3)).
- 11:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**, I_{ICL} = (((V_{SS} - 0.3) - V_{IL} source) / R_s). If **Note 8**, I_{ICH} = ((I_{ICH} source - (V_{DD} + 0.3)) / R_S). R_S = Resistance between input source voltage and device pin. If (V_{SS} - 0.3) ≤ V_{SOURCE} ≤ (V_{DD} + 0.3), injection current = 0.

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TABLE 32-13: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D300	V _{IOFF}	Input Offset Voltage	—	±7.5	±25	mV	AVDD = VDD, AVSS = VSS
D301	V _{ICM}	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS (Note 2)
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max V _{ICM} = (VDD - 1)V (Note 2)
D303	T _{RESP}	Response Time	—	150	400	ns	AVDD = VDD, AVSS = VSS (Notes 1, 2)
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	μs	Comparator module is configured before setting the comparator ON bit (Note 2)
D305	V _{REF}	Internal Voltage Reference	0.57	0.6	0.63	V	For devices without BGSEL<1:0>
			1.14	1.2	1.26	V	BGSEL<1:0> = 00
			0.57	0.6	0.63	V	BGSEL<1:0> = 01

- Note 1:** Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.
- 2:** These parameters are characterized but not tested.
- 3:** The Comparator module is functional at VB_{ORMIN} < VDD < VDD_{MIN}, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 32-42: USB OTG ELECTRICAL SPECIFICATIONS

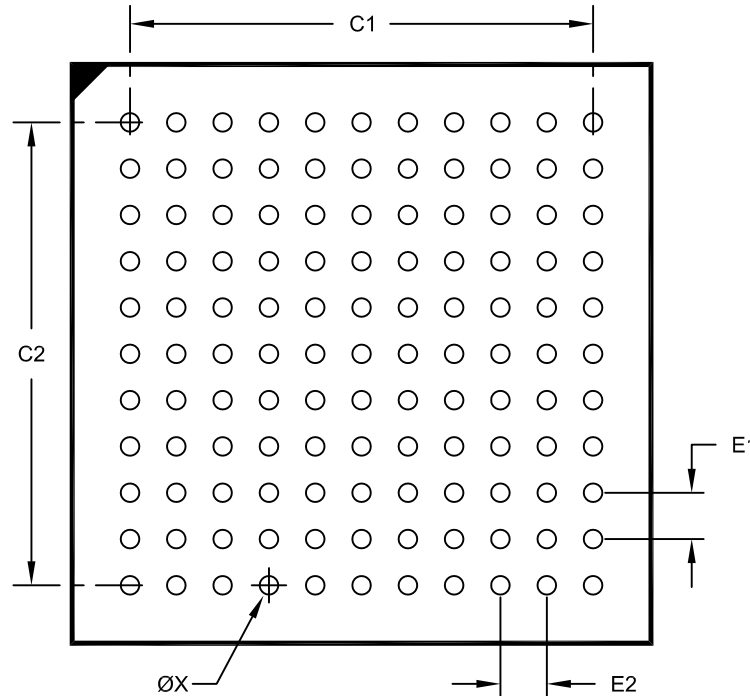
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	—
USB321	Vol	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized, but not tested in manufacturing.

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121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E1	0.80 BSC		
Contact Pitch	E2	0.80 BSC		
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D

TABLE B-4: SECTION UPDATES (CONTINUED)

Section Name	Update Description
4.0 “Memory Organization” (Continued)	- Table 4-13: - Changed register U4RG to U1BRG - Changed register U5RG to U3BRG - Changed register U6RG to U2BRG - Table 4-14: - Updated the All Resets values for the following registers: SPI3STAT, SPI2STAT and SPI4STAT - Table 4-15: Updated the All Resets values for the SPI1STAT register - Table 4-17: Added note 2 - Table 4-19: Added note 2 - Table 4-20: Updated the All Resets values for the CM1CON and CM2CON registers - Table 4-21: - Updated the All Resets values as 0000 for the CVRCON register - Updated note 2 - Table 4-38: Updated the All Resets values for the PMSTAT register - Table 4-40: Updated the All Resets values for the CHECON and CHETAG registers - Table 4-42: Updated the bit value of bit 29/13 as ‘—’ for the DEVCFG3 register - Table 4-44: - Updated the note references in the entire table - Changed existing note 1 to note 4 - Added notes 1, 2 and 3 - Changed bits 23/7 in U1PWRC to UACTPND - Changed register U1DDR to U1ADDR - Changed register U4DTP1 to U1BDTP1 - Changed register U4DTP2 to U1BDTP2 - Changed register U4DTP3 to U1BDTP3 - Table 4-45: - Updated the All Resets values for the C1CON and C1VEC registers - Changed bits 30/14 in C1CON to FRZ - Changed bits 27/11 in C1CON to CANBUSY - Changed bits 22/6-16/0 in C1VEC to ICODE<6:0> - Changed bits 22/6-16/0 in C1TREC to RERRCNT<7:0> - Changed bits 31/15-24/8 in C1TREC to TERRCNT<7:0> - Table 4-46: - Updated the All Resets values for the C2CON and C2VEC registers - Changed bits 30/14 in C1CON to FRZ - Changed bits 27/11 in C1CON to CANBUSY - Changed bits 22/6-16/0 in C1VEC register to ICODE<6:0> - Changed bits 22/6-16/0 in C1TREC register to RERRCNT<7:0> - Changed bits 31/15-24/8 in C1TREC to TERRCNT<7:0>