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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f512ht-80i-mr

PIC32MX5XX/6XX/7XX

TABLE 10: PIN NAMES (CONTINUED) FOR USB AND CAN DEVICES

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX575F256L PIC32MX575F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row. A1			
Pin #	Full Pin Name	Pin #	Full Pin Name
J3	PGED2/AN7/RB7	K8	VDD
J4	AVDD	K9	SCK3/U4TX/U1RTS/CN21/RD15
J5	AN11/PMA12/RB11	K10	USBID/RF3
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2
J7	AN12/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6
J8	No Connect (NC)	L2	VREF-/CVREF-/PMA7/RA9
J9	No Connect (NC)	L3	AVSS
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10
K1	PGEC1/AN1/CN3/RB1	L6	AC1TX/SCK4/U5TX/U2RTS/RF13
K2	PGED1/AN0/CN2/RB0	L7	AN13/PMA10/RB13
K3	VREF+/CVREF+/PMA6/RA10	L8	AN15/OCFB/PMALL/PMA0/CN12/RB15
K4	AN8/C1OUT/RB8	L9	SS3/U4RX/U1CTS/CN20/RD14
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
K6	AC1RX/SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5
K7	AN14/PMALH/PMA1/RB14		

Note 1: Shaded pins are 5V tolerant.

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1	
Pin #	Full Pin Name	Pin #	Full Pin Name
J3	PGED2/AN7/RB7	K8	VDD
J4	AVDD	K9	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
J5	AN11/ERXERR/AETXERR/PMA12/RB11	K10	USBID/RF3
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2
J7	AN12/ERXD0/AECRS/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6
J8	No Connect (NC)	L2	VREF-/CVREF-/AERXD2/PMA7/RA9
J9	No Connect (NC)	L3	AVss
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10
K1	PGEC1/AN1/CN3/RB1	L6	SCK4/U5TX/U2RTS/RF13
K2	PGED1/AN0/CN2/RB0	L7	AN13/ERXD1/AECOL/PMA10/RB13
K3	VREF+/CVREF+/AERXD3/PMA6/RA10	L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
K4	AN8/C1OUT/RB8	L9	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
K6	SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14		

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
AC2TX	—	7	E4	B4	O	—	Alternate CAN2 bus transmit pin
ERXD0	61	41	J7	B23	I	ST	Ethernet Receive Data 0 ⁽²⁾
ERXD1	60	42	L7	A28	I	ST	Ethernet Receive Data 1 ⁽²⁾
ERXD2	59	43	K7	B24	I	ST	Ethernet Receive Data 2 ⁽²⁾
ERXD3	58	44	L8	A29	I	ST	Ethernet Receive Data 3 ⁽²⁾
ERXERR	64	35	J5	B20	I	ST	Ethernet receive error input ⁽²⁾
ERXDV	62	12	F2	A8	I	ST	Ethernet receive data valid ⁽²⁾
ECRSdv	62	12	F2	A8	I	ST	Ethernet carrier sense data valid ⁽²⁾
ERXCLK	63	14	F3	A9	I	ST	Ethernet receive clock ⁽²⁾
EREFCLK	63	14	F3	A9	I	ST	Ethernet reference clock ⁽²⁾
ETXD0	2	88	A6	A60	O	—	Ethernet Transmit Data 0 ⁽²⁾
ETXD1	3	87	B6	B49	O	—	Ethernet Transmit Data 1 ⁽²⁾
ETXD2	43	79	A9	B43	O	—	Ethernet Transmit Data 2 ⁽²⁾
ETXD3	42	80	D8	A54	O	—	Ethernet Transmit Data 3 ⁽²⁾
ETXERR	54	89	E6	B50	O	—	Ethernet transmit error ⁽²⁾
ETXEN	1	83	D7	B45	O	—	Ethernet transmit enable ⁽²⁾
ETXCLK	55	84	C7	A56	I	ST	Ethernet transmit clock ⁽²⁾
ECOL	44	10	E3	A7	I	ST	Ethernet collision detect ⁽²⁾
ECRS	45	11	F4	B6	I	ST	Ethernet carrier sense ⁽²⁾
EMDC	30	71	C11	A46	O	—	Ethernet management data clock ⁽²⁾
EMDIO	49	68	E9	B37	I/O	—	Ethernet management data ⁽²⁾
AERXD0	43	18	G1	A11	I	ST	Alternate Ethernet Receive Data 0 ⁽²⁾
AERXD1	42	19	G2	B10	I	ST	Alternate Ethernet Receive Data 1 ⁽²⁾
AERXD2	—	28	L2	A21	I	ST	Alternate Ethernet Receive Data 2 ⁽²⁾
AERXD3	—	29	K3	B17	I	ST	Alternate Ethernet Receive Data 3 ⁽²⁾
AERXERR	55	1	B2	A2	I	ST	Alternate Ethernet receive error input ⁽²⁾
AERXDV	—	12	F2	A8	I	ST	Alternate Ethernet receive data valid ⁽²⁾
AECRSdv	44	12	F2	A8	I	ST	Alternate Ethernet carrier sense data valid ⁽²⁾
AERXCLK	—	14	F3	A9	I	ST	Alternate Ethernet receive clock ⁽²⁾
AEREFCLK	45	14	F3	A9	I	ST	Alternate Ethernet reference clock ⁽²⁾
AETXD0	59	47	L9	B26	O	—	Alternate Ethernet Transmit Data 0 ⁽²⁾
AETXD1	58	48	K9	A31	O	—	Alternate Ethernet Transmit Data 1 ⁽²⁾
AETXD2	—	44	L8	A29	O	—	Alternate Ethernet Transmit Data 2 ⁽²⁾
AETXD3	—	43	K7	B24	O	—	Alternate Ethernet Transmit Data 3 ⁽²⁾
AETXERR	—	35	J5	B20	O	—	Alternate Ethernet transmit error ⁽²⁾
AETXEN	54	67	E8	A44	O	—	Alternate Ethernet transmit enable ⁽²⁾
AETXCLK	—	66	E11	B36	I	ST	Alternate Ethernet transmit clock ⁽²⁾
AECOL	—	42	L7	A28	I	ST	Alternate Ethernet collision detect ⁽²⁾

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input P = Power
O = Output I = Input

Note 1: Pin numbers are only provided for reference. See the “**Device Pin Tables**” section for device pin availability.

2: See **25.0 “Ethernet Controller”** for more information.

PIC32MX5XX/6XX/7XX

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

Interrupt Source ⁽¹⁾	IRQ Number	Vector Number	Interrupt Bit Location			
			Flag	Enable	Priority	Sub-Priority
Highest Natural Order Priority						
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>
INT0 – External Interrupt 0	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>
IC1 – Input Capture 1	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>
OC1 – Output Compare 1	6	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>
INT1 – External Interrupt 1	7	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>
T2 – Timer2	8	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>
IC2 – Input Capture 2	9	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>
OC2 – Output Compare 2	10	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>
INT2 – External Interrupt 2	11	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>
T3 – Timer3	12	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>
IC3 – Input Capture 3	13	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>
OC3 – Output Compare 3	14	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>
INT3 – External Interrupt 3	15	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>
T4 – Timer4	16	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>
IC4 – Input Capture 4	17	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>
OC4 – Output Compare 4	18	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>
INT4 – External Interrupt 4	19	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>
T5 – Timer5	20	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>
IC5 – Input Capture 5	21	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>
OC5 – Output Compare 5	22	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>
SPI1E – SPI1 Fault	23	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>
SPI1RX – SPI1 Receive Done	24	23	IFS0<24>	IEC0<24>	IPC5<28:26>	IPC5<25:24>
SPI1TX – SPI1 Transfer Done	25	23	IFS0<25>	IEC0<25>	IPC5<28:26>	IPC5<25:24>
U1E – UART1 Error	26	24	IFS0<26>	IEC0<26>	IPC6<4:2>	IPC6<1:0>
SPI3E – SPI3 Fault						
I2C3B – I2C3 Bus Collision Event						
U1RX – UART1 Receiver	27	24	IFS0<27>	IEC0<27>	IPC6<4:2>	IPC6<1:0>
SPI3RX – SPI3 Receive Done						
I2C3S – I2C3 Slave Event						
U1TX – UART1 Transmitter	28	24	IFS0<28>	IEC0<28>	IPC6<4:2>	IPC6<1:0>
SPI3TX – SPI3 Transfer Done						
I2C3M – I2C3 Master Event						
I2C1B – I2C1 Bus Collision Event	29	25	IFS0<29>	IEC0<29>	IPC6<12:10>	IPC6<9:8>
I2C1S – I2C1 Slave Event	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>
I2C1M – I2C1 Master Event	31	25	IFS0<31>	IEC0<31>	IPC6<12:10>	IPC6<9:8>
CN – Input Change Interrupt	32	26	IFS1<0>	IEC1<0>	IPC6<20:18>	IPC6<17:16>

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX5XX USB and CAN Features”**, **TABLE 2: “PIC32MX6XX USB and Ethernet Features”** and **TABLE 3: “PIC32MX7XX USB, Ethernet, and CAN Features”** for the list of available peripherals.

TABLE 7-3: INTERRUPT REGISTER MAP FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H AND PIC32MX695F512H DEVICES

Virtual Address (BF88..#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>				—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
1010	INTSTAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>				—	—	VEC<5:0>					
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
		31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	—	—	USBIF	FCEIF	DMA7IF ⁽²⁾	DMA6IF ⁽²⁾	DMA5IF ⁽²⁾	DMA4IF ⁽²⁾	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
1040	IFS1	15:0	RTCCIF	FSCMIF	—	—	—	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1050	IFS2	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
		31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	—	—	USBIE	FCEIE	DMA7IE ⁽²⁾	DMA6IE ⁽²⁾	DMA5IE ⁽²⁾	DMA4IE ⁽²⁾	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
1070	IEC1	15:0	RTCCIE	FSCMIE	—	—	—	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1080	IEC2	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1090	IPC0	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
10A0	IPC1	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
10B0	IPC2	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
10C0	IPC3	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- 2: These bits are not available on PIC32MX664 devices.
- 3: This register does not have associated CLR, SET, and INV registers.

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
 0 = No interrupt is pending
- bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
 0 = No interrupt is pending
- bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a
 pattern match event occurs
 0 = No interrupt is pending
- bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
 0 = No interrupt is pending
- bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
 0 = No interrupt is pending
- bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
 1 = A channel address error has been detected (either the source or the destination address is invalid)
 0 = No interrupt is pending

TABLE 12-3: PORTC REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 12-4: PORTC REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F00F
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 12-5: PORTD REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0FFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 12-6: PORTD REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LAT15	LAT14	LAT13	LAT12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

REGISTER 18-1: SPIxCON: SPI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 FRMEN	R/W-0 FRMSYNC	R/W-0 FRMPOL	R/W-0 MSEN	R/W-0 FRMSYPW	R/W-0 FRMCNT<2:0>		
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 SPIFE	R/W-0 ENHBUF ⁽²⁾
15:8	R/W-0 ON ⁽¹⁾	U-0 —	R/W-0 SIDL	R/W-0 DISSDO	R/W-0 MODE32	R/W-0 MODE16	R/W-0 SMP	R/W-0 CKE ⁽³⁾
7:0	R/W-0 SSEN	R/W-0 CKP	R/W-0 MSTEN	U-0 —	R/W-0 STXISEL<1:0>	R/W-0 —	R/W-0 SRXISEL<1:0>	R/W-0 —

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (only Framed SPI mode)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)
- bit 29 **FRMPOL:** Frame Sync Polarity bit (only Framed SPI mode)
1 = Frame pulse is active-high
0 = Frame pulse is active-low
- bit 28 **MSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The $\overline{SS}$ pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.
- bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in Framed Sync mode.
111 = Reserved
110 = Reserved
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character
- bit 23-18 **Unimplemented:** Read as '0'
- bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (only Framed SPI mode)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF:** Enhanced Buffer Enable bit⁽²⁾
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit can only be written when the ON bit = 0.

3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

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REGISTER 18-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 15 **ON:** SPI Peripheral On bit⁽¹⁾
1 = SPI Peripheral is enabled
0 = SPI Peripheral is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode
- bit 12 **DISSDO:** Disable SDOx pin bit
1 = SDOx pin is not used by the module (pin is controlled by associated PORT register)
0 = SDOx pin is controlled by the module
- bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits
- | MODE32 | MODE16 | Communication |
|--------|--------|---------------|
| 1 | x | 32-bit |
| 0 | 1 | 16-bit |
| 0 | 0 | 8-bit |
- bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time

Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.
- bit 8 **CKE:** SPI Clock Edge Select bit⁽³⁾
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)
- bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = SSx pin used for Slave mode
0 = SSx pin not used for Slave mode (pin is controlled by port function)
- bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode
- bit 4 **Unimplemented:** Read as '0'
- bit 3-2 **STXISEL<1:0>:** SPI Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPIxSR and transmit operations are complete
- bit 1-0 **SRXISEL<1:0>:** SPI Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit can only be written when the ON bit = 0.
- 3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0> ⁽²⁾		ALP ⁽²⁾	—	CS1P ⁽²⁾	—	WRSP	RDSP

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾

1 = PMP is enabled

0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation when device enters Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits

11 = All 16 bits of address are multiplexed on PMD<15:0> pins

10 = All 16 bits of address are multiplexed on PMD<7:0> pins

01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>

00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit

1 = PMP module uses TTL input buffers

0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit

1 = PMWR/PMENB port is enabled

0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit

1 = PMRD/PMWR port is enabled

0 = PMRD/PMWR port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits⁽²⁾

11 = Reserved

10 = PMCS2 and PMCS1 function as Chip Select

01 = PMCS2 functions as Chip Select, PMCS1 functions as address bit 14

00 = PMCS2 and PMCS1 function as address bits 15 and 14⁽²⁾

bit 5 **ALP:** Address Latch Polarity bit⁽²⁾

1 = Active-high (PMALL and PMALH)

0 = Active-low (PMALL and PMALH)

bit 4 **Unimplemented:** Read as '0'

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

22.1 Control Registers

TABLE 22-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
0200	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										000
		15:0	ON	—	SIDL	—	—	—	—	—	RTSECSEL	RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	000
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	000	
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>					ARPT<7:0>							000
0220	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	xx0	
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0
0240	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	xx0	
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00x
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

REGISTER 23-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NB	—	—	—	CH0SB<3:0>			
23:16	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA	—	—	—	CH0SA<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **CH0NB:** Negative Input Select bit for Sample B

1 = Channel 0 negative input is AN1

0 = Channel 0 negative input is VREFL

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CH0SB<3:0>:** Positive Input Select bits for Sample B

1111 = Channel 0 positive input is AN15

•
•
•

0001 = Channel 0 positive input is AN1

0000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting

1 = Channel 0 negative input is AN1

0 = Channel 0 negative input is VREFL

bit 22-20 **Unimplemented:** Read as '0'

bit 19-16 **CH0SA<3:0>:** Positive Input Select bits for Sample A Multiplexer Setting

1111 = Channel 0 positive input is AN15

•
•
•

0001 = Channel 0 positive input is AN1

0000 = Channel 0 positive input is AN0

bit 15-0 **Unimplemented:** Read as '0'

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REGISTER 25-17: ETHFRMTXOK: ETHERNET CONTROLLER FRAMES TRANSMITTED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMTXOKCNT<15:0>:** Frame Transmitted OK Count bits
Increment counter for frames successfully transmitted.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	B2BIPKTGP<6:0>						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 25-27: EMAC1CLRT: ETHERNET CONTROLLER MAC COLLISION WINDOW/RETRY LIMIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	CWINDOW<5:0>					
7:0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	—	RETX<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13-8 **CWINDOW<5:0>:** Collision Window bits

This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RETX<3:0>:** Retransmission Maximum bits

This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts (attemptLimit) to be 0xF (15d). Its default is '0xF'.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 27-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON ⁽¹⁾	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 VREFSEL ⁽²⁾	R/W-0 BGSEL<1:0> ⁽²⁾	R/W-1
7:0	U-0 —	R/W-0 CVROE	R/W-0 CVRR	R/W-0 CVRSS	R/W-0	R/W-0	R/W-0	R/W-0
CVR<3:0>								

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit⁽¹⁾

Setting or clearing this bit does not affect the other bits in this register.

1 = Module is enabled

0 = Module is disabled and does not consume current

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Voltage Reference Select bit⁽²⁾

1 = CVREF = VREF+

0 = CVREF is generated by the resistor network

bit 9-8 **BGSEL<1:0>:** Band Gap Reference Source bits⁽²⁾

11 = IVREF = VREF+

10 = Reserved

01 = IVREF = 0.6V (nominal, default)

00 = IVREF = 1.2V (nominal)

bit 7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** CVREFOUT Enable bit

1 = Voltage level is output on CVREFOUT pin

0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit

1 = 0 to 0.625 CVRSRC, with CVRSRC/24 step size

0 = 0.25 CVRSRC to 0.719 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit

1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)

0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \leq \text{CVR}<3:0> \leq 15$ bits

When CVRR = 1:

$\text{CVREF} = (\text{CVR}<3:0>/24) \cdot (\text{CVRSRC})$

When CVRR = 0:

$\text{CVREF} = 1/4 \cdot (\text{CVRSRC}) + (\text{CVR}<3:0>/32) \cdot (\text{CVRSRC})$

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: These bits are not available on PIC32MX575/675/775/795 devices. On these devices, the reset value for CVRON is '0000'.

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NOTES:

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TABLE 32-37: 10-BIT ADC CONVERSION RATE PARAMETERS

Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp					
ADC Speed ⁽²⁾	T _{AD} Minimum	Sampling Time Minimum	R _s Maximum	V _{DD}	ADC Channels Configuration
1 Msps to 400 ksps ⁽¹⁾	65 ns	132 ns	500Ω	3.0V to 3.6V	
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	

- Note 1:** External VREF- and VREF+ pins must be used for correct operation.
- 2:** These parameters are characterized, but not tested in manufacturing.
- 3:** The ADC module is functional at $V_{BORMIN} < V_{DD} < 2.5\text{V}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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