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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f512ht-80v-pt

Device Pin Tables

TABLE 4: PIN NAMES FOR 64-PIN USB AND CAN DEVICES

64-PIN QFN ⁽²⁾ AND TQFP (TOP VIEW)			
PIC32MX534F064H PIC32MX564F064H PIC32MX564F128H PIC32MX575F256H PIC32MX575F512H		64	1
		QFN ⁽²⁾	TQFP ¹
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PMD5/RE5	33	USBID/RF3
2	PMD6/RE6	34	VBUS
3	PMD7/RE7	35	VUSB3V3
4	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	36	D-/RG3
5	SDA4/SDI2/U3RX/PMA4/CN9/RG7	37	D+/RG2
6	SCL4/SDO2/U3TX/PMA3/CN10/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	SS2/U6RX/U3CTS/PMA2/CN11/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RTCC/IC1/INT1/RD8
11	AN5/C1IN+/VBUSON/CN7/RB5	43	SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9
12	AN4/C1IN-/CN6/RB4	44	SCL1/IC3/PMCS2/PMA15/INT3/RD10
13	AN3/C2IN+/CN5/RB3	45	IC4/PMCS1/PMA14/INT4/RD11
14	AN2/C2IN-/CN4/RB2	46	OC1/INT0/RD0
15	PGEC1/AN1/VREF-/CVREF-/CN3/RB1	47	SOSCI/CN1/RC13
16	PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0	48	SOSCO/T1CK/CN0/RC14
17	PGEC2/AN6/OCFA/RB6	49	SCK3/U4TX/U1RTS/OC2/RD1
18	PGED2/AN7/RB7	50	SDA3/SDI3/U1RX/OC3/RD2
19	AVDD	51	SCL3/SDO3/U1TX/OC4/RD3
20	AVSS	52	OC5/IC5/PMWR/CN13/RD4
21	AN8/SS4/U5RX/U2CTS/C1OUT/RB8	53	PMRD/CN14/RD5
22	AN9/C2OUT/PMA7/RB9	54	CN15/RD6
23	TMS/AN10/CVREFOUT/PMA13/RB10	55	CN16/RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	C1RX/RF0
27	TCK/AN12/PMA11/RB12	59	C1TX/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14	61	PMD1/RE1
30	AN15/OCFB/PMALL/PMA0/CN12/RB15	62	PMD2/RE2
31	AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4	63	PMD3/RE3
32	AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5	64	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

PIC32MX5XX/6XX/7XX

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1	
Pin #	Full Pin Name	Pin #	Full Pin Name
A1	PMD4/RE4	E2	T4CK/RC3
A2	PMD3/RE3	E3	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6
A3	TRD0/RG13	E4	T3CK/RC2
A4	PMD0/RE0	E5	VDD
A5	PMD8/RG0	E6	ETXERR/PMD9/RG1
A6	ETXD0/PMD10/RF1	E7	VSS
A7	VDD	E8	AETXEN/SDA1/INT4/RA15
A8	VSS	E9	RTCC/EMDIO/AEMDIO/IC1/RD8
A9	ETXD2/IC5/PMD12/RD12	E10	SS1/IC2/RD9
A10	OC3/RD2	E11	AETXCLK/SCL1/INT3/RA14
A11	OC2/RD1	F1	MCLR
B1	No Connect (NC)	F2	ERXDVI/AERXDVI/ECRSDVI/AECRSDVI/SCL4/SDO2/U3TX/PMA3/CN10/RG8
B2	AERXERR/RG15	F3	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9
B3	PMD2/RE2	F4	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7
B4	PMD1/RE1	F5	VSS
B5	TRD3/RA7	F6	No Connect (NC)
B6	ETXD1/PMD11/RF0	F7	No Connect (NC)
B7	VCAP	F8	VDD
B8	PMRD/CN14/RD5	F9	OSC1/CLKI/RC12
B9	OC4/RD3	F10	VSS
B10	VSS	F11	OSC2/CLKO/RC15
B11	SOSCO/T1CK/CN0/RC14	G1	AERXD0/INT1/RE8
C1	PMD6/RE6	G2	AERXD1/INT2/RE9
C2	VDD	G3	TMS/RA0
C3	TRD1/RG12	G4	No Connect (NC)
C4	TRD2/RG14	G5	VDD
C5	TRCLK/RA6	G6	VSS
C6	No Connect (NC)	G7	VSS
C7	ETXCLK/PMD15/CN16/RD7	G8	No Connect (NC)
C8	OC5/PMWR/CN13/RD4	G9	TDO/RA5
C9	VDD	G10	SDA2/RA3
C10	SOSCI/CN1/RC13	G11	TDI/RA4
C11	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	H1	AN5/C1IN+/VBUSON/CN7/RB5
D1	T2CK/RC1	H2	AN4/C1IN-/CN6/RB4
D2	PMD7/RE7	H3	VSS
D3	PMD5/RE5	H4	VDD
D4	VSS	H5	No Connect (NC)
D5	VSS	H6	VDD
D6	No Connect (NC)	H7	No Connect (NC)
D7	ETXEN/PMD14/CN15/RD6	H8	VBUS
D8	ETXD3/PMD13/CN19/RD13	H9	VUSB3V3
D9	SDO1/OC1/INT0/RD0	H10	D+/RG2
D10	No Connect (NC)	H11	SCL2/RA2
D11	SCK1/IC3/PMCS2/PMA15/RD10	J1	AN3/C2IN+/CN5/RB3
E1	T5CK/SDI1/RC4	J2	AN2/C2IN-/CN4/RB2

Note 1: Shaded pins are 5V tolerant.

TABLE 7-4: INTERRUPT REGISTER MAP FOR PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0	
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000	
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000	
10E0	IPC5	31:16	—	—	—	—	—	—	—	—	—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000	
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000	
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000	
		15:0	—	—	I2C1IP<2:0>			I2C1IS<1:0>			—	—	—	U1IP<2:0>			U1IS<1:0>		0000	
														SPI3IP<2:0>			SPI3IS<1:0>			
														I2C3IP<2:0>			I2C3IS<1:0>			
1100	IPC7	31:16	—	—	—	U3IP<2:0>			U3IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000	
						SPI2IP<2:0>			SPI2IS<1:0>											
						I2C4IP<2:0>			I2C4IS<1:0>											
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000	
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000	
		15:0	—	—	—	—	—	—	—	—	—	—	U2IP<2:0>			U2IS<1:0>		0000		
													SPI4IP<2:0>			SPI4IS<1:0>				
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000	
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000	
1130	IPC10	31:16	—	—	—	DMA7IP<2:0> ⁽²⁾			DMA7IS<1:0> ⁽²⁾		—	—	—	DMA6IP<2:0> ⁽²⁾			DMA6IS<1:0> ⁽²⁾		0000	
		15:0	—	—	—	DMA5IP<2:0> ⁽²⁾			DMA5IS<1:0> ⁽²⁾		—	—	—	DMA4IP<2:0> ⁽²⁾			DMA4IS<1:0> ⁽²⁾		0000	
1140	IPC11	31:16	—	—	—	CAN2IP<2:0> ⁽²⁾			CAN2IS<1:0> ⁽²⁾		—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		0000	
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000	
1150	IPC12	31:16	—	—	—	U5IP<2:0>			U5IS<1:0>		—	—	—	U6IP<2:0>			U6IS<1:0>		0000	
		15:0	—	—	—	U4IP<2:0>			U4IS<1:0>		—	—	—	ETHIP<2:0>			ETHIS<1:0>		0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- 2: This bit is unimplemented on PIC32MX764F128H device.
- 3: This register does not have associated CLR, SET, and INV registers.

PIC32MX5XX/6XX/7XX

REGISTER 10-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	RDWR	DMACH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **RDWR:** Read/Write Status bit

1 = Last DMA bus access was a read

0 = Last DMA bus access was a write

bit 2-0 **DMACH<2:0>:** DMA Channel bits

These bits contain the value of the most recent active DMA channel.

REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits

These bits contain the address of the most recent DMA access.

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REGISTER 11-16: U1SOF: USB SOF THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:

01001010 = 64-byte packet

00101010 = 32-byte packet

00011010 = 16-byte packet

00010010 = 8-byte packet

REGISTER 11-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BDTPTRL<15:9>							—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'

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REGISTER 14-1: TXCON: TYPE B TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON ^(1,3)	—	SIDL ⁽⁴⁾	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE ⁽³⁾	TCKPS<2:0> ⁽³⁾			T32 ⁽²⁾	—	TCS ⁽³⁾	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit^(1,3)

1 = Module is enabled

0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit⁽⁴⁾

1 = Discontinue operation when device enters Idle mode

0 = Continue operation when device is in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽³⁾

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits⁽³⁾

111 = 1:256 prescale value

110 = 1:64 prescale value

101 = 1:32 prescale value

100 = 1:16 prescale value

011 = 1:8 prescale value

010 = 1:4 prescale value

001 = 1:2 prescale value

000 = 1:1 prescale value

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSClk cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only available on even numbered timers (Timer2 and Timer4).

3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, and Timer5). All timer functions are set through the even numbered timers.

4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

15.1 Control Registers

TABLE 15-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets ⁽²⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	SWDTPS<4:0>					—	WDTCLR	0000

- Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

REGISTER 23-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	—	CSCNA	—	—
7:0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFS	—	SMPI<3:0>				BUFM	ALTS

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>**: Voltage Reference Configuration bits

Bit Value	VREFH	VREFL
1xx	AVDD	AVss
011	External VREF+ pin	External VREF- pin
010	AVDD	External VREF- pin
001	External VREF+ pin	AVSS
000	AVDD	AVss

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the S&H circuit are connected to VREFL.

0 = Disable Offset Calibration mode

The inputs to the S&H circuit are controlled by AD1CHS or AD1CSSL.

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit

1 = Scan inputs

0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1.

1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7

0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>**: Sample/Convert Sequences Per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence

1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence

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.

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0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence

0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8

0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses Sample A input multiplexer settings for first sample, and then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples

0 = Always use Sample A input multiplexer settings

24.1 Control Registers

TABLE 24-1: CAN1 REGISTER SUMMARY FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name(L)	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
B000	C1CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480	
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000	
B010	C1CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000	
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>						0000	
B020	C1INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000	
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000	
B030	C1VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040	
B040	C1TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000	
		15:0	TERRCNT<7:0>									RERRCNT<7:0>								
B050	C1FSTAT	31:16	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16	0000	
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000	
B060	C1RXOVF	31:16	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000	
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000	
B070	C1TMR	31:16	CANTS<15:0>																0000	
		15:0	CANTSPRE<15:0>															0000		
B080	C1RXM0	31:16	SID<10:0>											—		MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx	
B090	C1RXM1	31:16	SID<10:0>											—		MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx	
B0A0	C1RXM2	31:16	SID<10:0>											—		MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx	
B0B0	C1RXM3	31:16	SID<10:0>											—		MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx	
B0C0	C1FLTCON0	31:16	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				FLTEN2		MSEL2<1:0>		FSEL2<4:0>				0000		
		15:0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				FLTEN0		MSEL0<1:0>		FSEL0<4:0>				0000		
B0D0	C1FLTCON1	31:16	FLTEN7	MSEL7<1:0>		FSEL7<4:0>				FLTEN6		MSEL6<1:0>		FSEL6<4:0>				0000		
		15:0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>				FLTEN4		MSEL4<1:0>		FSEL4<4:0>				0000		
B0E0	C1FLTCON2	31:16	FLTEN11	MSEL11<1:0>		FSEL11<4:0>				FLTEN10		MSEL10<1:0>		FSEL10<4:0>				0000		
		15:0	FLTEN9	MSEL9<1:0>		FSEL9<4:0>				FLTEN8		MSEL8<1:0>		FSEL8<4:0>				0000		

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)

- bit 13 **SIDLE:** CAN Stop in Idle bit
 1 = CAN Stops operation when system enters Idle mode
 0 = CAN continues operation when system enters Idle mode
- bit 12 **Unimplemented:** Read as '0'
- bit 11 **CANBUSY:** CAN Module is Busy bit
 1 = The CAN module is active
 0 = The CAN module is completely disabled
- bit 10-5 **Unimplemented:** Read as '0'
- bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
 10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
 10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
 •
 •
 •
 00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
 00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 24-11: CifLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)

bit 15 **FLTEN5**: Filter 17 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 14-13 **MSEL5<1:0>**: Filter 5 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 12-8 **FSEL5<4:0>**: FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

.

.

.

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4**: Filter 4 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 6-5 **MSEL4<1:0>**: Filter 4 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 4-0 **FSEL4<4:0>**: FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

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.

.

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

25.1 Control Registers

TABLE 25-5: ETHERNET CONTROLLER REGISTER SUMMARY FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX695F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX764F128H, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	ETHCON1	31:16	PTV<15:0>																0000
		15:0	ON	—	SIDL	—	—	—	TXRTS	RXEN	AUTOFC	—	—	MANFC	—	—	—	BUFCDEC	0000
9010	ETHCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RXBUFSZ<6:0>							—	—	—	—	0000
9020	ETHTXST	31:16	TXSTADDR<31:16>																0000
		15:0	TXSTADDR<15:2>													—	—	—	0000
9030	ETHRXST	31:16	RXSTADDR<31:16>																0000
		15:0	RXSTADDR<15:2>													—	—	—	0000
9040	ETHHT0	31:16	HT<31:0>																0000
		15:0																	0000
9050	ETHHT1	31:16	HT<63:32>																0000
		15:0																	0000
9060	ETHPMM0	31:16	PMM<31:0>																0000
		15:0																	0000
9070	ETHPMM1	31:16	PMM<63:32>																0000
		15:0																	0000
9080	ETHPMCS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMCS<15:0>																0000
9090	ETHPMO	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMO<15:0>																0000
90A0	ETHRXFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	HTEN	MPEN	—	NOTPM	PMMODE<3:0>				CRC ERREN	CRC OKEN	RUNT ERREN	RUNTEN	UCEN	NOT MEEN	MCEN	BCEN	0000
90B0	ETHRXWM	31:16	—	—	—	—	—	—	—	RXFWM<7:0>								0000	
		15:0	—	—	—	—	—	—	RXEWM<7:0>								0000		
90C0	ETHIEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TX BUSEIE	RX BUSEIE	—	—	—	EW MARKIE	FW MARKIE	RX DONEIE	PK TPENDIE	RX ACTIE	—	TX DONEIE	TX ABORTIE	RX BUFNAIE	RX OVFLWIE	0000
90D0	ETHIRQ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TXBUSE	RXBUSE	—	—	—	EWMARK	FWMARK	RXDONE	PKTPEND	RXACT	—	TXDONE	TXABORT	RXBUFNA	RXOVFLW	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

Note 2: Reset values default to the factory programmed value.

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REGISTER 25-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER (CONTINUED)

- bit 7 **CRCERREN:** CRC Error Collection Enable bit
1 = The received packet CRC must be invalid for the packet to be accepted
0 = Disable CRC Error Collection filtering
This bit allows the user to collect all packets that have an invalid CRC.
- bit 6 **CRCOKEN:** CRC OK Enable bit
1 = The received packet CRC must be valid for the packet to be accepted
0 = Disable CRC filtering
This bit allows the user to reject all packets that have an invalid CRC.
- bit 5 **RUNTERREN:** Runt Error Collection Enable bit
1 = The received packet must be a runt packet for the packet to be accepted
0 = Disable Runt Error Collection filtering

This bit allows the user to collect all packets that are runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes (when CRCOKEN = 0) or any packet with a size of less than 64 bytes that has a valid CRC (when CRCOKEN = 1).
- bit 4 **RUNTEN:** Runt Enable bit
1 = The received packet must not be a runt packet for the packet to be accepted
0 = Disable Runt filtering

This bit allows the user to reject all runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes.
- bit 3 **UCEN:** Unicast Enable bit
1 = Enable Unicast Filtering
0 = Disable Unicast Filtering

This bit allows the user to accept all unicast packets whose Destination Address matches the Station Address.
- bit 2 **NOTMEEN:** Not Me Unicast Enable bit
1 = Enable Not Me Unicast Filtering
0 = Disable Not Me Unicast Filtering

This bit allows the user to accept all unicast packets whose Destination Address does not match the Station Address.
- bit 1 **MCEN:** Multicast Enable bit
1 = Enable Multicast Filtering
0 = Disable Multicast Filtering

This bit allows the user to accept all Multicast Address packets.
- bit 0 **BCEN:** Broadcast Enable bit
1 = Enable Broadcast Filtering
0 = Disable Broadcast Filtering

This bit allows the user to accept all Broadcast Address packets.

- Note 1:** XOR = True when either one or the other conditions are true, but not both.
2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

- Note 1:** This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

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REGISTER 25-26: EMAC1IPGR: ETHERNET CONTROLLER MAC NON-BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
	—	NB2BIPKTGP1<6:0>						
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	NB2BIPKTGP2<6:0>						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14-8 **NB2BIPKTGP1<6:0>:** Non-Back-to-Back Interpacket Gap Part 1 bits

This is a programmable field representing the optional carrierSense window referenced in section 4.2.3.2.1 "Deference" of the IEEE 80.23 Specification. If the carrier is detected during the timing of IPGR1, the MAC defers to the carrier. If, however, the carrier comes after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision, thus ensuring fair access to the medium. Its range of values is 0x0 to IPGR2. Its recommend value is 0xC (12d).

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **NB2BIPKTGP2<6:0>:** Non-Back-to-Back Interpacket Gap Part 2 bits

This is a programmable field representing the non-back-to-back Inter-Packet-Gap. Its recommended value is 0x12 (18d), which represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 25-39: EMAC1SA2: ETHERNET CONTROLLER MAC STATION ADDRESS 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR2<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR1<7:0>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

P = Programmable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Reserved:** Maintain as '0'; ignore read

bit 15-8 **STNADDR2<7:0>:** Station Address Octet 2 bits
These bits hold the second transmitted octet of the station address.

bit 7-0 **STNADDR1<7:0>:** Station Address Octet 1 bits
These bits hold the most significant (first transmitted) octet of the station address.

- Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.
- 2:** This register is loaded at reset from the factory preprogrammed station address.

26.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS60001110) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Comparator module contains two comparators that can be configured in a variety of ways.

Key features of the Comparator module include:

- Selectable inputs available include:
 - Analog inputs multiplexed with I/O pins
 - On-chip internal absolute voltage reference (IVREF)
 - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the Comparator module is illustrated in Figure 26-1.

FIGURE 26-1: COMPARATOR MODULE BLOCK DIAGRAM

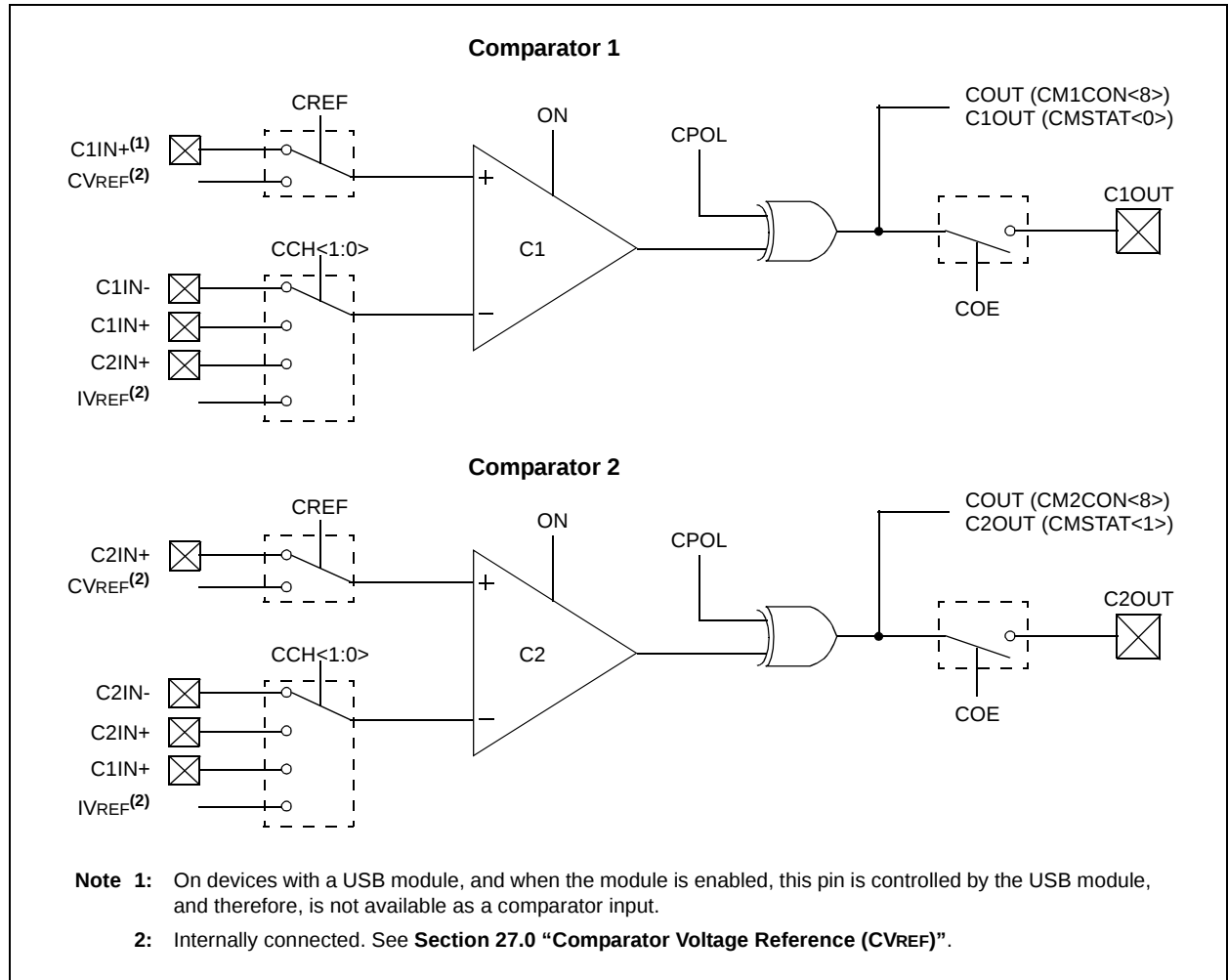


FIGURE 32-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

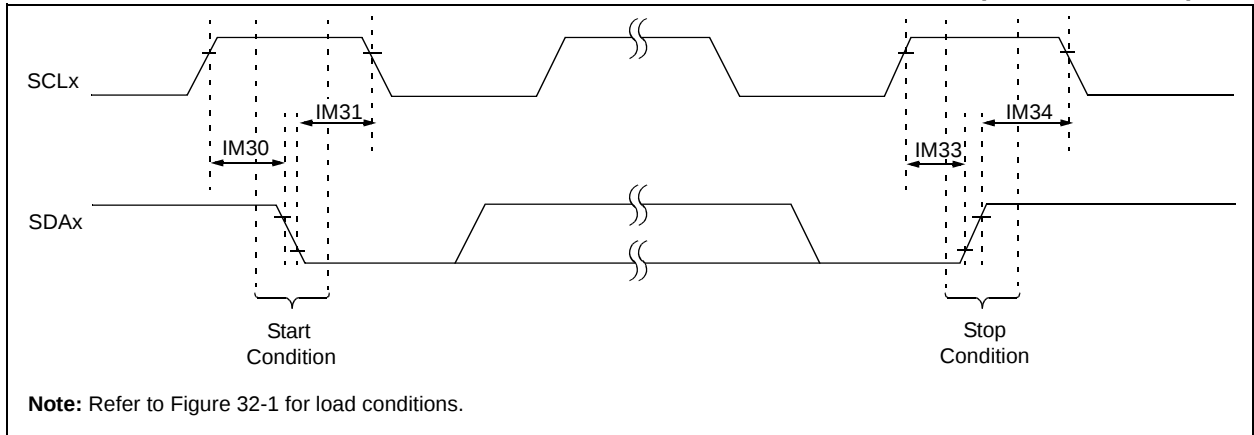
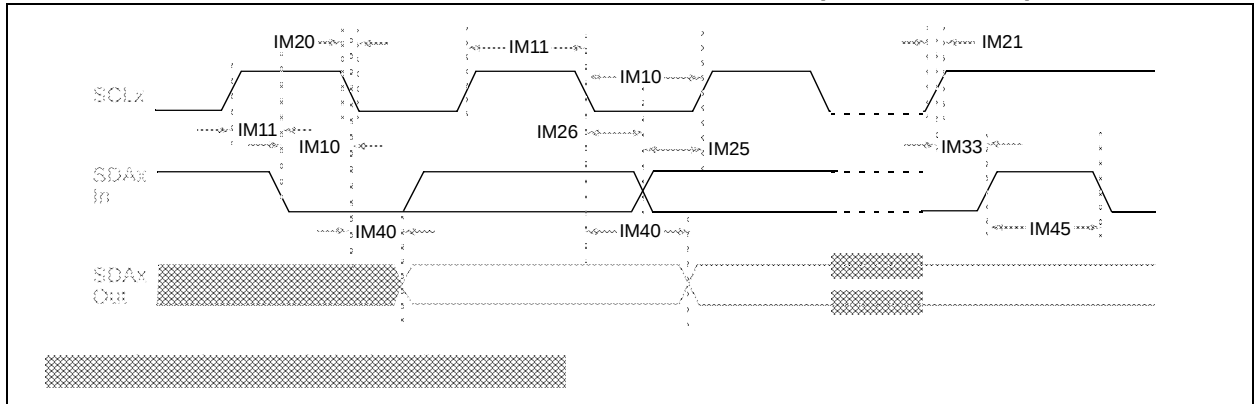


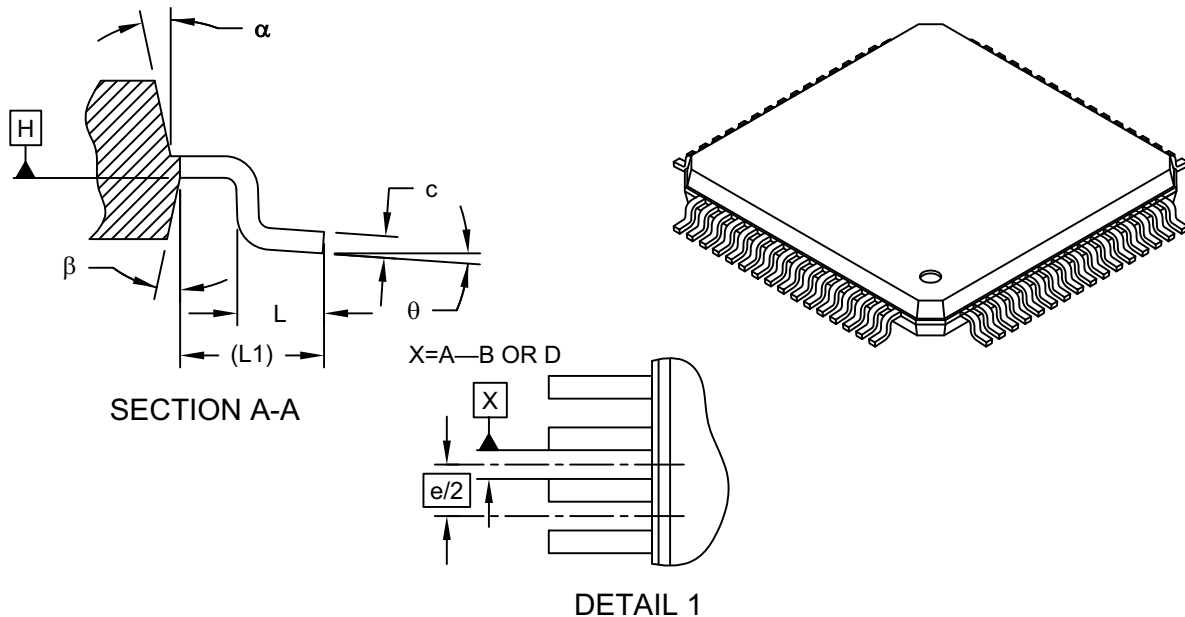
FIGURE 32-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



PIC32MX5XX/6XX/7XX

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		64		
Lead Pitch	e		0.50 BSC		
Overall Height	A	-	-	-	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	-	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	φ		0°	3.5°	7°
Overall Width	E		12.00 BSC		
Overall Length	D		12.00 BSC		
Molded Package Width	E1		10.00 BSC		
Molded Package Length	D1		10.00 BSC		
Lead Thickness	c		0.09	-	0.20
Lead Width	b		0.17	0.22	0.27
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

PIC32MX5XX/6XX/7XX

TABLE B-7: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
32.0 “Electrical Characteristics”	Note 4 in the Operating Current specification was updated (see Table 32-5). Note 3 in the Idle Current specification was updated (see Table 32-6). Note 6 references in the Power-Down Current specification were updated (see Table 32-7). The Program Memory parameters, D135, D136, and D137, and Note 4 were updated (see Table 32-11). The Voltage Reference Specifications were updated (see Table 32-14). Parameter DO50 (Cosco) was added to the Capacitive Loading Requirements on Output Pins (see Table 32-16). The EJTAG Timing Characteristics were updated (see Figure 32-28). The maximum value for parameters ET13 and ET14 were updated in the Ethernet Module Specifications (see Table 32-35). Parameter PM7 (TDHOLD) was updated (see Table 32-40).
34.0 “Packaging Information”	Packaging diagrams were updated.
Product Identification System	The Speed and Program Memory Size were updated and Note 1 was added.

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