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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f512l-80i-pf

PIC32MX5XX/6XX/7XX

TABLE 1: PIC32MX5XX USB AND CAN FEATURES

USB and CAN																
Device	Pins	Program Memory (KB)	Data Memory (KB)	USB	CAN	Timers/Capture/Compare	DMA Channels (Programmable/Dedicated)	UART ^(2,3)	SPI ⁽³⁾	I ² C ⁽³⁾	10-bit 1 Msps ADC (Channels)	Comparators	PMP/PSP	JTAG	Trace	Packages ⁽⁴⁾
PIC32MX534F064H	64	64 + 12 ⁽¹⁾	16	1	1	5/5/5	4/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX564F064H	64	64 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX564F128H	64	128 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX575F256H	64	256 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX575F512H	64	512 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX534F064L	100	64 + 12 ⁽¹⁾	16	1	1	5/5/5	4/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX564F064L	100	64 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX564F128L	100	128 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX575F256L	100	256 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX575F512L	100	512 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG

Legend: PF, PT = TQFP MR = QFN BG = TFBGA TL = VTLA⁽⁵⁾

Note 1: This device features 12 KB boot Flash memory.

Note 2: CTS and RTS pins may not be available for all UART modules. Refer to the “**Device Pin Tables**” section for more information.

Note 3: Some pins between the UART, SPI and I²C modules may be shared. Refer to the “**Device Pin Tables**” section for more information.

Note 4: Refer to **34.0 “Packaging Information”** for more information.

Note 5: 100-pin devices in the VTLA package are available upon request. Please contact your local Microchip Sales Office for details.

PIC32MX5XX/6XX/7XX

TABLE 12: PIN NAMES FOR USB, ETHERNET, AND CAN DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX764F128L PIC32MX775F256L PIC32MX775F512L PIC32MX795F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1	
Pin #	Full Pin Name	Pin #	Full Pin Name
J3	PGED2/AN7/RB7	K8	VDD
J4	AVDD	K9	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
J5	AN11/ERXERR/AETXERR/PMA12/RB11	K10	USBID/RF3
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2
J7	AN12/ERXD0/AECRS/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6
J8	No Connect (NC)	L2	VREF-/CVREF-/AERXD2/PMA7/RA9
J9	No Connect (NC)	L3	AVSS
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10
K1	PGEC1/AN1/CN3/RB1	L6	AC1TX/SCK4/U5TX/U2RTS/RF13
K2	PGED1/AN0/CN2/RB0	L7	AN13/ERXD1/AECOL/PMA10/RB13
K3	VREF+/CVREF+/AERXD3/PMA6/RA10	L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
K4	AN8/C1OUT/RB8	L9	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
K6	AC1RX/SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14		

- Note** 1: This pin is not available on PIC32MX764F128L devices.
 2: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 18-16 **PLLMULT<2:0>**: Phase-Locked Loop (PLL) Multiplier bits

- 111 = Clock is multiplied by 24
- 110 = Clock is multiplied by 21
- 101 = Clock is multiplied by 20
- 100 = Clock is multiplied by 19
- 011 = Clock is multiplied by 18
- 010 = Clock is multiplied by 17
- 001 = Clock is multiplied by 16
- 000 = Clock is multiplied by 15

bit 15 **Unimplemented**: Read as '0'

bit 14-12 **COSC<2:0>**: Current Oscillator Selection bits

- 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC (FRC) Oscillator divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (Sosc)
- 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (Posc) (XT, HS or EC)
- 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast RC (FRC) Oscillator

bit 11 **Unimplemented**: Read as '0'

bit 10-8 **NOSC<2:0>**: New Oscillator Selection bits

- 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC Oscillator (FRC) divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (Sosc)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (XT, HS or EC)
- 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK**: Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):

- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):

Clock and PLL selections are never locked and may be modified.

bit 6 **ULOCK**: USB PLL Lock Status bit

- 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
- 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled

bit 5 **SLOCK**: PLL Lock Status bit

- 1 = PLL module is in lock or PLL module start-up timer is satisfied
- 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **SLPEN**: Sleep Mode Enable bit

- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF**: Clock Fail Detect bit

- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

PIC32MX5XX/6XX/7XX

REGISTER 11-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 11-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

15.1 Control Registers

TABLE 15-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets ⁽²⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					—	WDTCLR	0000

- Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
- Note** 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2: Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

19.0 INTER-INTEGRATED CIRCUIT (I²C)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I²C)”** (DS60001116) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard. Figure 19-1 illustrates the I²C module block diagram.

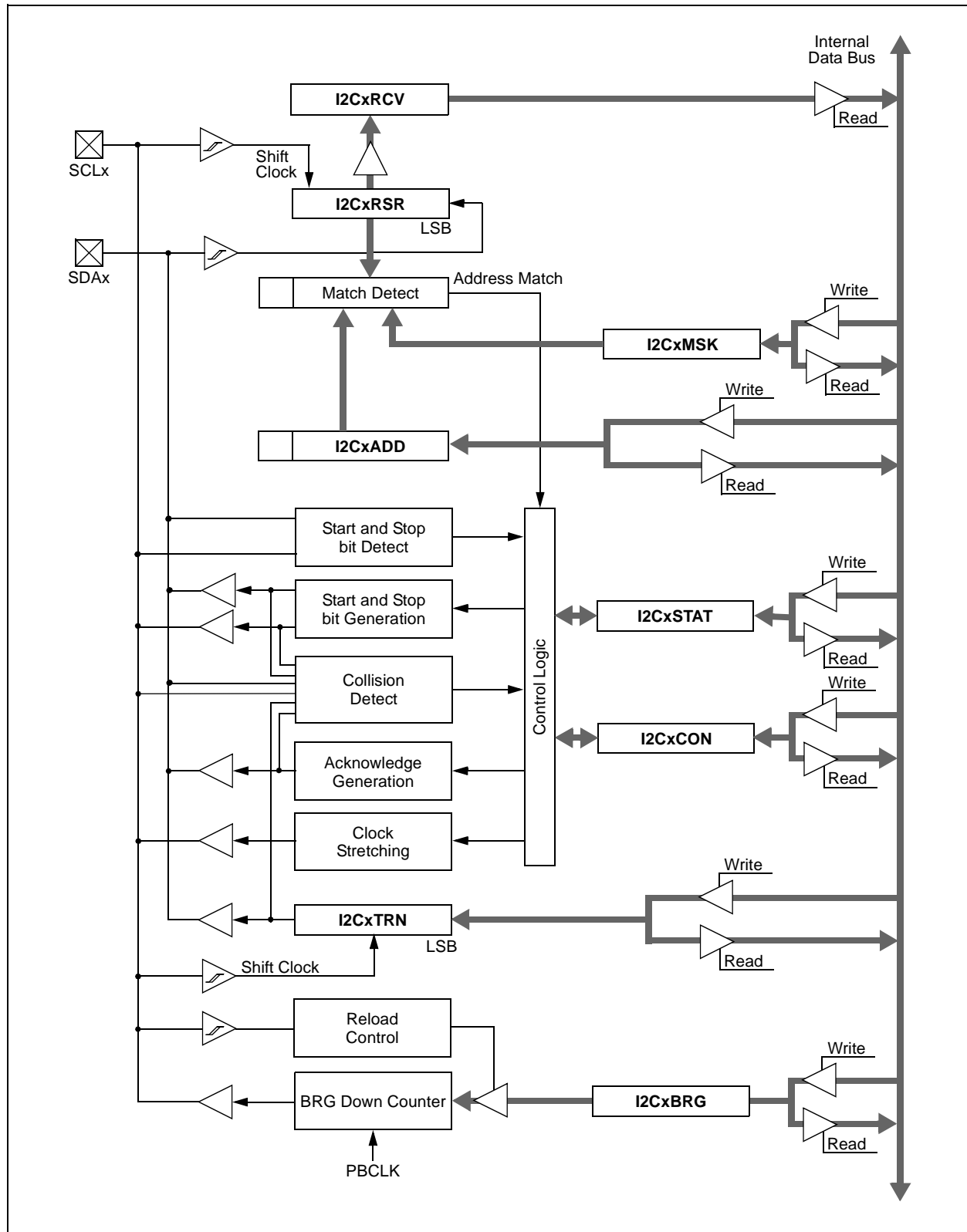
Each I²C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module offers the following key features:

- I²C interface supporting both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

PIC32MX5XX/6XX/7XX

FIGURE 19-1: I²C BLOCK DIAGRAM



REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)

- bit 13 **SIDLE:** CAN Stop in Idle bit
 1 = CAN Stops operation when system enters Idle mode
 0 = CAN continues operation when system enters Idle mode
- bit 12 **Unimplemented:** Read as '0'
- bit 11 **CANBUSY:** CAN Module is Busy bit
 1 = The CAN module is active
 0 = The CAN module is completely disabled
- bit 10-5 **Unimplemented:** Read as '0'
- bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
 10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
 10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
 •
 •
 •
 00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
 00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 24-13: CifLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)

- bit 15 **FLTEN13**: Filter 13 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 14-13 **MSEL13<1:0>**: Filter 13 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL13<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN12**: Filter 12 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 6-5 **MSEL12<1:0>**: Filter 12 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL12<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MX5XX/6XX/7XX

REGISTER 24-22: CiFIFOUn: CAN FIFO USER ADDRESS REGISTER 'n' (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUn<31:24>							
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUn<23:16>							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUn<15:8>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-0 ⁽¹⁾	R-0 ⁽¹⁾
	CiFIFOUn<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CiFIFOUn<31:0>**: CAN FIFO User Address bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit will always read '0', which forces byte-alignment of messages.

Note: This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

REGISTER 24-23: CiFIFOCIN: CAN MODULE MESSAGE INDEX REGISTER 'n' (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	CiFIFOCIN<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-5 **Unimplemented**: Read as '0'

bit 4-0 **CiFIFOCIN<4:0>**: CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return an index to the message that the FIFO will use to save the next message.

25.0 ETHERNET CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 35. “Ethernet Controller”** (DS60001155) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

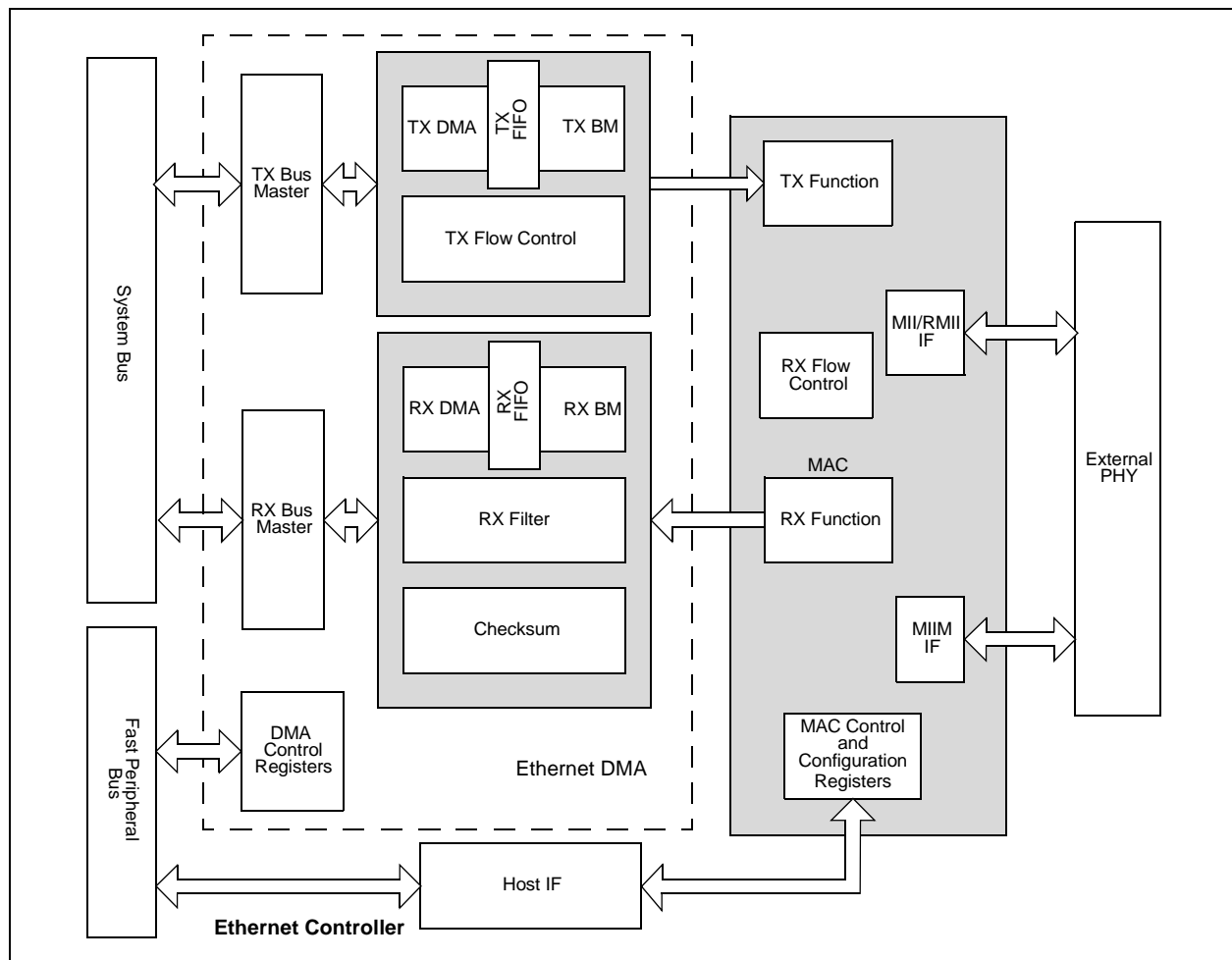
The Ethernet controller is a bus master module that interfaces with an off-chip Physical Layer (PHY) to implement a complete Ethernet node in a system.

Key features of the Ethernet Controller include:

- Supports 10/100 Mbps data transfer rates
- Supports full-duplex and half-duplex operation
- Supports RMI and MII PHY interface
- Supports MIIM PHY management interface
- Supports both manual and automatic Flow Control
- RAM descriptor-based DMA operation for both receive and transmit path
- Fully configurable interrupts
- Configurable receive packet filtering
 - CRC check
 - 64-byte pattern match
 - Broadcast, multicast and unicast packets
 - Magic Packet™
 - 64-bit hash table
 - Runt packet
- Supports packet payload checksum calculation
- Supports various hardware statistics counters

Figure 25-1 illustrates a block diagram of the Ethernet controller.

FIGURE 25-1: ETHERNET CONTROLLER BLOCK DIAGRAM



PIC32MX5XX/6XX/7XX

REGISTER 25-17: ETHFRMTXOK: ETHERNET CONTROLLER FRAMES TRANSMITTED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMTXOKCNT<15:0>:** Frame Transmitted OK Count bits
Increment counter for frames successfully transmitted.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

PIC32MX5XX/6XX/7XX

REGISTER 25-28: EMAC1MAXF: ETHERNET CONTROLLER MAC MAXIMUM FRAME LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	MACMAXF<15:8> ⁽¹⁾							
7:0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
	MACMAXF<7:0> ⁽¹⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MACMAXF<15:0>:** Maximum Frame Length bits⁽¹⁾

These bits reset to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter/longer maximum length restriction is desired, program this 16-bit field.

Note 1: If a proprietary header is allowed, this bit should be adjusted accordingly. For example, if 4-byte headers are prepended to frames, MACMAXF could be set to 1527 octets. This would allow the maximum VLAN tagged frame plus the 4-byte header.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

PIC32MX5XX/6XX/7XX

REGISTER 25-34: EMAC1MWTD: ETHERNET CONTROLLER MAC MII MANAGEMENT WRITE DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MWTD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MWTD<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MWTD<15:0>:** MII Management Write Data bits

When written, a MII Management write cycle is performed using the 16-bit data and the pre-configured PHY and Register addresses from the EMAC1MADR register.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 25-35: EMAC1MRDD: ETHERNET CONTROLLER MAC MII MANAGEMENT READ DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MRDD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MRDD<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MRDD<15:0>:** MII Management Read Data bits

Following a MII Management Read Cycle, the 16-bit data can be read from this location.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

31.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

31.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

PIC32MX5XX/6XX/7XX

TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions		
Idle Current (I _{IDLE}) ⁽¹⁾ for PIC32MX534/564/664/764 Family Devices						
DC30a	1.5	5	mA	-40°C, +25°C, +85°C	—	4 MHz
DC30c	3.5	6		+105°C		
DC31a	7	11		-40°C, +25°C, +85°C		
DC32a	13	20	mA	-40°C, +25°C, +85°C	—	25 MHz (Note 3)
DC33a	17	25	mA	-40°C, +25°C, +85°C	—	80 MHz
DC33c	20	27		+105°C		
DC34c	—	40	μA	-40°C	2.3V	LPRC (31 kHz) (Note 3)
DC34d		75		+25°C		
DC34e		800		+85°C		
DC34f		1000		+105°C		
DC35c	30	—	μA	-40°C	3.3V	
DC35d	55			+25°C		
DC35e	230			+85°C		
DC35f	800			+105°C		
DC36c	—	43	μA	-40°C	3.6V	
DC36d		106		+25°C		
DC36e		800		+85°C		
DC36f		1000		+105°C		

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0)
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to V_{SS}
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
- 2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** This parameter is characterized, but not tested in manufacturing.
- 4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

FIGURE 32-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

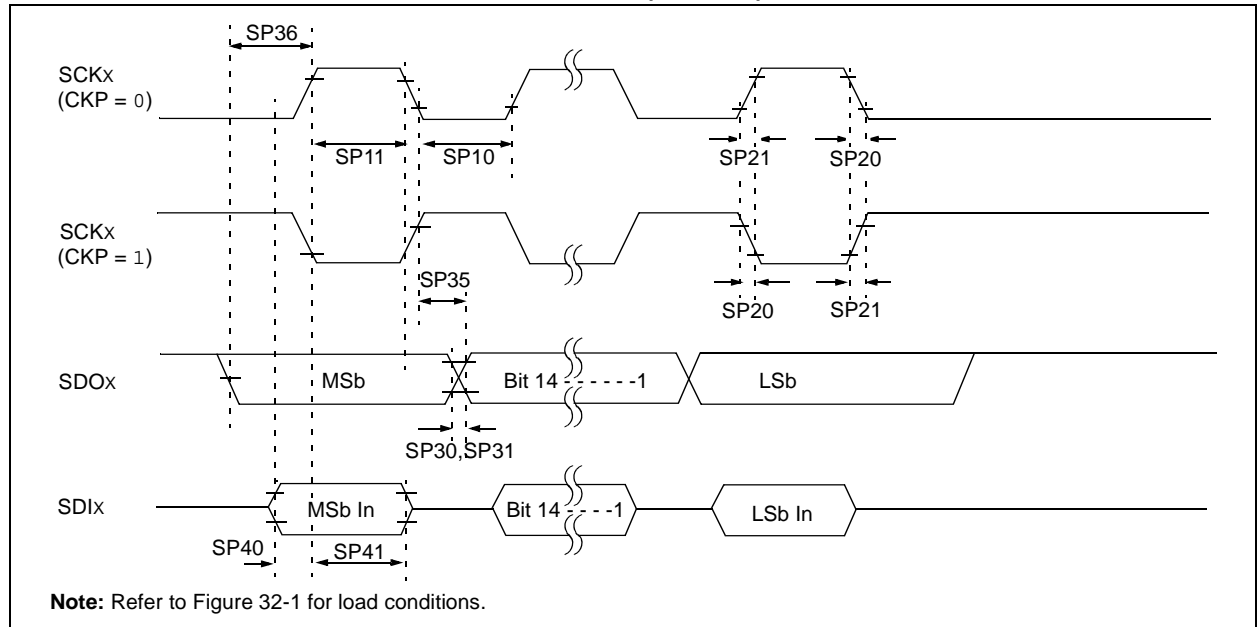


TABLE 32-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TsCL	SCKx Output Low Time ⁽³⁾	TsCK/2	—	—	ns	—
SP11	TsCH	SCKx Output High Time ⁽³⁾	TsCK/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP30	TdOF	SDOx Data Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP31	TdOR	SDOx Data Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP35	TsCH2DoV, TsCL2DoV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP36	TdOV2sc, TdOV2sCL	SDOx Data Output Setup to First SCKx Edge	15	—	—	ns	—
SP40	TdIV2sch, TdIV2sCL	Setup Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V
SP41	TsCH2dIL, TsCL2dIL	Hold Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 32-38: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	Analog-to-Digital Clock Period ⁽²⁾	65	—	—	ns	See Table 32-37
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1 TAD	—	—	—	TSAMP must be ≥ 132 ns
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽³⁾	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from Analog-to-Digital Off to Analog-to-Digital On ⁽³⁾	—	—	2	μs	—

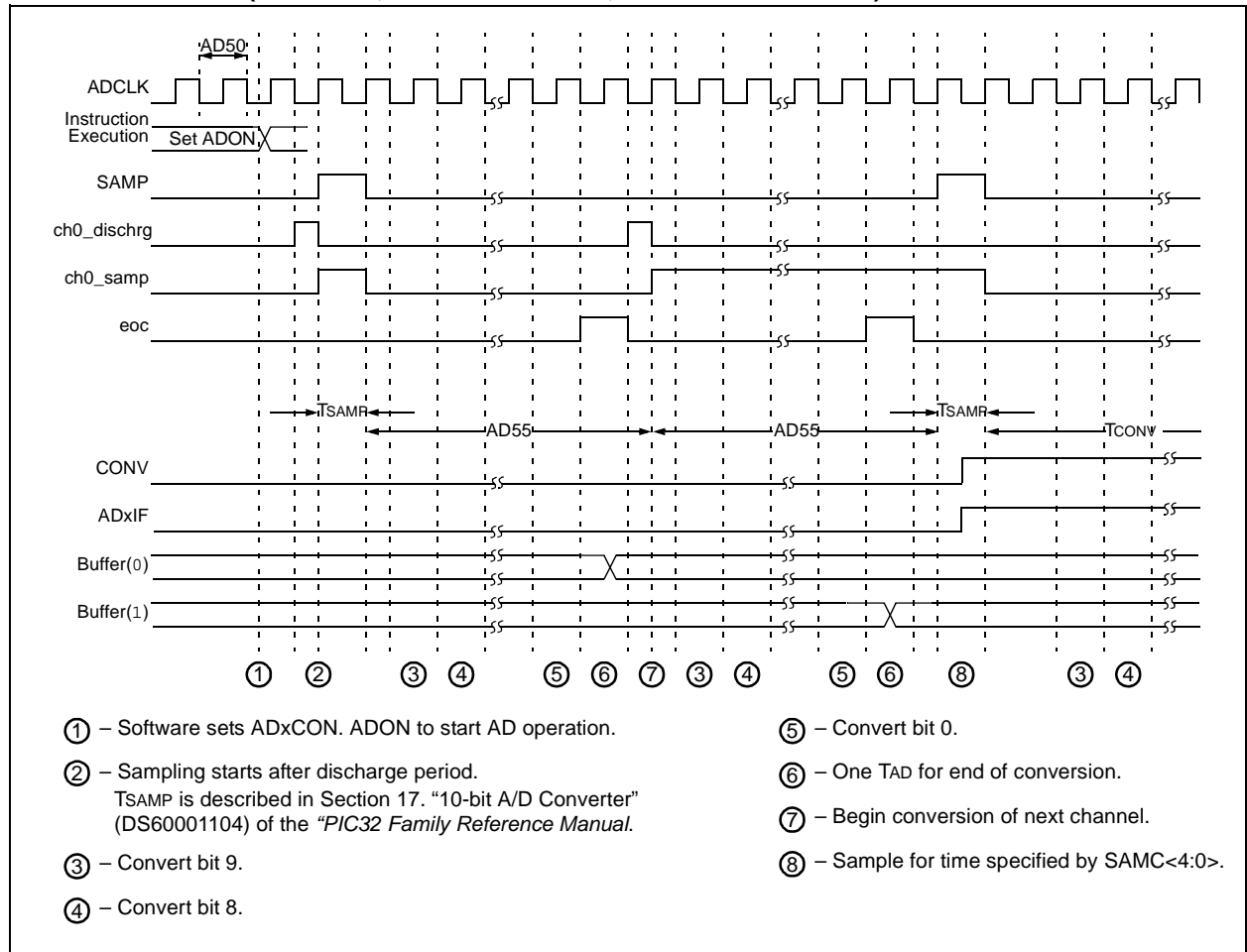
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

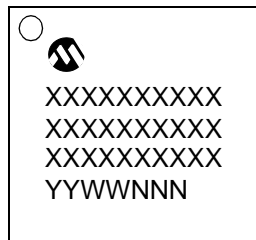
FIGURE 32-24: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS
(ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)



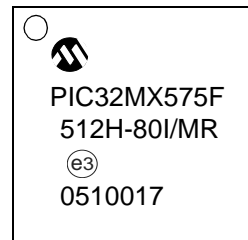
PIC32MX5XX/6XX/7XX

34.1 Package Marking Information (Continued)

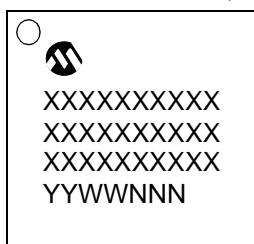
64-Lead QFN (9x9x0.9 mm)



Example



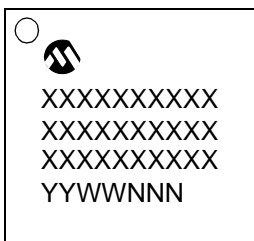
121-Lead TFBGA (10x10x1.1 mm)



Example



124-Lead VTLA (9x9x0.9 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	*	Pb-free JEDEC designator for Matte Tin (Sn)
		This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.