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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f512lt-80i-pf

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 4-1: SFR MEMORY MAP

	Virtual A	Address
Peripheral	Base	Offset Start
Watchdog Timer		0x0000
RTCC		0x0200
Timer1-Timer5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
I2C1-I2C5		0x5000
SPI1-SPI4		0x5800
UART1-UART6		0x6000
PMP	UXDFOU	0x7000
ADC		0x9000
CVREF		0x9800
Comparator		0xA000
Oscillator		0xF000
Device and Revision ID		0xF200
Flash Controller		0xF400
Reset		0xF600
Interrupts		0x1000
Bus Matrix		0x2000
DMA		0x3000
Prefetch	0xBF88	0x4000
USB		0x5040
PORTA-PORTG		0x6000
Ethernet		0x9000
Configuration	0xBFC0	0x2FF0

|--|

Interrupt Source(1)	IRQ	Vector	Interrupt Bit Location					
Interrupt Source.	Number	Number	Flag	Enable	Priority	Sub-Priority		
IC3E – Input Capture 3 Error	63	13	IFS1<31>	IEC1<31>	IPC3<12:10>	IPC3<9:8>		
IC4E – Input Capture 4 Error	64	17	IFS2<0>	IEC2<0>	IPC4<12:10>	IPC4<9:8>		
IC5E – Input Capture 5 Error	65	21	IFS2<1>	IEC2<1>	IPC5<12:10>	IPC5<9:8>		
PMPE – Parallel Master Port Error	66	28	IFS2<2>	IEC2<2>	IPC7<4:2>	IPC7<1:0>		
U4E – UART4 Error	67	49	IFS2<3>	IEC2<3>	IPC12<12:10>	IPC12<9:8>		
U4RX – UART4 Receiver	68	49	IFS2<4>	IEC2<4>	IPC12<12:10>	IPC12<9:8>		
U4TX – UART4 Transmitter	69	49	IFS2<5>	IEC2<5>	IPC12<12:10>	IPC12<9:8>		
U6E – UART6 Error	70	50	IFS2<6>	IEC2<6>	IPC12<20:18>	IPC12<17:16>		
U6RX – UART6 Receiver	71	50	IFS2<7>	IEC2<7>	IPC12<20:18>	IPC12<17:16>		
U6TX – UART6 Transmitter	72	50	IFS2<8>	IEC2<8>	IPC12<20:18>	IPC12<17:16>		
U5E – UART5 Error	73	51	IFS2<9>	IEC2<9>	IPC12<28:26>	IPC12<25:24>		
U5RX – UART5 Receiver	74	51	IFS2<10>	IEC2<10>	IPC12<28:26>	IPC12<25:24>		
U5TX – UART5 Transmitter	75	51	IFS2<11>	IEC2<11>	IPC12<28:26>	IPC12<25:24>		
(Reserved)	_	_	_					
	Lowe	st Natural (Order Priority	/				

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX5XX USB and CAN Features", TABLE 2: "PIC32MX6XX USB and Ethernet Features" and TABLE 3: "PIC32MX7XX USB, Ethernet, and CAN Features" for the list of available peripherals.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

ess										В	its								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3400		31:16	_	_	—	—	—	—	_	—	—	—	_	—	_	—		_	0000
3400	DONIJDAI	15:0	—	—	—	—	—	—	—	—				CHPDA	T<7:0>				0000
34F0	DCH6CON	31:16	_	_	—	—	—	—	_	—	—	—	_	—	_	_	_	—	0000
0.20	201100011	15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPR	l<1:0>	0000
34F0	DCH6ECON	31:16	—	_	-	-			_	-	050005	OADODT	DATEN	CHAIR	Q<7:0>				00FF
		15:0				CHSIR	Q<7:0>					CABORT							FF00
3500	DCH6INT	15.0									CHSDIE	CHSHIE							0000
		31:16									CHODI	CHOIM	CIIDDII	CHDHII	CLIPCII	CHOON	OTTAI	CHLINI	0000
3510	DCH6SSA	15:0								CHSSA	A<31:0>								0000
0500	DOLIODOA	31:16								01100									0000
3520	DCH6DSA	15:0								CHDSA	A<31:0>								0000
3530	DCH6SSIZ	31:16	—	-	—	_	_	_	_	—	_	_	-	_	-	_	_	-	0000
3330	DCH000012	15:0 CHSSIZ<15:0> 0000																	
3540	DCH6DSIZ	31:16	_	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	5:0 CHDSIZ<15:0> 00									0000							
3550	DCH6SPTR	31:16	—	—	—	—	—	—	—		— —	—	—	—	—	—	—	—	0000
		15:0								CHSPT	R<15:0>								0000
3560	DCH6DPTR	15.0	_	_	_	—	_	—	_	CHDPT	— R<15:0>	—	_	_	—	—	-	_	0000
-		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3570	DCH6CSIZ	15:0								CHCSI	Z<15:0>								0000
0500		31:16	_	_	_	_	_	—	_	_	_	_	_	_	_	_	_	_	0000
3580	DCH6CPTR	15:0			•					CHCPT	R<15:0>			•					0000
3590		31:16	—		—	—	—	—		—	—	—	-	_	-	_	—	-	0000
0000	DONODAI	15:0		—	—	—	—	—	_	—				CHPDA	T<7:0>				0000
35A0	DCH7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	_	—	0000
		15:0	CHBUSY							CHCHNS	CHEN	CHAED	CHCHN	CHAEN		CHEDET	CHPR	l<1:0>	0000
35B0	DCH7ECON	31:16		_			-	_	_		CEORCE	CARODT							OOFF
		15.0	_	_	_		Q<7.0>		_	_									FF00
35C0	DCH7INT	15.0	_	_	_	_	_	_	_	_	CHSDIE	CHSHIF	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		31:16									0110211	0110111	01001		0112011	0110011	U 117.01	JILIN	0000
35D0	DCH7SSA	15:0								CHSSA	A<31:0>								0000
2552		31:16																	0000
35E0	DCH/DSA	15:0								CHDSA	4<31:0>								0000
Legen	d: x = u	Inknowr	value on Re	eset; — = ui	nimplemente	d, read as '0	'. Reset val	ues are show	vn in hexade	ecimal.									

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information. Note 1:

DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices. 2:

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
15:8	ON ⁽¹⁾	—	—	SUSPEND	DMABUSY	—	—	—
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	_		_	_	_

REGISTER 10-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- ON: DMA On bit⁽¹⁾ bit 15
 - 1 = DMA module is enabled
 - 0 = DMA module is disabled
- bit 14-13 Unimplemented: Read as '0'
- bit 12 SUSPEND: DMA Suspend bit
 - 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
 - 0 = DMA operates normally
- bit 11 DMABUSY: DMA Module Busy bit
 - 1 = DMA module is active
 - 0 = DMA module is disabled and not actively transferring data
- bit 10-0 Unimplemented: Read as '0'
- Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX5XX/6XX/7XX



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	—	—	—	—	—	—	—	—
7.0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
7:0							FRMH<2:0>	

REGISTER 11-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-3 Unimplemented: Read as '0'

bit 2-0 **FRMH<2:0>:** Upper 3 bits of the Frame Numbers bits These register bits are updated with the current frame number whenever a SOF TOKEN is received.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0		PID<	<3:0>		EP<3:0>			

REGISTER 11-15: U1TOK: USB TOKEN REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-4 PID<3:0>: Token Type Indicator bits⁽¹⁾ 1101 = SETUP (TX) token type transaction 1001 = IN (RX) token type transaction 0001 = OUT (TX) token type transaction Note: All other values not listed, are Reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits The four bit value must specify a valid endpoint.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—		-					
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	—	_							
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15:8	—	—							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	BDTPTRH<23:16>								

REGISTER 11-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 BDTPTRH<23:16>: BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 11-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—		—				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—		_				
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—		—				
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0				BDTPTR	U<31:24>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 BDTPTRU<31:24>: BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

TABLE 12-13: CHANGE NOTICE AND PULL-UP REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512 AND PIC32MX795F512L DEVICES PIC32MX795F512L DEVICES

ess				Bits												\$			
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
C1 C0		31:16	_		_	_	—	_	_	_		_	_	_		_	_	_	0000
6100	CINCOIN	15:0	ON	—	SIDL	_	_	_	_	_	—	_	_	_	_	_	_	_	0000
6100		31:16	—	_		-				_	_		CNEN21	CNEN20	CNEN19	CNEN18	CNEN17	CNEN16	0000
61D0 CNEN	CINEIN	15:0	CNEN15	CNEN14	CNEN13	CNEN12	CNEN11	CNEN10	CNEN9	CNEN8	CNEN7	CNEN6	CNEN5	CNEN4	CNEN3	CNEN2	CNEN1	CNEN0	0000
6150		31:16	—										CNPUE21	CNPUE20	CNPUE19	CNPUE18	CNPUE17	CNPUE16	0000
61E0 CNPU	CINPUE	15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	CNPUE11	CNPUE10	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 12-14: CHANGE NOTICE AND PULL-UP REGISTER MAP FOR PIC32MX575F256H, PIC32MX575F512H, PIC32MX675F512H, PIC32MX675F512H, PIC32MX675F512H, PIC32MX775F512H, PIC32MX775F512H, PIC32MX795F512H, DEVICES

ess			Bits									6							
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6100	CNICON	31:16	-	_	_	-	—	-	—	-	-	_	-	—	_	—	-	—	0000
6100	CINCOIN	15:0	ON	_	SIDL	-		—	-	—	-	_	-	—	_	—	-		0000
6100		31:16		_	-	_	_	_	_		_	_	_		_	CNEN18	CNEN17	CNEN16	0000
0100	CINEIN	15:0	CNEN15	CNEN14	CNEN13	CNEN12	CNEN11	CNEN10	CNEN9	CNEN8	CNEN7	CNEN6	CNEN5	CNEN4	CNEN3	CNEN2	CNEN1	CNEN0	0000
6150		31:16		-	-	_	_	-	—	-	—	_	_	-	_	CNPUE18	CNPUE17	CNPUE16	0000
OTEU	CINPUE	15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	CNPUE11	CNPUE10	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	—	FEDGE	C32
7.0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
7:0	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16	Unimplemented: Read as '0'
bit 15	ON: Input Capture Module Enable bit ⁽¹⁾
	 1 = Module is enabled 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Stop in Idle Control bit
	1 = Halt in Idle mode0 = Continue to operate in Idle mode
bit 12-10	Unimplemented: Read as '0'
bit 9	FEDGE: First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
	 1 = Capture rising edge first 0 = Capture falling edge first
bit 8	C32: 32-bit Capture Select bit
	1 = 32-bit timer resource capture0 = 16-bit timer resource capture
bit 7	ICTMR: Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
	 1 = Timer2 is the counter source for capture 0 = Timer3 is the counter source for capture
bit 6-5	ICI<1:0>: Interrupt Control bits
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	00 = Interrupt on every second capture event
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
	 1 = Input capture overflow is occurred 0 = No input capture overflow is occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	 1 = Input capture buffer is not empty; at least one more capture value can be read 0 = Input capture buffer is empty

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

- bit 2-0 ICM<2:0>: Input Capture Mode Select bits
 - 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
 - 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
 - 101 = Prescaled Capture Event mode every sixteenth rising edge
 - 100 = Prescaled Capture Event mode every fourth rising edge
 - 011 = Simple Capture Event mode every rising edge
 - 010 = Simple Capture Event mode every falling edge
 - 001 = Edge Detect mode every edge (rising and falling)
 - 000 = Input Capture module is disabled
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 22-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)

- bit 3 RTCWREN: RTC Value Registers Write Enable bit⁽⁴⁾
 - 1 = RTC Value registers can be written to by the user
 - 0 = RTC Value registers are locked out from being written to by the user
- bit 2 RTCSYNC: RTCC Value Registers Read Synchronization bit
 - 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
 - 0 = RTC Value registers can be read without concern about a rollover ripple
- bit 1 HALFSEC: Half-Second Status bit⁽⁵⁾
 - 1 = Second half period of a second
- 0 = First half period of a second
- bit 0 RTCOE: RTCC Output Enable bit
 - 1 = RTCC clock output is enabled (clock presented onto an I/O)
 - 0 = RTCC clock output is disabled
- **Note 1:** The ON bit is only writable when RTCWREN = 1.
 - 2: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
 - 4: The RTCWREN bit can only be set when the write sequence is enabled.
 - 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is only reset on a Power-on Reset (POR).

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24	FLTEN27	MSEL2	27<1:0>			FSEL27<4:0>	•		
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	FLTEN26	MSEL2	26<1:0>	FSEL26<4:0>					
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15.6	FLTEN25	MSEL2	25<1:0>	FSEL25<4:0>					
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	FLTEN24	MSEL2	24<1:0>	FSEL24<4:0>					

REGISTER 24-16: CIFLTCON6: CAN FILTER CONTROL REGISTER 6

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN27: Filter 27 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL27<1:0>: Filter 27 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
hit 20 24	
DIL 20-24	FSEL2/<4.0>. FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buller 31
	• •
	•
	00001 = Message matching filter is stored in FIFO buffer 1
hit 00	ELTEN26. Eiter 26 Enchlo bit
DIL 23	FLIENZO. FIREI ZO ENADIE DI
	0 = Filter is disabled
bit 22-21	MSEL26<1:0>: Filter 26 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 20-16	FSEL26<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 24-17: CIFLTCON7: CAN FILTER CONTROL REGISTER 7 (CONTINUED)

bit 15	FLTEN29: Filter 29 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 14-13	MSEL29<1:0>: Filter 29 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 12-8	FSEL29<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 7	FLTEN28: Filter 28 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 6-5	MSEL28<1:0>: Filter 28 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask U selected
bit 4-0	FSEL28<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
51.24		PMM<31:24>										
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
23.10	PMM<23:16>											
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
15.6	PMM<15:8>											
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
7.0				PMM	<7:0>							

REGISTER 25-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER

Legend:

- 5			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24	PMM<31:24>: Pattern Match Mask 3 bits
hit 23-16	PMM-23-16- Pattern Match Mask 2 hits

- bit 23-16 PMM<23:16>: Pattern Match Mask 2 bits
- bit 15-8 **PMM<15:8>:** Pattern Match Mask 1 bits
- bit 7-0 PMM<7:0>: Pattern Match Mask 0 bits
- Note 1: This register is only used for RX operations.
 2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 25-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	PMM<63:56>									
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	PMM<55:48>									
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15.6	PMM<47:40>									
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7.0				PMM<	39:32>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented b	oit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

PMM<63:56>: Pattern Match Mask 7 bits
PMM<55:48>: Pattern Match Mask 6 bits
PMM<47:40>: Pattern Match Mask 5 bits
PMM<39:32>: Pattern Match Mask 4 bits

Note 1: This register is only used for RX operations. 2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0						
31.24		_	—	—	—	—	—	—
00.40	U-0	U-0						
23.10		—	—	—	—	—	—	—
15.0	U-0	U-0						
15:8		—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
			_	_	_	TESTBP	TESTPAUSE ⁽¹⁾	SHRTQNTA ⁽¹⁾

REGISTER 25-30: EMAC1TEST: ETHERNET CONTROLLER MAC TEST REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 Unimplemented: Read as '0'

- bit 2 TESTBP: Test Backpressure bit
 - 1 = The MAC will assert backpressure on the link. Backpressure causes preamble to be transmitted, raising carrier sense. A transmit packet from the system will be sent during backpressure.
 0 = Normal operation

bit 1 **TESTPAUSE:** Test PAUSE bit⁽¹⁾

- 1 = The MAC Control sub-layer will inhibit transmissions, just as if a PAUSE Receive Control frame with a non-zero pause time parameter was received
- 0 = Normal operation

bit 0 SHRTQNTA: Shortcut PAUSE Quanta bit⁽¹⁾

- 1 = The MAC reduces the effective PAUSE Quanta from 64 byte-times to 1 byte-time
- 0 = Normal operation
- **Note 1:** This bit is only for testing purposes.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

27.1 Control Register

TABLE 27-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

ess		0		Bits												ú			
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
		04.40																	
0000		31:16	_	—		_	_			_	_	_			_		_	_	0000
9800	CVRCON	15:0	ON	_	-	-		VREFSEL ⁽²⁾	BGSEL	<1:0> ⁽²⁾	_	CVROE	CVRR	CVRSS		CVR<	3:0>		0100

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: These bits are not available on PIC32MX575/675/695/775/795 devices. On these devices, reset value for CVRCON is '0000'.

REGISTER 29-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

- bit 3 ICESEL: In-Circuit Emulator/Debugger Communication Channel Select bit
 - 1 = PGEC2/PGED2 pair is used
 - 0 = PGEC1/PGED1 pair is used
- bit 2 Reserved: Write '1'
- bit 1-0 DEBUG<1:0>: Background Debugger Enable bits (forced to '11' if code-protect is enabled)
 - 11 = Debugger is disabled
 - 10 = Debugger is enabled
 - 01 = Reserved (same as '11' setting)
 - 00 = Reserved (same as '11' setting)



TABLE 32-29: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

АС СНА	ARACTERIS	TICS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-Temp						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions		
SP10	TscL	SCKx Output Low Time ⁽³⁾	Tsck/2	—		ns	—		
SP11	TscH	SCKx Output High Time ⁽³⁾	Tsck/2	—	—	ns	—		
SP20	TscF	SCKx Output Fall Time ⁽⁴⁾		—		ns	See parameter DO32		
SP21	TscR	SCKx Output Rise Time ⁽⁴⁾		_		ns	See parameter DO31		
SP30	TDOF	SDOx Data Output Fall Time ⁽⁴⁾	_	—	_	ns	See parameter DO32		
SP31	TDOR	SDOx Data Output Rise Time ⁽⁴⁾		_		ns	See parameter DO31		
SP35	TscH2doV,	SDOx Data Output Valid after	_	—	15	ns	VDD > 2.7V		
	TscL2doV	SCKx Edge	_	—	20	ns	Vdd < 2.7V		
SP36	TDOV2SC, TDOV2SCL	SDOx Data Output Setup to First SCKx Edge	15	—		ns	—		
SP40	TDIV2scH,	Setup Time of SDIx Data Input to	15	_		ns	VDD > 2.7V		
	TDIV2scL	SCKx Edge	20	—	_	ns	VDD < 2.7V		
SP41	TscH2DIL,	Hold Time of SDIx Data Input	15	_	_	ns	VDD > 2.7V		
	TscL2DIL	to SCKx Edge	20	_	_	ns	Vdd < 2.7V		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- **3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.



TABLE 32-34: CAN MODULE I/O TIMING REQUIREMENTS

AC CHAR	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Min Typ ⁽²⁾ Max			Conditions
CA10	TioF	Port Output Fall Time	_	—	_	ns	See parameter DO32
CA11	TioR	Port Output Rise Time	_	—		ns	See parameter DO31
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	700	_		ns	_

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 32-36: ADC MODULE SPECIFICATIONS

		STICS	Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated)								
			Operating ter	mperature	$-40^{\circ}C \le TA \le -40^{\circ}C \le TA \le TA$	≤ +85°0 ≤ +105°	C for Industrial °C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions				
Device	Supply										
AD01	AVdd	Module VDD Supply	Greater of VDD – 0.3 or 2.5	_	Lesser of VDD + 0.3 or 3.6	V	_				
AD02	AVss	Module Vss Supply	Vss	—	Vss + 0.3	V	—				
Referen	nce Inputs										
AD05 AD05a	Vrefh	Reference Voltage High	AVss + 2.0 2.5		AVDD 3.6	V V	(Note 1) VREFH = AVDD (Note 3)				
AD06	Vrefl	Reference Voltage Low	AVss	—	Vrefh – 2.0	V	(Note 1)				
AD07	Vref	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVdd	V	(Note 3)				
AD08 AD08a	IREF	Current Drain	_	250 —	400 3	μΑ μΑ	ADC operating ADC off				
Analog	Input										
AD12	VINH-VINL	Full-Scale Input Span	VREFL		Vrefh	V	—				
AD13	VINL	Absolute Vın∟ Input Voltage	AVss – 0.3	—	AVdd/2	V	—				
AD14	Vin	Absolute Input Voltage	AVss - 0.3	—	AVDD + 0.3	V	—				
AD15		Leakage Current	_	±0.001	±0.610	μΑ	$\label{eq:VINL} \begin{array}{l} VINL = AVSS = VREFL = 0V,\\ AVDD = VREFH = 3.3V\\ Source \ Impedance = 10 \ k\Omega \end{array}$				
AD17	Rin	Recommended Impedance of Analog Voltage Source		—	5K	Ω	(Note 1)				
ADC Ac	curacy – N	leasurements with Exter	rnal VREF+/VF	REF-							
AD20c	Nr	Resolution	1	0 data bits	5	bits	—				
AD21c	INL	Integral Nonlinearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V				
AD22c	DNL	Differential Nonlinearity	> -1	_	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)				
AD23c	Gerr	Gain Error	> -1	_	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V				
AD24c	EOFF	Offset Error	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 3.3V				
AD25c		Monotonicity	—	_		_	Guaranteed				

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.