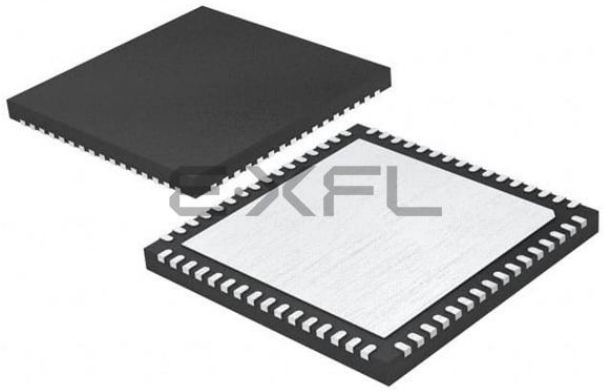

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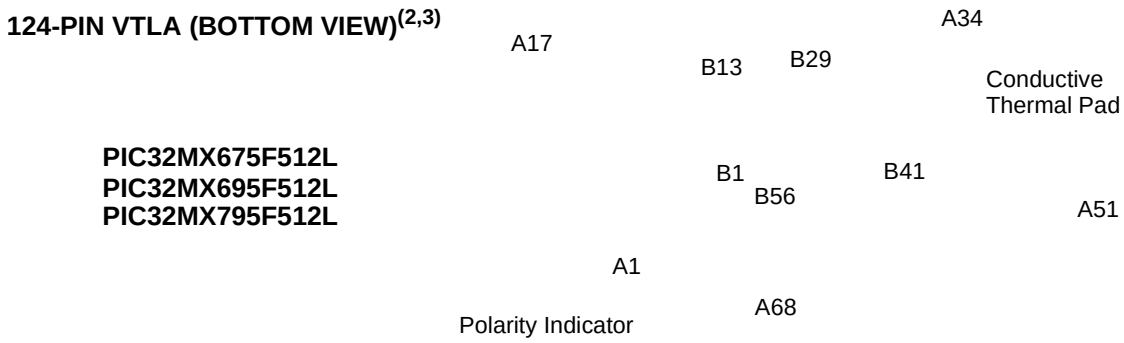
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx695f512ht-80v-mr

TABLE 13: PIN NAMES FOR 124-PIN USB, ETHERNET, AND CAN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)(2,3)



Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
B8	VSS	B33	TDO/RA5
B9	TMS/RA0	B34	OSC1/CLKI/RC12
B10	AERXD1/INT2/RE9	B35	No Connect (NC)
B11	AN4/C1IN-/CN6/RB4	B36	AETXCLK/SCL1/INT3/RA14
B12	VSS	B37	RTCC/EMDIO/AEMDIO/IC1/RD8
B13	AN2/C2IN-/CN4/RB2	B38	SCK1/IC3/PMCS2/PMA15/RD10
B14	PGED1/AN0/CN2/RB0	B39	SDO1/OC1/INT0/RD0
B15	No Connect (NC)	B40	SOSCO/T1CK/CN0/RC14
B16	PGED2/AN7/RB7	B41	VSS
B17	VREF+/CVREF+/AERXD3/PMA6/RA10	B42	OC3/RD2
B18	AVSS	B43	ETXD2/IC5/PMD12/RD12
B19	AN9/C2OUT/RB9	B44	OC5/PMWR/CN13/RD4
B20	AN11/ERXERR/AETXERR/PMA12/RB11	B45	ETXEN/PMD14/CN15/RD6
B21	VDD	B46	VSS
B22	AC1TX/SCK4/U5TX/U2RTS/RF13	B47	No Connect (NC)
B23	AN12/ERXD0/AECRS/PMA11/RB12	B48	VCAP
B24	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14	B49	C1RX(1)/ETXD1/PMD11/RF0
B25	VSS	B50	C2TX(1)/ETXERR/PMD9/RG1
B26	AETXD0/SS3/U4RX/U1CTS/CN20/RD14	B51	TRCLK/RA6
B27	SDA5/SDI4/U2RX/PMA9/CN17/RF4	B52	PMD0/RE0
B28	No Connect (NC)	B53	VDD
B29	SCL3/SDO3/U1TX/RF8	B54	TRD2/RG14
B30	VUSB3V3	B55	TRD0/RG13
B31	D+/RG2	B56	PMD3/RE3

Note 1: This pin is only available on PIC32MX795F512L devices.
2: Shaded package bumps are 5V tolerant.
3: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUS

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX5XX/6XX/7XX family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- VCAP pin (see **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **2.8 "External Oscillator Pins"**)

The following pin may be required, as well: VREF+/VREF- pins used when external voltage reference for ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of the ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDUPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDUPBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUPBA<15:10>:** DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** DRM User Program Base Address Read-Only bits

Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

TABLE 7-7: INTERRUPT REGISTER MAP FOR PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>		—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		—	—	—	U1IP<2:0>			U1IS<1:0>		0000
														SPI3IP<2:0>			SPI3IS<1:0>		
														I2C3IP<2:0>			I2C3IS<1:0>		
1100	IPC7	31:16	—	—	—	U3IP<2:0>			U3IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
						SPI2IP<2:0>			SPI2IS<1:0>										
						I2C4IP<2:0>			I2C4IS<1:0>										
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>		—	—	—	U2IP<2:0>			U2IS<1:0>		0000
														SPI4IP<2:0>			SPI4IS<1:0>		
														I2C5IP<2:0>			I2C5IS<1:0>		
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
1130	IPC10	31:16	—	—	—	DMA7IP<2:0>(2)			DMA7IS<1:0>(2)		—	—	—	DMA6IP<2:0>(2)			DMA6IS<1:0>(2)		0000
		15:0	—	—	—	DMA5IP<2:0>(2)			DMA5IS<1:0>(2)		—	—	—	DMA4IP<2:0>(2)			DMA4IS<1:0>(2)		0000
1140	IPC11	31:16	—	—	—	CAN2IP<2:0>(2)			CAN2IS<1:0>(2)		—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000
1150	IPC12	31:16	—	—	—	U5IP<2:0>			U5IS<1:0>		—	—	—	U6IP<2:0>			U6IS<1:0>		0000
		15:0	—	—	—	U4IP<2:0>			U4IS<1:0>		—	—	—	ETHIP<2:0>			ETHIS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This bit is unimplemented on PIC32MX764F128L device.

3: This register does not have associated CLR, SET, and INV registers.

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDL	TWDIS	TWIP	—	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Timer is enabled
- 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation when device is in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
- 1 = Writes to TMR1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:
- 1 = Asynchronous write to TMR1 register in progress
- 0 = Asynchronous write to TMR1 register complete

In Synchronous Timer mode:
This bit is read as '0'.

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

17.0 OUTPUT COMPARE

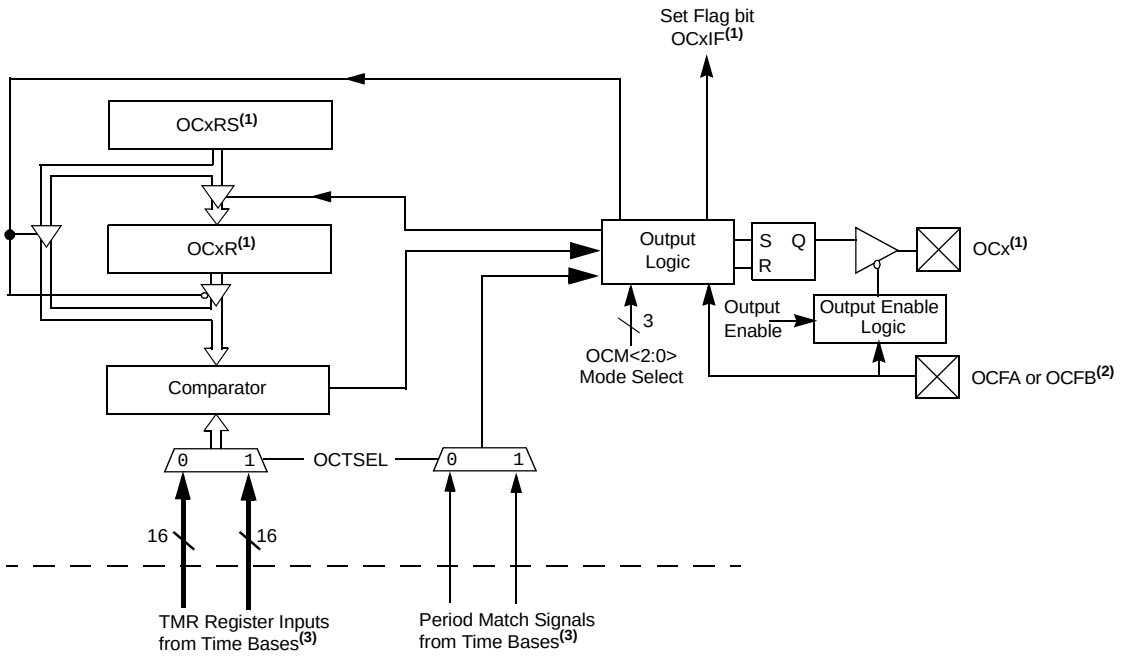
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Output Compare module is used to generate a single pulse or a series of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

FIGURE 17-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 5.

2: The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

3: Each output compare channel can use one of two selectable 16-bit time bases or a single 32-bit timer base.

19.1 Control Registers

TABLE 19-1: I2C1THROUGH I2C5 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	I2C3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5010	I2C3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5020	I2C3ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
5030	I2C3MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5040	I2C3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5050	I2C3TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
5060	I2C3RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000
5100	I2C4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5110	I2C4STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5120	I2C4ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
5130	I2C4MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5140	I2C4BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5150	I2C4TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
5160	I2C4RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000
5200	I2C5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5210	I2C5STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5220	I2C5ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This register is not available on 64-pin devices.

REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low (PMCS1)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master mode 2 (PMMODE<9:8> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low (PMWR)
For Master mode 1 (PMMODE<9:8> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low (PMENB)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (PMMODE<9:8> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low (PMRD)
For Master mode 1 (PMMODE<9:8> = 11):
1 = Read/write strobe active-high (PMRD/PMWR)
0 = Read/write strobe active-low (PMRD/PMWR)

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 21-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		—	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0>(1)		WAITM<3:0>(1)				WAITE<1:0>(1)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (only Master mode)
- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
- 11 = Reserved
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (only Addressable Slave mode)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = Interrupt is not generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
- 11 = Slave mode read and write buffers auto-increment (only PMMODE<1:0> = 00)
- 10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle(2)
- 01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle(2)
- 00 = No increment or decrement of address

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
- 11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)
- 10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)
- 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
- 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits(1)
- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)

bit 13 **SIDLE:** CAN Stop in Idle bit
1 = CAN Stops operation when system enters Idle mode
0 = CAN continues operation when system enters Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **CANBUSY:** CAN Module is Busy bit
1 = The CAN module is active
0 = The CAN module is completely disabled

bit 10-5 **Unimplemented:** Read as '0'

bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
•
•
•
00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 24-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5 (CONTINUED)

bit 15 **FLTEN21:** Filter 21 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL21<1:0>:** Filter 21 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL21<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN20:** Filter 20 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL20<1:0>:** Filter 20 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL20<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 25-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits

Increment count for frames that were successfully transmitted after there was more than one collision.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-39: EMAC1SA2: ETHERNET CONTROLLER MAC STATION ADDRESS 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR2<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR1<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Maintain as '0'; ignore read

bit 15-8 **STNADDR2<7:0>:** Station Address Octet 2 bits
These bits hold the second transmitted octet of the station address.

bit 7-0 **STNADDR1<7:0>:** Station Address Octet 1 bits
These bits hold the most significant (first transmitted) octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

26.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

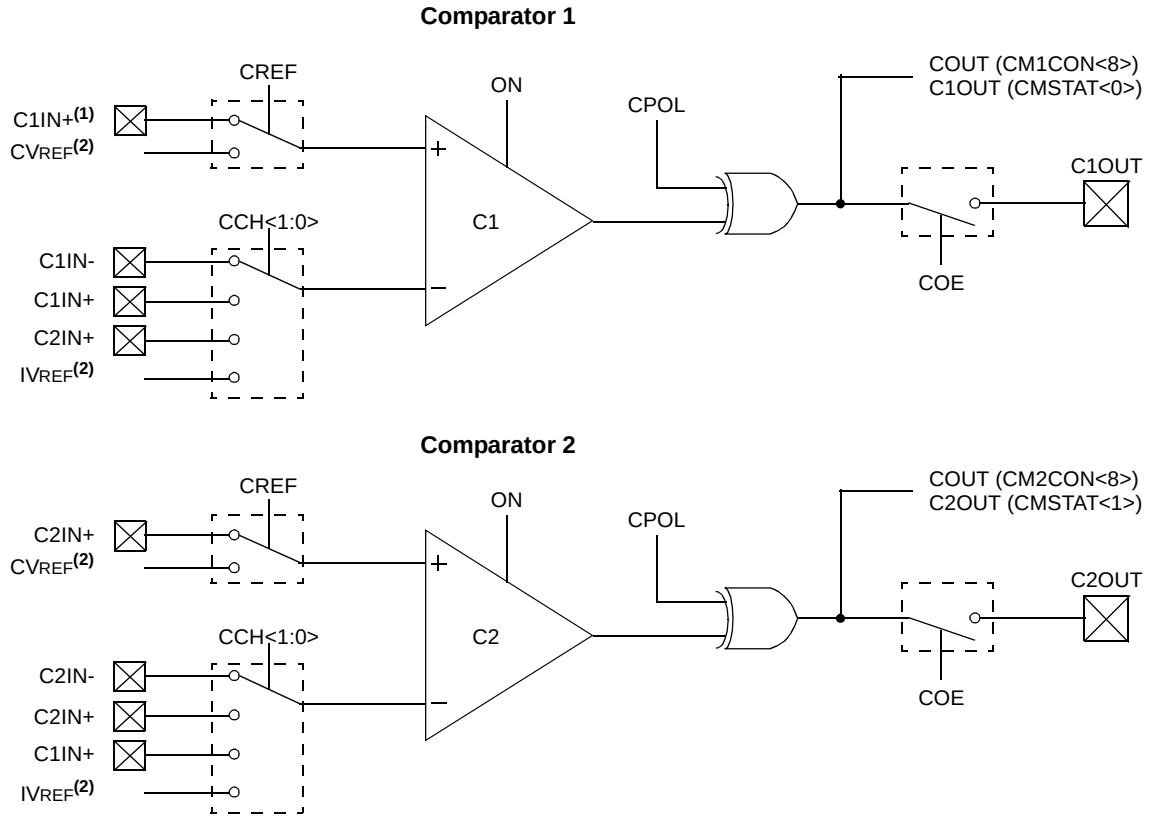
The Comparator module contains two comparators that can be configured in a variety of ways.

Key features of the Comparator module include:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the Comparator module is illustrated in Figure 26-1.

FIGURE 26-1: COMPARATOR MODULE BLOCK DIAGRAM



Note 1: On devices with a USB module, and when the module is enabled, this pin is controlled by the USB module, and therefore, is not available as a comparator input.

2: Internally connected. See **Section 27.0 "Comparator Voltage Reference (CVREF)"**.

TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Typical(3)**	**Max.**	**Units**	**Conditions**			
Operating Current (IDD)(1,2) for PIC32MX534/564/664/764 Family Devices							
DC20c	6	9	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	4 MHz
DC20d	7	10			+105ºC		
DC20e	2	—		Code executing from SRAM	—		
DC21b	19	32	mA	Code executing from Flash	—	—	25 MHz **(Note 4)**
DC21c	14	—		Code executing from SRAM			
DC22b	31	50	mA	Code executing from Flash	—	—	60 MHz **(Note 4)**
DC22c	29	—		Code executing from SRAM			
DC23c	39	65	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	80 MHz
DC23d	49	70			+105ºC		
DC23e	39	—		Code executing from SRAM	—		
DC25b	100	150	µA	—	+25°C	3.3V	LPRC (31 kHz) **(Note 4)**

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

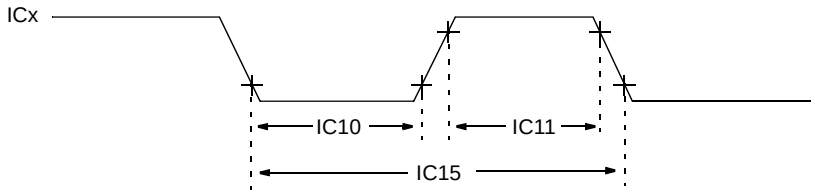
2: The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

FIGURE 32-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



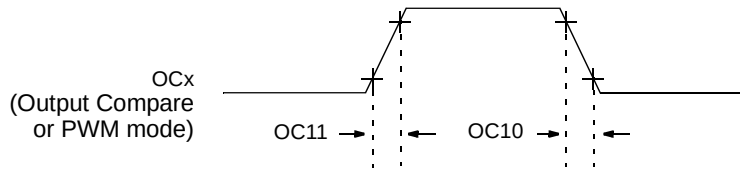
Note: Refer to Figure 32-1 for load conditions.

TABLE 32-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TccL	ICx Input Low Time	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	TccH	ICx Input High Time	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter IC15.	
IC15	TccP	ICx Input Period	[(25 ns or 2 TPB)/N] + 50 ns	—	ns	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 32-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

TABLE 32-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 32-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

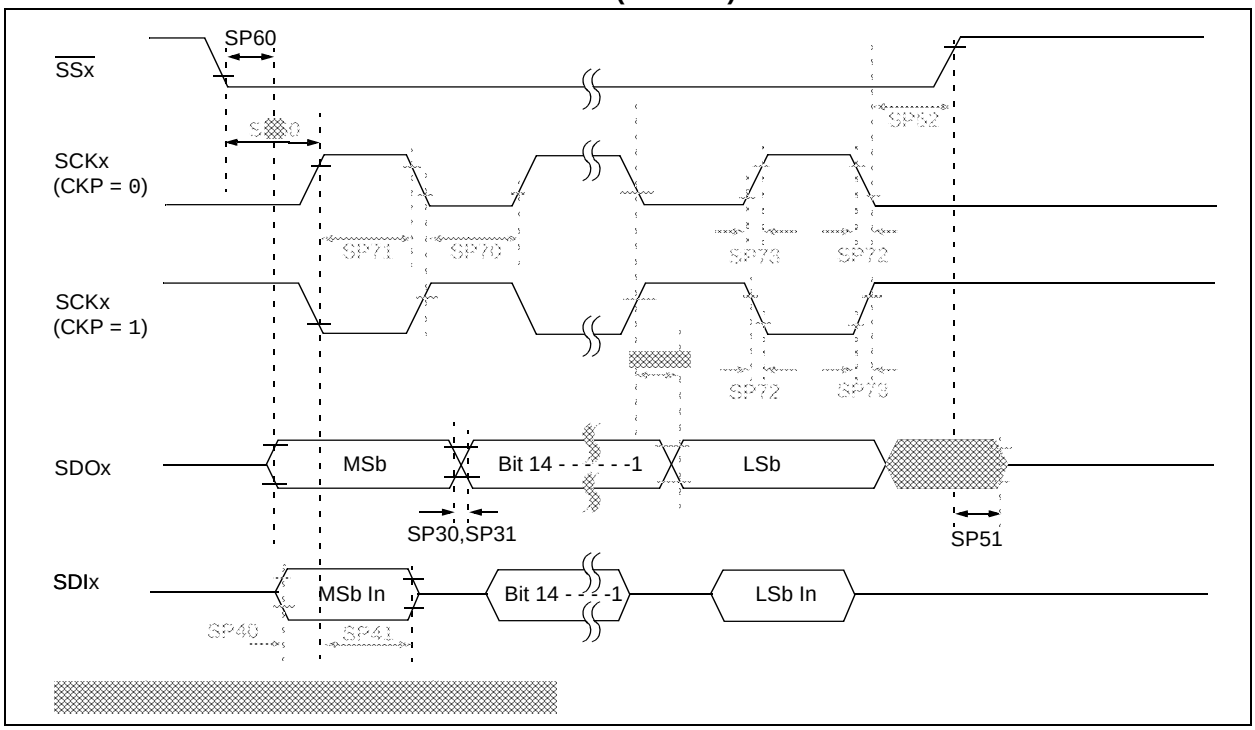


TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	5	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	5	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	20	ns	VDD > 2.7V
			—	—	30	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	175	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

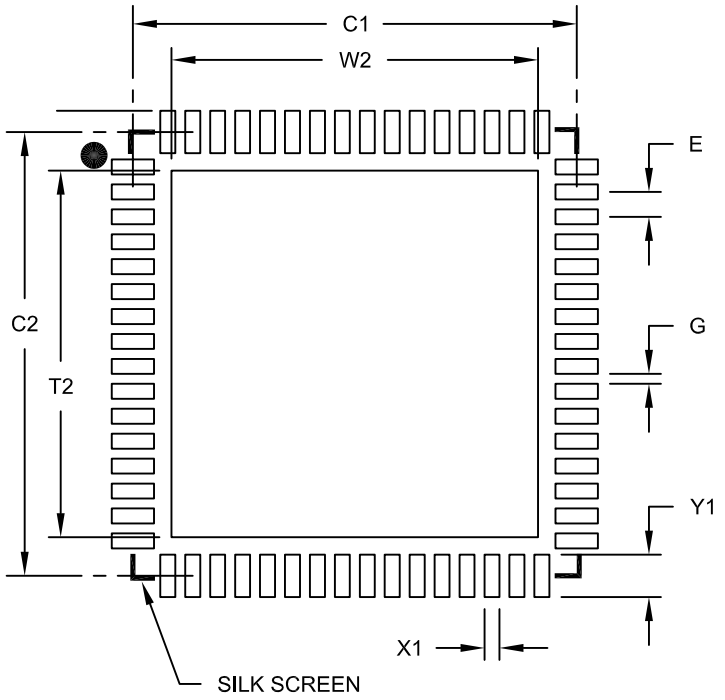
2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

Revision C (February 2010)

The revision includes the following updates, as described in Table B-2:

TABLE B-2: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"	Added the following devices: • PIC32MX675F256H • PIC32MX775F256H • PIC32MX775F512H • PIC32MX675F256L • PIC32MX775F256L • PIC32MX775F512L Added the following pins: • EREFCLK • ECRSDV • AEREFCLK • AECRSDV Added the EREFCLK and ECRSDV pins to Table 5 and Table 6.
1.0 "Device Overview"	Updated the pin number pinout I/O descriptions for the following pin names in Table 1-1: • SCL3 • SCL5 • RTCC • C1OUT • SDA3 • SDA5 • CVREF- • C2IN- • SCL2 • TMS • CVREF+ • C2IN+ • SDA2 • TCK • CVREFOUT • C2OUT • SCL4 • TDI • C1IN- • PMA0 • SDA4 • TDO • C1IN+ • PMA1 Added the following pins to the Pinout I/O Descriptions table (Table 1-1): • EREFCLK • ECRSDV • AEREFCLK • AECRSDV
4.0 "Memory Organization"	Added new devices and updated the virtual and physical memory map values in Figure 4-4. Added new devices to Figure 4-5. Added new devices to the following register maps: • Table 4-3, Table 4-4, Table 4-6 and Table 4-7 (Interrupt Register Maps) • Table 4-12 (I2C2 Register Map) • Table 4-15 (SPI1 Register Map) • Table 4-24 through Table 4-35 (PORTA-PORTG Register Maps) • Table 4-36 and Table 4-37 (Change Notice and Pull-up Register Maps) • Table 4-45 (CAN1 Register Map) • Table 4-46 (CAN2 Register Map) • Table 4-47 (Ethernet Controller Register Map) Changed the bits named POSCMD to POSCMOD in Table 4-42 (Device Configuration Word Summary).
1.0 "Special Features"	Changed all references of POSCMD to POSCMOD in the Device Configuration Word 1 register (see Register 1-2).
Appendix A: "Migrating from PIC32MX3XX/4XX to PIC32MX5XX/6XX/7XX Devices"	Added the new section Appendix .

TABLE B-7: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
32.0 “Electrical Characteristics”	Note 4 in the Operating Current specification was updated (see Table 32-5). Note 3 in the Idle Current specification was updated (see Table 32-6). Note 6 references in the Power-Down Current specification were updated (see Table 32-7). The Program Memory parameters, D135, D136, and D137, and Note 4 were updated (see Table 32-11). The Voltage Reference Specifications were updated (see Table 32-14). Parameter DO50 (Cosco) was added to the Capacitive Loading Requirements on Output Pins (see Table 32-16). The EJTAG Timing Characteristics were updated (see Figure 32-28). The maximum value for parameters ET13 and ET14 were updated in the Ethernet Module Specifications (see Table 32-35). Parameter PM7 (TDHOLD) was updated (see Table 32-40).
34.0 “Packaging Information”	Packaging diagrams were updated.
Product Identification System	The Speed and Program Memory Size were updated and Note 1 was added.