Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx695f512l-80i-tl

TABLE 9: PIN NAMES FOR 100-PIN USB, ETHERNET, AND CAN DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MX764F128L
PIC32MX775F256L
PIC32MX775F512L
PIC32MX795F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AERXERR/RG15	36	VSS
2	VDD	37	VDD
3	PMD5/RE5	38	TCK/RA1
4	PMD6/RE6	39	AC1TX/SCK4/U5TX/U2RTS/RF13
5	PMD7/RE7	40	AC1RX/SS4/U5RX/U2CTS/RF12
6	T2CK/RC1	41	AN12/ERXD0/AECRS/PMA11/RB12
7	T3CK/AC2TX(1)/RC2	42	AN13/ERXD1/AECOL/PMA10/RB13
8	T4CK/AC2RX(1)/RC3	43	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14
9	T5CK/SDI1/RC4	44	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
10	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6	45	VSS
11	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7	46	VDD
12	ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8	47	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
13	MCLR	48	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
14	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9	49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
15	VSS	50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
16	VDD	51	USBID/RF3
17	TMS/RA0	52	SDA3/SDI3/U1RX/RF2
18	AERXD0/INT1/RE8	53	SCL3/SDO3/U1TX/RF8
19	AERXD1/INT2/RE9	54	VBUS
20	AN5/C1IN+/VBUSON/CN7/RB5	55	VUSB3V3
21	AN4/C1IN-/CN6/RB4	56	D-/RG3
22	AN3/C2IN+/CN5/RB3	57	D+/RG2
23	AN2/C2IN-/CN4/RB2	58	SCL2/RA2
24	PGEC1/AN1/CN3/RB1	59	SDA2/RA3
25	PGED1/AN0/CN2/RB0	60	TDI/RA4
26	PGEC2/AN6/OCFA/RB6	61	TDO/RA5
27	PGED2/AN7/RB7	62	VDD
28	VREF-/CVREF-/AERXD2/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/AERXD3/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	AETXCLK/SCL1/INT3/RA14
32	AN8/C1OUT/RB8	67	AETXEN/SDA1/INT4/RA15
33	AN9/C2OUT/RB9	68	RTCC/EMDIO/AEMDIO/IC1/RD8
34	AN10/CVREFOUT/PMA13/RB10	69	SS1/IC2/RD9
35	AN11/ERXERR/AETXERR/PMA12/RB11	70	SCK1/IC3/PMCS2/PMA15/RD10

Note 1: This pin is not available on PIC32MX764F128L devices.
2: Shaded pins are 5V tolerant.

1.0 DEVICE OVERVIEW

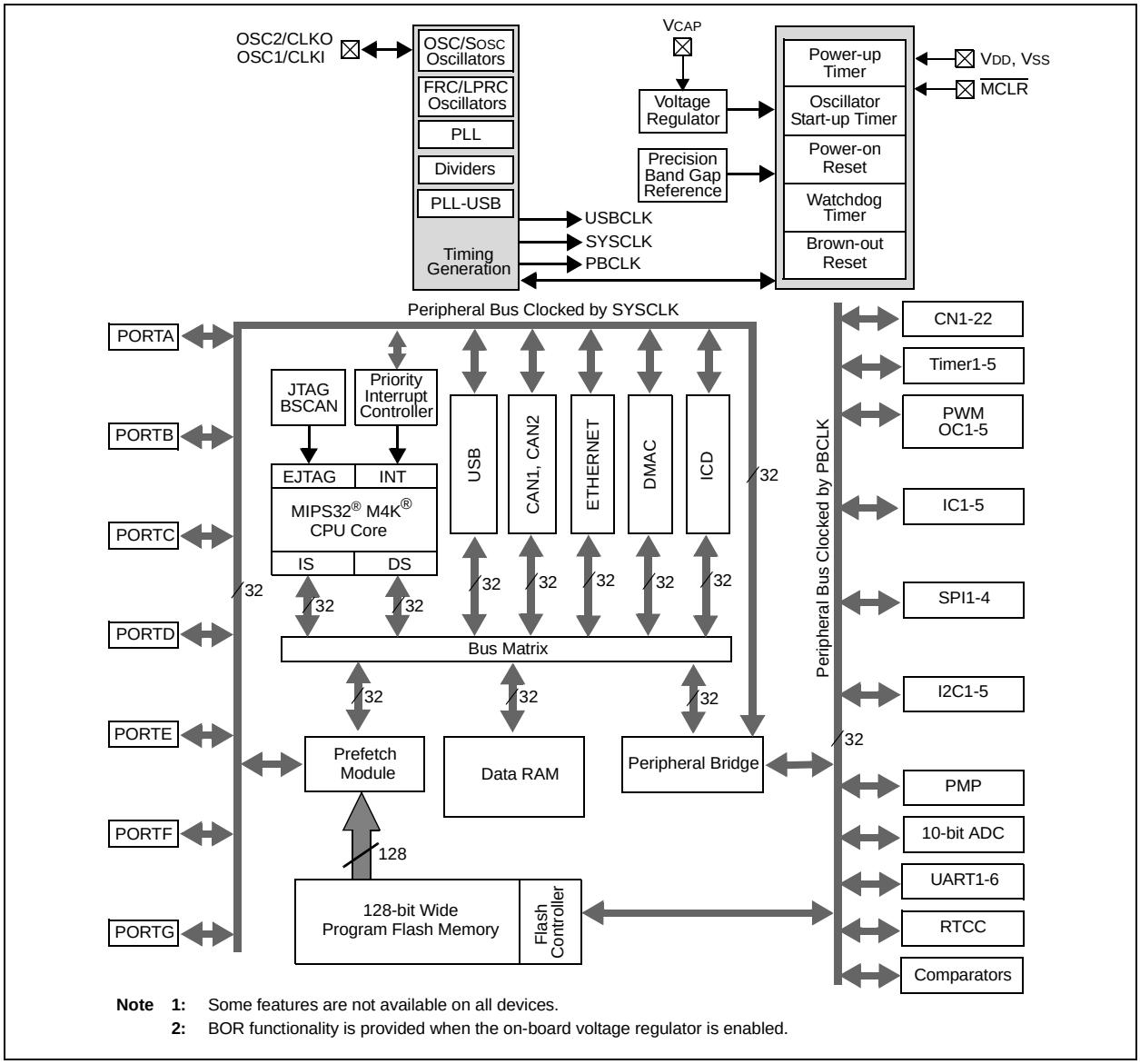
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX5XX/6XX/7XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX5XX/6XX/7XX family of devices.

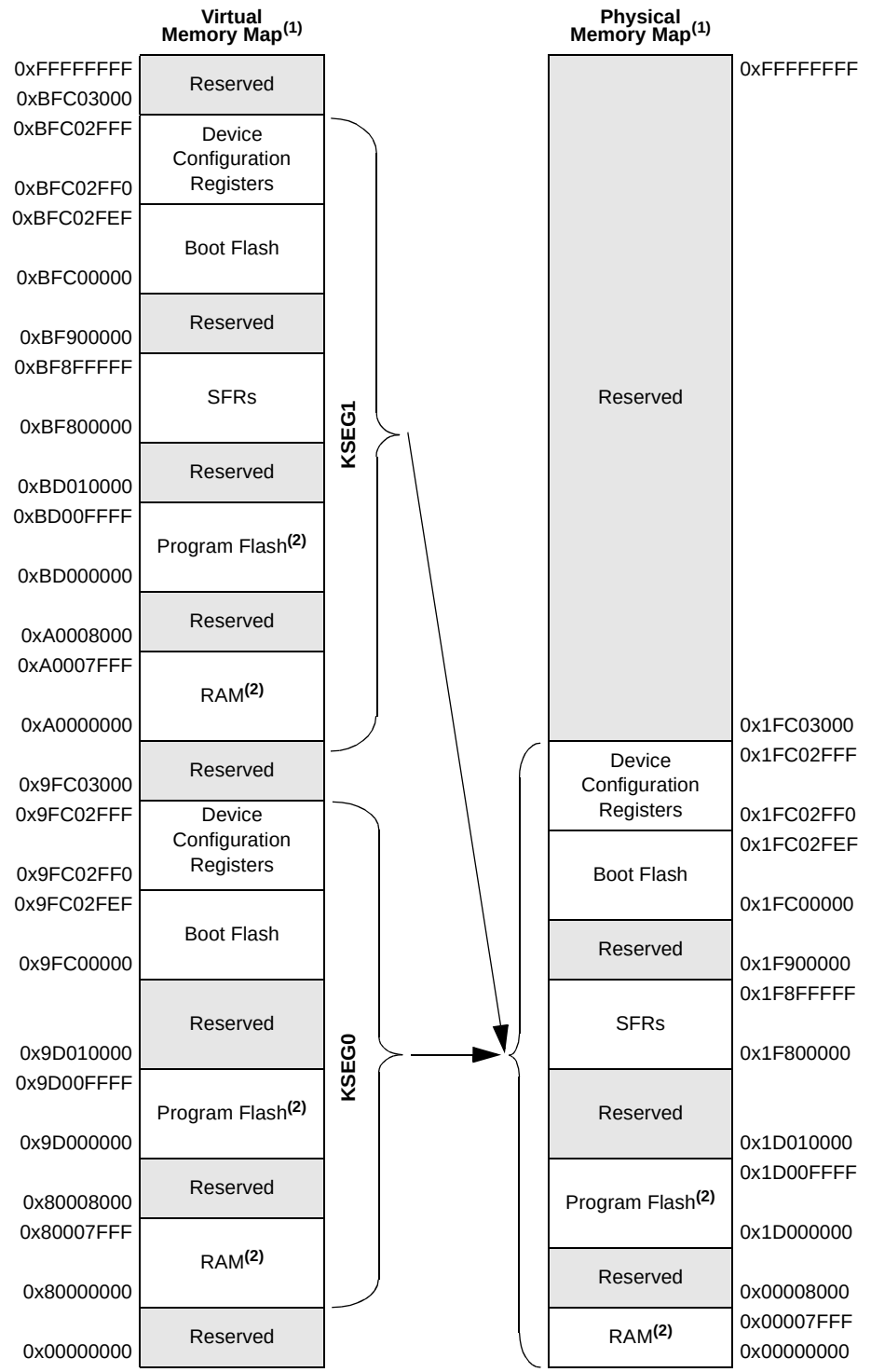
Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM(1,2)



Note 1: Some features are not available on all devices.
2: BOR functionality is provided when the on-board voltage regulator is enabled.

FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX564F064H, PIC32MX564F064L, PIC32MX664F064H AND PIC32MX664F064L DEVICES



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXDRMSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXDRMSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXDRMSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXDRMSZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXDRMSZ<31:0>:** Data RAM Memory (DRM) Size bits
Static value that indicates the size of the Data RAM in bytes:
0x00004000 = device has 16 KB RAM
0x00008000 = device has 32 KB RAM
0x00010000 = device has 64 KB RAM

REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER(1,2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	BMXPUPBA<19:16>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
	BMXPUPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXPUPBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-11 **BMXPUPBA<19:11>:** Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>:** Program Flash (PFM) User Program Base Address Read-Only bits
Value is always '0', which forces 2 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXPFMSZ.

REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXPFMSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXPFMSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXPFMSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXPFMSZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXPFMSZ<31:0>:** Program Flash Memory (PFM) Size bits
Static value that indicates the size of the PFM in bytes:
0x00010000 = device has 64 KB Flash
0x00020000 = device has 128 KB Flash
0x00040000 = device has 256 KB Flash
0x00080000 = device has 512 KB Flash

REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXBOOTSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXBOOTSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXBOOTSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXBOOTSZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits
Static value that indicates the size of the Boot PFM in bytes:
0x00003000 = device has 12 KB boot Flash

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS09	IFS08
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS07	IFS06	IFS05	IFS04	IFS03	IFS02	IFS01	IFS00

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS31-IFS00:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC09	IEC08
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC07	IEC06	IEC05	IEC04	IEC03	IEC02	IEC01	IEC00

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC31-IEC00:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 11-5: U1PWRC: USB POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit

1 = USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit

1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit

1 = USB module is active or disabled, but not ready to be enabled
0 = USB module is not active and is ready to be enabled

Note: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit

1 = USB module is placed in Suspend mode
(The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit

1 = USB module is turned on
0 = USB module is disabled
(Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

REGISTER 11-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit
1 = Next token command to be executed at low-speed
0 = Next token command to be executed at full-speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 11-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

12.1 Parallel I/O (PIO) Ports

All port pins have three registers (TRIS, LAT and PORT) that are directly associated with their operation.

TRIS is a Data Direction or Tri-State Control register that determines whether a digital pin is an input or an output. Setting a TRISx register bit = 1, configures the corresponding I/O pin as an input; setting a TRISx register bit = 0, configures the corresponding I/O pin as an output. All port I/O pins are defined as inputs after a device Reset. Certain I/O pins are shared with analog peripherals and default to analog inputs after a device Reset.

PORT is a register used to read the current state of the signal applied to the port I/O pins. Writing to a PORTx register performs a write to the port's latch, LATx register, latching the data to the port's I/O pins.

LAT is a register used to write data to the port I/O pins. The LATx Latch register holds the data written to either the LATx or PORTx registers. Reading the LATx Latch register reads the last value written to the corresponding PORT or Latch register.

Not all port I/O pins are implemented on some devices, therefore, the corresponding PORTx, LATx and TRISx register bits will read as zeros.

12.1.1 CLR, SET AND INV REGISTERS

Every I/O module register has a corresponding Clear (CLR), Set (SET) and Invert (INV) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

Note:	Using a PORTxINV register to toggle a bit is recommended because the operation is performed in hardware atomically, using fewer instructions, as compared to the traditional read-modify-write method, as follows: `PORTC ^ = 0x0001;`

12.1.2 DIGITAL INPUTS

Pins are configured as digital inputs by setting the corresponding TRIS register bits = 1. When configured as inputs, they are either TTL buffers or Schmitt Triggers. Several digital pins share functionality with analog inputs and default to the analog inputs at POR. Setting the corresponding bit in the AD1PCFG register = 1 enables the pin as a digital pin.

The maximum input voltage allowed on the input pins is the same as the maximum V_{IH} specification. Refer to **Section 32.0 "Electrical Characteristics"** for V_{IH} specification details.

Note:	Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

12.1.3 ANALOG INPUTS

Certain pins can be configured as analog inputs used by the ADC and comparator modules. Setting the corresponding bits in the AD1PCFG register = 0 enables the pin as an analog input pin and must have the corresponding TRIS bit set = 1 (input). If the TRIS bit is cleared = 0 (output), the digital output level (V_{OH} or V_{OL}) will be converted. Any time a port I/O pin is configured as analog, its digital input is disabled and the corresponding PORTx register bit will read '0'. The AD1PCFG register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

12.1.4 DIGITAL OUTPUTS

Pins are configured as digital outputs by setting the corresponding TRIS register bits = 0. When configured as digital outputs, these pins are CMOS drivers or can be configured as open-drain outputs by setting the corresponding bits in the Open-Drain Configuration (ODCx) register.

The open-drain feature allows generation of outputs higher than V_{DD} (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

See the **"Device Pin Tables"** section for the available pins and their functionality.

12.1.5 ANALOG OUTPUTS

Certain pins can be configured as analog outputs, such as the CV_{REF} output voltage used by the comparator module. Configuring the comparator reference module to provide this output will present the analog output voltage on the pin, independent of the TRIS register setting for the corresponding pin.

12.1.6 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports (CNx) allows devices to generate interrupt requests in response to change-of-state on selected pin.

Each CNx pin also has a weak pull-up, which acts as a current source connected to the pin. The pull-ups are enabled by setting the corresponding bit in the CNPUE register.

16.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

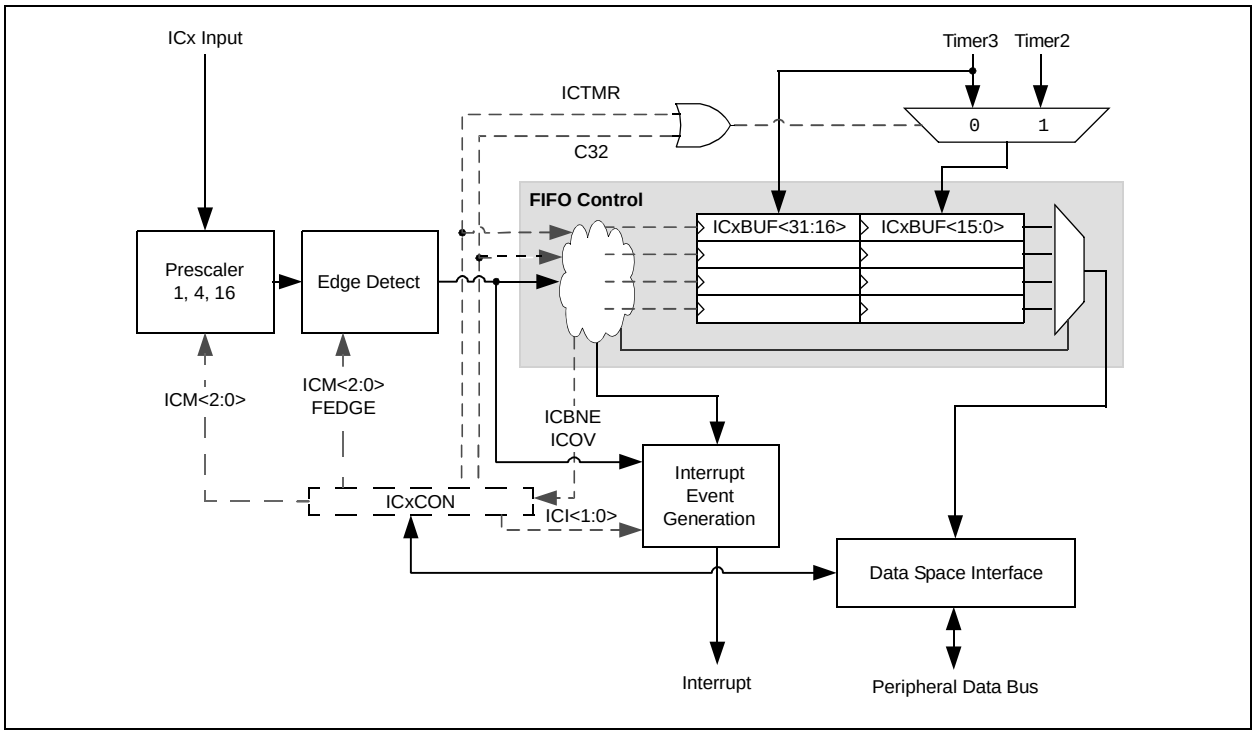
- Simple capture event modes:
  - Capture timer value on every falling edge of input at ICx pin
  - Capture timer value on every rising edge of input at ICx pin
- Capture timer value on every edge (rising and falling)
- Capture timer value on every edge (rising and falling), specified edge first.
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
  Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input Capture module can also be used to provide additional sources of external interrupts

FIGURE 16-1: INPUT CAPTURE BLOCK DIAGRAM



REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON(1)	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit(1)
- 1 = Module is enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in Idle mode
- 0 = Continue to operate in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
- 1 = Timer2 is the counter source for capture
- 0 = Timer3 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow is occurred
- 0 = No input capture overflow is occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Note 1: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 24-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4 (CONTINUED)

bit 15 **FLTEN17:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL17<1:0>:** Filter 17 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL17<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN16:** Filter 16 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL16<1:0>:** Filter 16 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL16<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 24-18: CiRXFn: CAN ACCEPTANCE FILTER 'n' REGISTER 7 (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SID<10:3>							
23:16	R/W-x	R/W-x	R/W-x	U-0	R/W-0	U-0	R/W-x	R/W-x
	SID<2:0>			—	EXID	—	EID<17:16>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Message address bit SIDx must be '1' to match filter
0 = Message address bit SIDx must be '0' to match filter

bit 20 **Unimplemented:** Read as '0'

bit 19 **EXID:** Extended Identifier Enable bits
1 = Match only messages with extended identifier addresses
0 = Match only messages with standard identifier addresses

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Message address bit EIDx must be '1' to match filter
0 = Message address bit EIDx must be '0' to match filter

Note: This register can only be modified when the filter is disabled (FLTENn = 0).

26.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

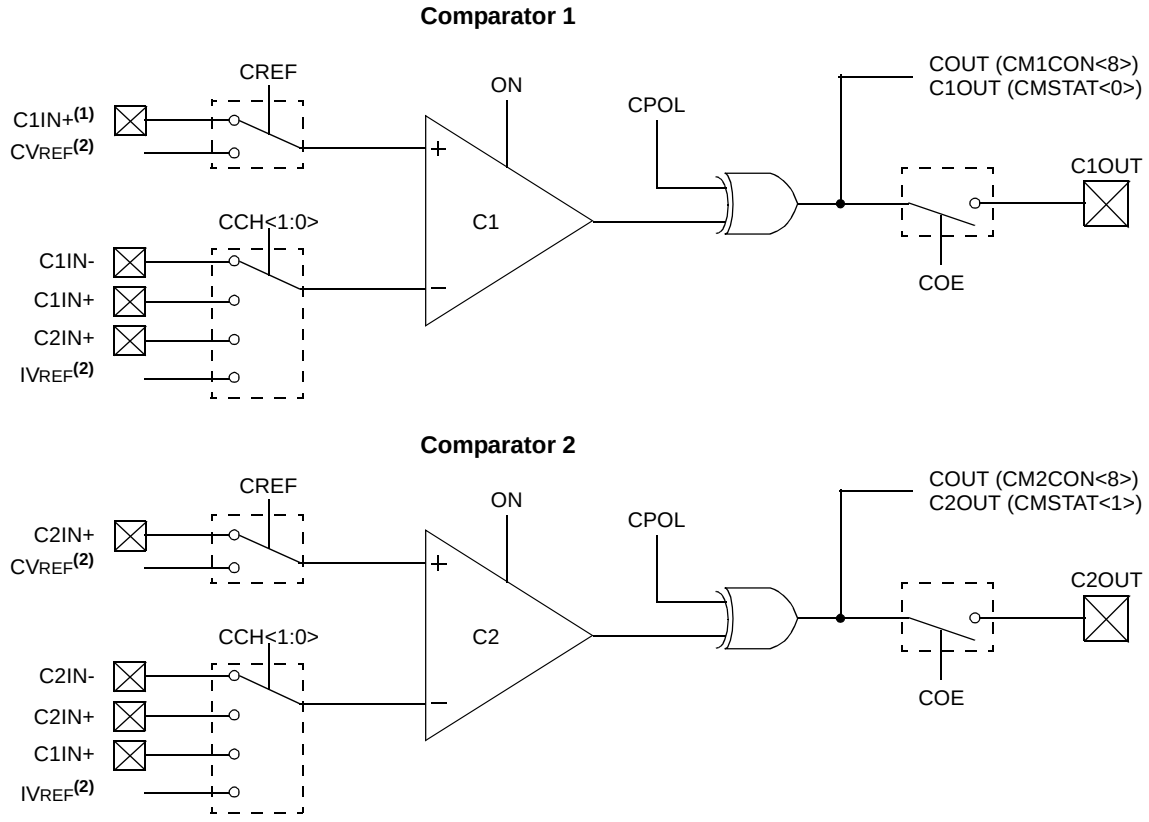
The Comparator module contains two comparators that can be configured in a variety of ways.

Key features of the Comparator module include:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the Comparator module is illustrated in Figure 26-1.

FIGURE 26-1: COMPARATOR MODULE BLOCK DIAGRAM



Note 1: On devices with a USB module, and when the module is enabled, this pin is controlled by the USB module, and therefore, is not available as a comparator input.

2: Internally connected. See **Section 27.0 "Comparator Voltage Reference (CVREF)"**.

REGISTER 29-5: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0>(1)				DEVID<27:24>(1)			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16>(1)							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8>(1)							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID bits(1)

Note 1: See the *"PIC32 Flash Programming Specification"* (DS60001145) for a list of Revision and Device ID values.

REGISTER 29-6: DDPCON: DEBUG DATA PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	U-0	R/W-0
	—	—	—	—	JTAGEN	TROEN	—	TDOEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Port Enable bit
- 1 = Enable the JTAG port
- 0 = Disable the JTAG port

bit 2 **TROEN:** Trace Output Enable bit
- 1 = Enable the trace port
- 0 = Disable the trace port

bit 1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG
- 1 = 2-wire JTAG protocol uses TDO
- 0 = 2-wire JTAG protocol does not use TDO

32.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX5XX/6XX/7XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX5XX/6XX/7XX devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ..... -40°C to +105°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +5.5V
Maximum current out of V_{SS} pin(s) ..... 300 mA
Maximum current into V_{DD} pin(s) **(Note 2)** ..... 300 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports **(Note 2)** ..... 200 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

3: See the **"Device Pin Tables"** section for the 5V tolerant pins.

FIGURE 32-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

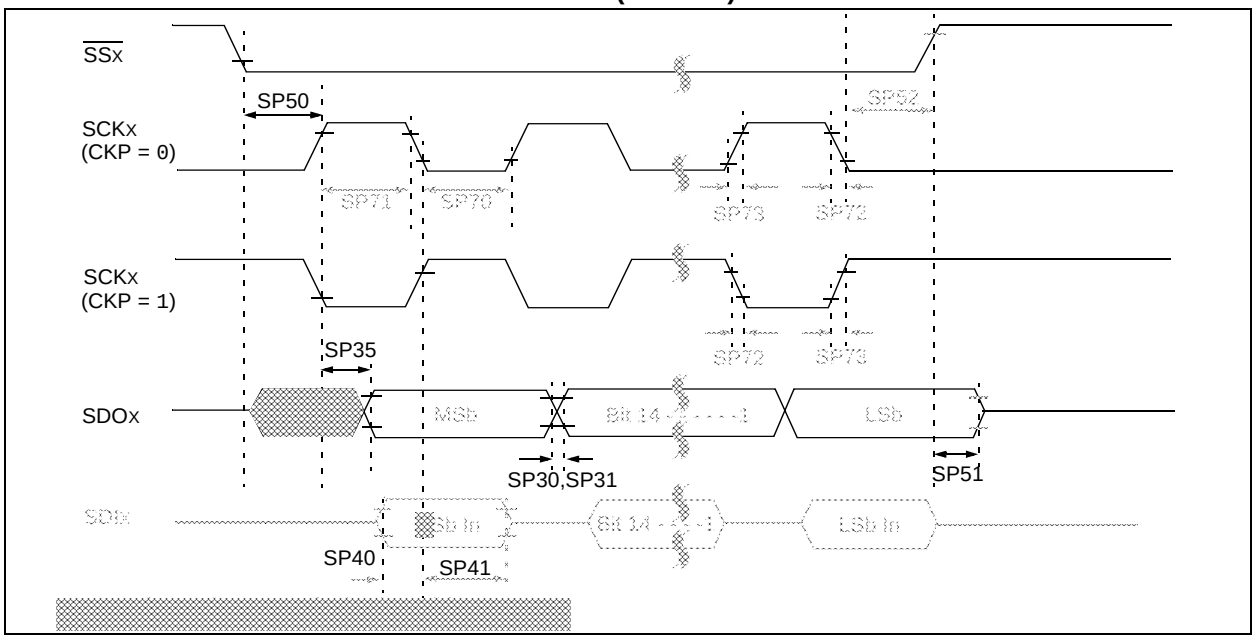


TABLE 32-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	175	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(3)	5	—	25	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	Tsck + 20	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 32-21: TRANSMIT SIGNAL TIMING RELATIONSHIPS AT THE MII

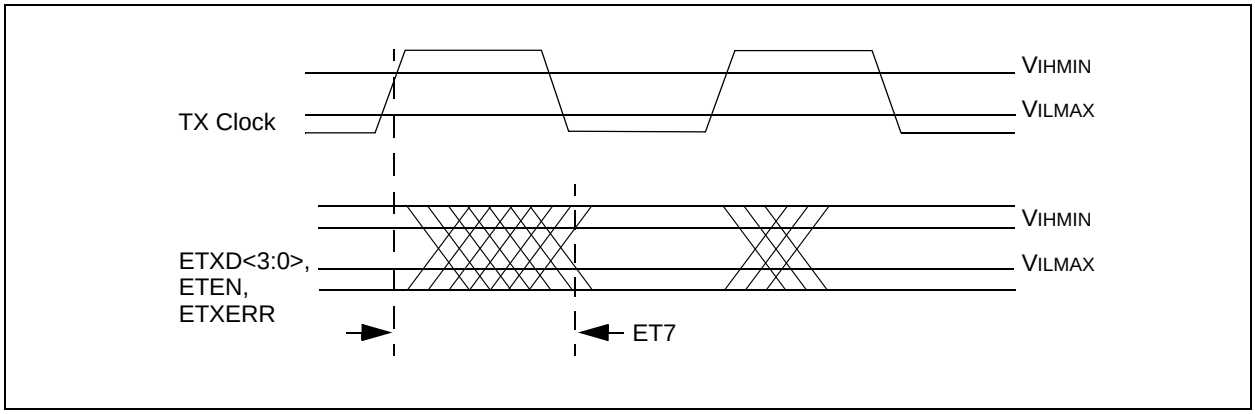


FIGURE 32-22: RECEIVE SIGNAL TIMING RELATIONSHIPS AT THE MII

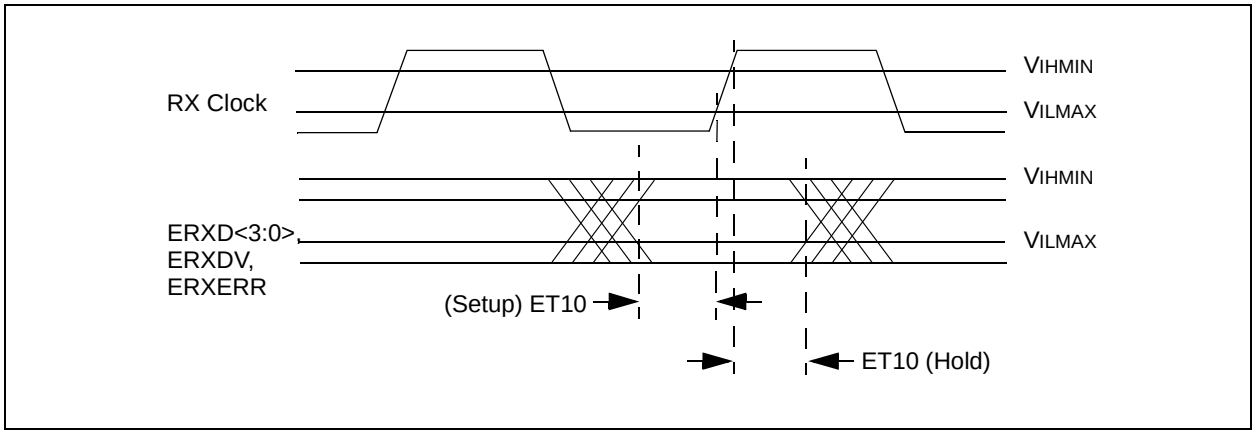
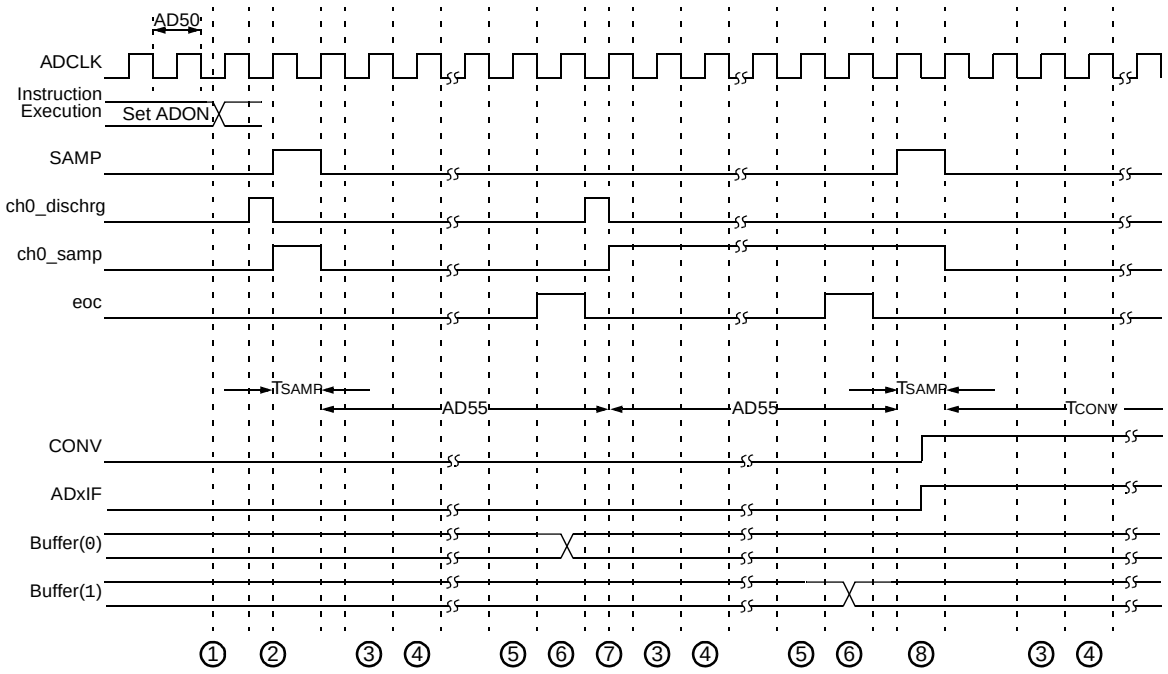


FIGURE 32-24: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)



(1) – Software sets ADxCON. ADON to start AD operation.

(2) – Sampling starts after discharge period.
TSAMP is described in Section 17. “10-bit A/D Converter” (DS60001104) of the *“PIC32 Family Reference Manual*.

(3) – Convert bit 9.

(4) – Convert bit 8.

(5) – Convert bit 0.

(6) – One TAD for end of conversion.

(7) – Begin conversion of next channel.

(8) – Sample for time specified by SAMC<4:0>.