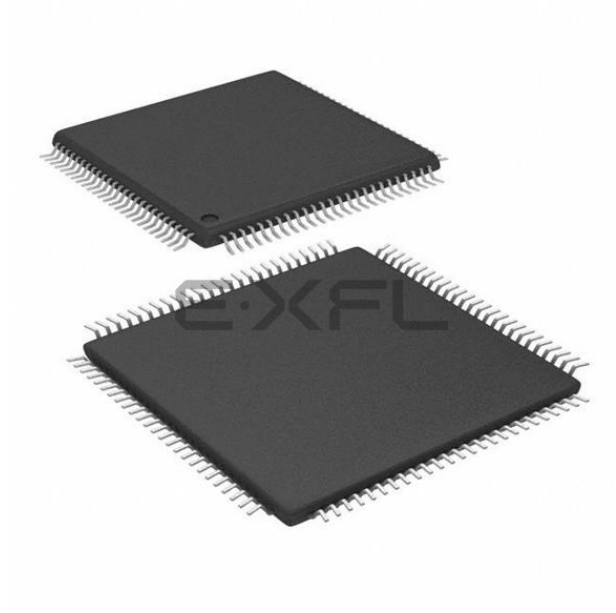
# Microchip Technology - PIC32MX695F512LT-80I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | Ethernet, I²C, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx695f512lt-80i-pt |

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| TMS | 23 | 17 | G3 | B9 | I | ST | JTAG Test mode select pin |
| TCK | 27 | 38 | J6 | A26 | I | ST | JTAG test clock input pin |
| TDI | 28 | 60 | G11 | A40 | I | ST | JTAG test data input pin |
| TDO | 24 | 61 | G9 | B33 | O | — | JTAG test data output pin |
| RTCC | 42 | 68 | E9 | B37 | O | — | Real-Time Clock alarm output |
| CVREF- | 15 | 28 | L2 | A21 | I | Analog | Comparator Voltage Reference (low) |
| CVREF+ | 16 | 29 | K3 | B17 | I | Analog | Comparator Voltage Reference (high) |
| CVREFOUT | 23 | 34 | L5 | A24 | O | Analog | Comparator Voltage Reference output |
| C1IN- | 12 | 21 | H2 | B11 | I | Analog | Comparator 1 negative input |
| C1IN+ | 11 | 20 | H1 | A12 | I | Analog | Comparator 1 positive input |
| C1OUT | 21 | 32 | K4 | A23 | O | — | Comparator 1 output |
| C2IN- | 14 | 23 | J2 | B13 | I | Analog | Comparator 2 negative input |
| C2IN+ | 13 | 22 | J1 | A13 | I | Analog | Comparator 2 positive input |
| C2OUT | 22 | 33 | L4 | B19 | O | — | Comparator 2 output |
| PMA0 | 30 | 44 | L8 | A29 | I/O | TTL/ST | Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes) |
| PMA1 | 29 | 43 | K7 | B24 | I/O | TTL/ST | Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes) |
| PMA2 | 8 | 14 | F3 | A9 | O | — | Parallel Master Port address (Demultiplexed Master modes) |
| PMA3 | 6 | 12 | F2 | A8 | O | — | |
| PMA4 | 5 | 11 | F4 | B6 | O | — | |
| PMA5 | 4 | 10 | E3 | A7 | O | — | |
| PMA6 | 16 | 29 | K3 | B17 | O | — | |
| PMA7 | 22 | 28 | L2 | A21 | O | — | |
| PMA8 | 32 | 50 | L11 | A32 | O | — | |
| PMA9 | 31 | 49 | L10 | B27 | O | — | |
| PMA10 | 28 | 42 | L7 | A28 | O | — | |
| PMA11 | 27 | 41 | J7 | B23 | O | — | |
| PMA12 | 24 | 35 | J5 | B20 | O | — | |
| PMA13 | 23 | 34 | L5 | A24 | O | — | |
| PMA14 | 45 | 71 | C11 | A46 | O | — | |
| PMA15 | 44 | 70 | D11 | B38 | O | — | |
| PMCS1 | 45 | 71 | C11 | A46 | O | — | Parallel Master Port Chip Select 1 strobe |
| PMCS2 | 44 | 70 | D11 | B38 | O | — | Parallel Master Port Chip Select 2 strobe |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.

# 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUS

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

## 2.1 Basic Connection Requirements

Getting started with the PIC32MX5XX/6XX/7XX family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- VCAP pin (see **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **2.8 "External Oscillator Pins"**)

The following pin may be required, as well: VREF+/VREF- pins used when external voltage reference for ADC module is implemented.

**Note:** The AVDD and AVSS pins must be connected, regardless of the ADC use and the ADC voltage reference source.

## 2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

**TABLE 7-6: INTERRUPT REGISTER MAP FOR PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L AND PIC32MX695F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF<br>SPI3TXIF<br>I2C3MIF | U1RXIF<br>SPI3RXIF<br>I2C3SIF | U1EIF<br>SPI3EIF<br>I2C3BIF | SPI1TXIF | SPI1RXIF | SPI1EIF | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | IC3EIF | IC2EIF | IC1EIF | ETHIF | — | — | USBIF | FCEIF | DMA7IF(2) | DMA6IF(2) | DMA5IF(2) | DMA4IF(2) | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | I2C2MIF | I2C2SIF | I2C2BIF | U2TXIF<br>SPI4TXIF<br>I2C5MIF | U2RXIF<br>SPI4RXIF<br>I2C5SIF | U2EIF<br>SPI4EIF<br>I2C5BIF | U3TXIF<br>SPI2TXIF<br>I2C4MIF | U3RXIF<br>SPI2RXIF<br>I2C4SIF | U3EIF<br>SPI2EIF<br>I2C4BIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIF | U5RXIF | U5EIF | U6TXIF | U6RXIF | U6EIF | U4TXIF | U4RXIF | U4EIF | PMPEIF | IC5EIF | IC4EIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE<br>SPI3TXIE<br>I2C3MIE | U1RXIE<br>SPI3RXIE<br>I2C3SIE | U1EIE<br>SPI3EIE<br>I2C3BIE | SPI1TXIE | SPI1RXIE | SPI1EIE | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | IC3EIE | IC2EIE | IC1EIE | ETHIE | — | — | USBIE | FCEIE | DMA7IE(2) | DMA6IE(2) | DMA5IE(2) | DMA4IE(2) | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | I2C2MIE | I2C2SIE | I2C2BIE | U2TXIE<br>SPI4TXIE<br>I2C5MIE | U2RXIE<br>SPI4RXIE<br>I2C5SIE | U2EIE<br>SPI4EIE<br>I2C5BIE | U3TXIE<br>SPI2TXIE<br>I2C4MIE | U3RXIE<br>SPI2RXIE<br>I2C4SIE | U3EIE<br>SPI2EIE<br>I2C4BIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIE | U5RXIE | U5EIE | U6TXIE | U6RXIE | U6EIE | U4TXIE | U4RXIE | U4EIE | PMPEIE | IC5EIE | IC4EIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX664 devices.

**3:** This register does note have associated CLR, SET, and INV registers.

## 8.0 OSCILLATOR CONFIGURATION

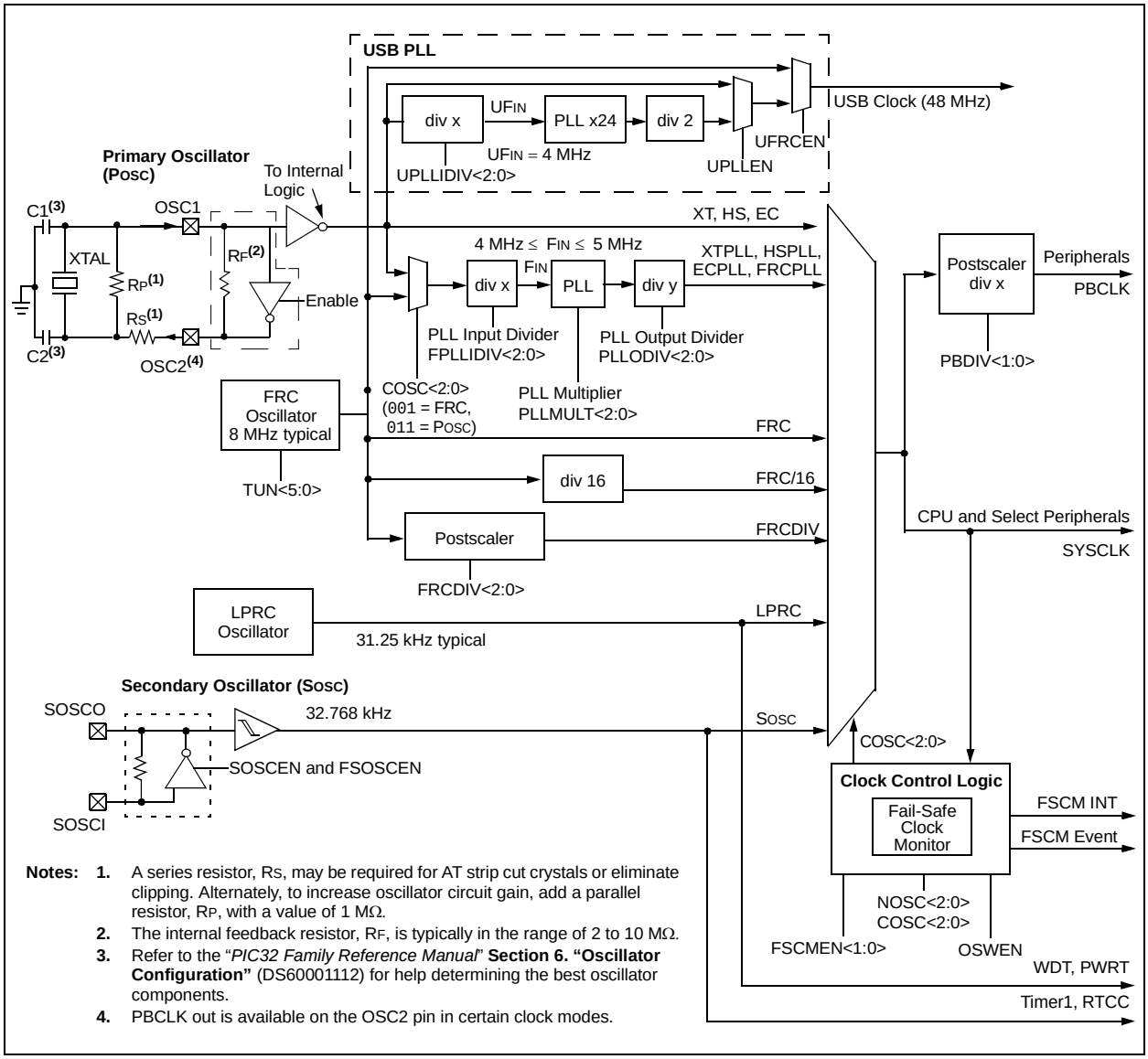
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Oscillator module has the following features:

- A total of four external and internal oscillator options as clock sources
- On-chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

Figure 8-1shows the Oscillator module block diagram.

**FIGURE 8-1: OSCILLATOR BLOCK DIAGRAM**




**Notes:**
1. A series resistor, RS, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP, with a value of 1 MΩ.
2. The internal feedback resistor, RF, is typically in the range of 2 to 10 MΩ.
3. Refer to the "*PIC32 Family Reference Manual*" **Section 6. "Oscillator Configuration"** (DS60001112) for help determining the best oscillator components.
4. PBCLK out is available on the OSC2 pin in certain clock modes.

## 8.1 Control Registers

**TABLE 8-1: OSCILLATOR REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F000 | OSCCON | 31:16 | — | — | PLLODIV<2:0> | | | FRCDIV<2:0> | | | — | SOSCRDY | — | PBDIV<1:0> | | PLLMULT<2:0> | | | 0000 |
| | | 15:0 | — | COSC<2:0> | | | — | NOSC<2:0> | | | CLKLOCK | ULOCK | SLOCK | SLPEN | CF | UFRCEN | SOSCEN | OSWEN | 0000 |
| F010 | OSCTUN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

**REGISTER 9-4: CHEMSK: CACHE TAG MASK REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | LMASK<10:3> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | LMASK<2:0> | | | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Write '0'; ignore read

bit 15-5 **LMASK<10:0>:** Line Mask bits

1 = Enables mask logic to force a match on the corresponding bit position in LTAG<19:0> bits (CHETAG<23:4>) and the physical address

0 = Only writeable for values of CHEIDX<3:0> bits (CHEACC<3:0>) equal to 0x0A and 0x0B (disables mask logic)

bit 4-0 **Unimplemented:** Write '0'; ignore read

**REGISTER 9-5: CHEW0: CACHE WORD 0**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW0<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW0<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW0<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW0<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEW0<31:0>:** Word 0 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
Readable only if the device is not code-protected.

**REGISTER 11-5: U1PWRC: USB POWER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | UACTPND | — | — | USLPGRD | USBBUSY | — | USUSPEND | USBPWR |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit

1 = USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit

1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit

1 = USB module is active or disabled, but not ready to be enabled
0 = USB module is not active and is ready to be enabled

**Note:** When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit

1 = USB module is placed in Suspend mode
(The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit

1 = USB module is turned on
0 = USB module is disabled
(Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

**TABLE 20-1: UART1 THROUGH UART6 REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6620 | U6TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6630 | U6RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6640 | U6BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |
| 6800 | U2MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6810 | U2STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 6820 | U2TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6830 | U2RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6840 | U2BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |
| 6A00 | U5MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | — | — | — | — | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6A10 | U5STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 6A20 | U5TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6A30 | U5RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6A40 | U5BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**REGISTER 22-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)**

bit 3 **RTCWREN:** RTC Value Registers Write Enable bit(4)
- 1 = RTC Value registers can be written to by the user
- 0 = RTC Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
- 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
- 0 = RTC Value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(5)
- 1 = Second half period of a second
- 0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit
- 1 = RTCC clock output is enabled (clock presented onto an I/O)
- 0 = RTCC clock output is disabled

**Note 1:** The ON bit is only writable when RTCWREN = 1.

**2:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

**4:** The RTCWREN bit can only be set when the write sequence is enabled.

**5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

| **Note:** | This register is only reset on a Power-on Reset (POR). |
|---|---|

**REGISTER 24-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN31 | MSEL31<1:0> | | FSEL31<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN30 | MSEL30<1:0> | | FSEL30<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN29 | MSEL29<1:0> | | FSEL29<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN28 | MSEL28<1:0> | | FSEL28<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN31:** Filter 31 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL31<1:0>:** Filter 31 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL31<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN30:** Filter 30Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL30<1:0>:** Filter 30Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL30<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 25-3: ETHTXST: ETHERNET CONTROLLER TX PACKET DESCRIPTOR START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | TXSTADDR<7:2> | | | | | | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **TXSTADDR<31:2>:** Starting Address of First Transmit Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for TX operations.
**2:** This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

**REGISTER 25-4: ETHRXST: ETHERNET CONTROLLER RX PACKET DESCRIPTOR START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | RXSTADDR<7:2> | | | | | | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **RXSTADDR<31:2>:** Starting Address of First Receive Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for RX operations.
**2:** This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

**REGISTER 25-9: ETHPMCS: ETHERNET CONTROLLER PATTERN MATCH CHECKSUM REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMCS<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMCS<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **PMCS<15:8>:** Pattern Match Checksum 1 bits

bit 7-0 **PMCS<7:0>:** Pattern Match Checksum 0 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

**REGISTER 25-10: ETHPMO: ETHERNET CONTROLLER PATTERN MATCH OFFSET REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMO<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMO<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PMO<15:0>:** Pattern Match Offset 1 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

**REGISTER 25-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MCOLFRMCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MCOLFRMCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits

Increment count for frames that were successfully transmitted after there was more than one collision.

**Note 1:** This register is only used for TX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

**REGISTER 25-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER (CONTINUED)**

bit 6 **VLANPAD:** VLAN Pad Enable bit(1,2)
1 = The MAC will pad all short frames to 64 bytes and append a valid CRC
0 = The MAC does not perform padding of short frames

bit 5 **PADENABLE:** Pad/CRC Enable bit(1,3)
1 = The MAC will pad all short frames
0 = The frames presented to the MAC have a valid length

bit 4 **CRCENABLE:** CRC Enable1 bit
1 = The MAC will append a CRC to every frame whether padding was required or not. Must be set if the PADENABLE bit is set.
0 = The frames presented to the MAC have a valid CRC

bit 3 **DELAYCRC:** Delayed CRC bit
This bit determines the number of bytes, if any, of proprietary header information that exist on the front of the IEEE 802.3 frames.
1 = Four bytes of header (ignored by the CRC function)
0 = No proprietary header

bit 2 **HUGEFRM:** Huge Frame enable bit
1 = Frames of any length are transmitted and received
0 = Huge frames are not allowed for receive or transmit

bit 1 **LENGTHCK:** Frame Length checking bit
1 = Both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the transmit/receive statistics vector.
0 = Length/Type field check is not performed

bit 0 **FULLDPLX:** Full-Duplex Operation bit
1 = The MAC operates in Full-Duplex mode
0 = The MAC operates in Half-Duplex mode

**Note 1:** Table 25-6 provides a description of the pad function based on the configuration of this register.
**2:** This bit is ignored if the PADENABLE bit is cleared.
**3:** This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

| **Note:** | Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware |
|---|---|

**TABLE 25-6: PAD OPERATION**

| Type | AUTOPAD | VLANPAD | PADENABLE | Action |
|---|---|---|---|---|
| Any | x | x | 0 | No pad, check CRC |
| Any | 0 | 0 | 1 | Pad to 60 Bytes, append CRC |
| Any | x | 1 | 1 | Pad to 64 Bytes, append CRC |
| Any | 1 | 0 | 1 | If untagged: Pad to 60 Bytes, append CRC<br>If VLAN tagged: Pad to 64 Bytes, append CRC |

**REGISTER 26-2: CMSTAT: COMPARATOR STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 |
| | — | — | — | — | — | — | C2OUT | C1OUT |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = All Comparator modules are disabled while in Idle mode
- 0 = All Comparator modules continue to operate while in Idle mode

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **C2OUT:** Comparator Output bit
- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit
- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

**NOTES:**

**TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(3)** | **Max.** | **Units** | **Conditions** | | | |
| **Operating Current (IDD)(1,2,4) for PIC32MX575/675/695/775/795 Family Devices** | | | | | | | |
| DC20 | 6 | 9 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 4 MHz |
| DC20b | 7 | 10 | | | +105ºC | | |
| DC20a | 4 | — | | Code executing from SRAM | — | | |
| DC21 | 37 | 40 | mA | Code executing from Flash | — | — | 25 MHz |
| DC21a | 25 | — | | Code executing from SRAM | | | |
| DC22 | 64 | 70 | mA | Code executing from Flash | — | — | 60 MHz |
| DC22a | 61 | — | | Code executing from SRAM | | | |
| DC23 | 85 | 98 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 80 MHz |
| DC23b | 90 | 120 | | | +105ºC | | |
| DC23a | 85 | — | | Code executing from SRAM | — | | |
| DC25a | 125 | 150 | µA | — | +25°C | 3.3V | LPRC (31 kHz) |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

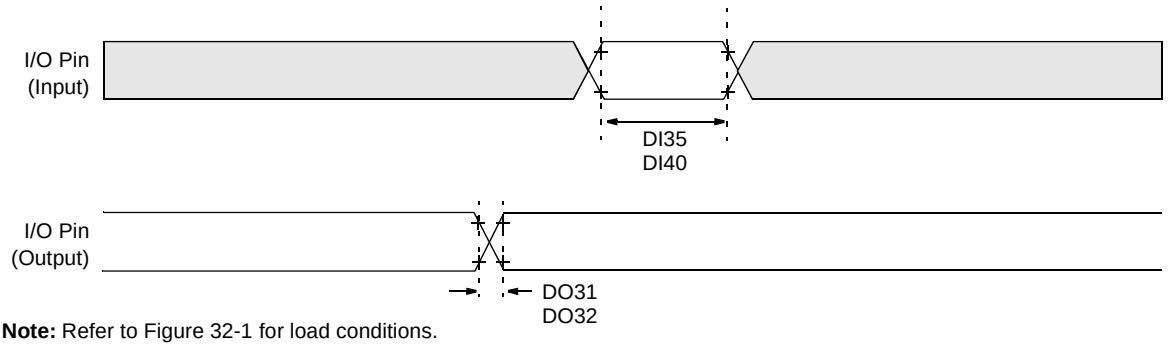
**4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

**TABLE 32-20: INTERNAL RC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **LPRC @ 31.25 kHz(1)** | | | | | | |
| F21 | LPRC | -15 | — | +15 | % | — |

**Note 1:** Change of LPRC frequency as VDD changes.

**FIGURE 32-3: I/O TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-21: I/O TIMING REQUIREMENTS**

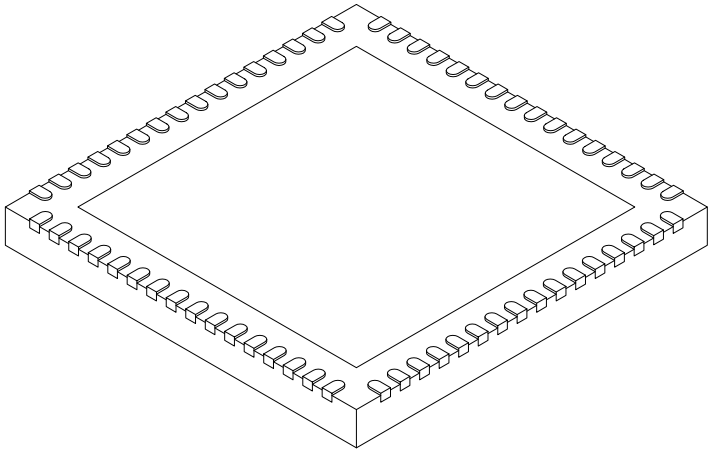
| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| DO31 | TIOR | Port Output Rise Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DO32 | TIOF | Port Output Fall Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DI35 | TINP | INTx Pin High or Low Time | 10 | — | — | ns | — |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | TSYSCLK | — |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

**2:** This parameter is characterized, but not tested in manufacturing.

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]**
**With 7.15 x 7.15 Exposed Pad [QFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 64 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 9.00 BSC | |
| Exposed Pad Width | E2 | 7.05 | 7.15 | 7.50 |
| Overall Length | D | | 9.00 BSC | |
| Exposed Pad Length | D2 | 7.05 | 7.15 | 7.50 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149C Sheet 2 of 2

# APPENDIX A: MIGRATING FROM PIC32MX3XX/4XX TO PIC32MX5XX/6XX/7XX DEVICES

This appendix provides an overview of considerations for migrating from PIC32MX3XX/4XX devices to the PIC32MX5XX/6XX/7XX family of devices. The code developed for the PIC32MX3XX/4XX devices can be ported to the PIC32MX5XX/6XX/7XX devices after making the appropriate changes outlined below.

## A.1 DMA

PIC32MX5XX/6XX/7XX devices do not support stopping DMA transfers in Idle mode.

## A.2 Interrupts

PIC32MX5XX/6XX/7XX devices have persistent interrupts for some of the peripheral modules. This means that the interrupt condition for these peripherals must be cleared before the interrupt flag can be cleared.

For example, to clear a UART receive interrupt, the user application must first read the UART Receive register to clear the interrupt condition and then clear the associated UxIF flag to clear the pending UART interrupt. In other words, the UxIF flag cannot be cleared by software until the UART Receive register is read.

Table A-1 outlines the peripherals and associated interrupts that are implemented differently on PIC32MX5XX/6XX/7XX versus PIC32MX3XX/4XX devices.

In addition, on the SPI module, the IRQ numbers for the receive done interrupts were changed from 25 to 24 and the transfer done interrupts were changed from 24 to 25.

**TABLE A-1: PIC32MX3XX/4XX VERSUS PIC32MX5XX/6XX/7XX INTERRUPT IMPLEMENTATION DIFFERENCES**

| Module | Interrupt Implementation |
|---|---|
| Input Capture | To clear an interrupt source, read the Buffer Result (ICxBUF) register to obtain the number of capture results in the buffer that are below the interrupt threshold (specified by ICI<1:0> bits). |
| SPI | Receive and transmit interrupts are controlled by the SRXISEL<1:0> and STXISEL<1:0> bits, respectively. To clear an interrupt source, data must be written to, or read from, the SPIxBUF register to obtain the number of data to receive/transmit below the level specified by the SRXISEL<1:0> and STXISEL<1:0> bits. |
| UART | TX interrupt will be generated as soon as the UART module is enabled.<br>Receive and transmit interrupts are controlled by the URXISEL<1:0> and UTXISEL<1:0> bits, respectively. To clear an interrupt source, data must be read from, or written to, the UxRXREG or UxTXREG registers to obtain the number of data to receive/transmit below the level specified by the URXISEL<1:0> and UTXISEL<1:0> bits. |
| ADC | All samples must be read from the result registers (ADC1BUFx) to clear the interrupt source. |
| PMP | To clear an interrupt source, read the Parallel Master Port Data Input/Output (PMDIN/PMDOUT) register. |