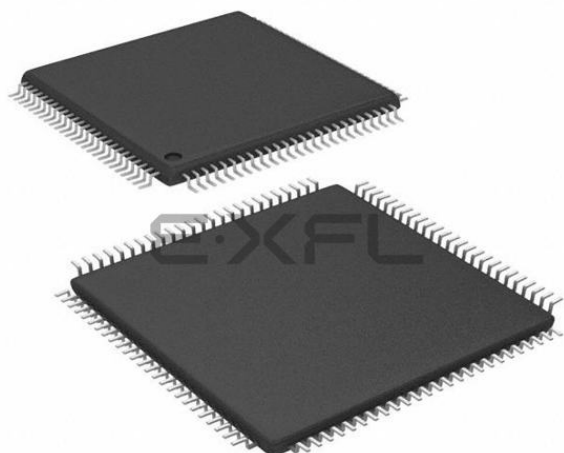




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx695f512lt-80v-pf

TABLE 8: PIN NAMES FOR 100-PIN USB AND ETHERNET DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MX664F064L
 PIC32MX664F128L
 PIC32MX675F256L
 PIC32MX675F512L
 PIC32MX695F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
71	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	86	VDD
72	SDO1/OC1/INT0/RD0	87	ETXD1/PMD11/RF0
73	SOSCI/CN1/RC13	88	ETXD0/PMD10/RF1
74	SOSCO/T1CK/CN0/RC14	89	ETXERR/PMD9/RG1
75	Vss	90	PMD8/RG0
76	OC2/RD1	91	TRCLK/RA6
77	OC3/RD2	92	TRD3/RA7
78	OC4/RD3	93	PMD0/RE0
79	ETXD2/IC5/PMD12/RD12	94	PMD1/RE1
80	ETXD3/PMD13/CN19/RD13	95	TRD2/RG14
81	OC5/PMWR/CN13/RD4	96	TRD1/RG12
82	PMRD/CN14/RD5	97	TRD0/RG13
83	ETXEN/PMD14/CN15/RD6	98	PMD2/RE2
84	ETXCLK/PMD15/CN16/RD7	99	PMD3/RE3
85	VCAP/VDDCORE	100	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 10: PIN NAMES (CONTINUED) FOR USB AND CAN DEVICES

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX575F256L PIC32MX575F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row. A1			
Pin #	Full Pin Name	Pin #	Full Pin Name
J3	PGED2/AN7/RB7	K8	VDD
J4	AVDD	K9	SCK3/U4TX/U1RTS/CN21/RD15
J5	AN11/PMA12/RB11	K10	USBID/RF3
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2
J7	AN12/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6
J8	No Connect (NC)	L2	VREF-/CVREF-/PMA7/RA9
J9	No Connect (NC)	L3	AVSS
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10
K1	PGEC1/AN1/CN3/RB1	L6	AC1TX/SCK4/U5TX/U2RTS/RF13
K2	PGED1/AN0/CN2/RB0	L7	AN13/PMA10/RB13
K3	VREF+/CVREF+/PMA6/RA10	L8	AN15/OCFB/PMALL/PMA0/CN12/RB15
K4	AN8/C1OUT/RB8	L9	SS3/U4RX/U1CTS/CN20/RD14
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
K6	AC1RX/SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5
K7	AN14/PMALH/PMA1/RB14		

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
CN0	48	74	B11	B40	I	ST	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
CN1	47	73	C10	A47	I	ST	
CN2	16	25	K2	B14	I	ST	
CN3	15	24	K1	A15	I	ST	
CN4	14	23	J2	B13	I	ST	
CN5	13	22	J1	A13	I	ST	
CN6	12	21	H2	B11	I	ST	
CN7	11	20	H1	A12	I	ST	
CN8	4	10	E3	A7	I	ST	
CN9	5	11	F4	B6	I	ST	
CN10	6	12	F2	A8	I	ST	
CN11	8	14	F3	A9	I	ST	
CN12	30	44	L8	A29	I	ST	
CN13	52	81	C8	B44	I	ST	
CN14	53	82	B8	A55	I	ST	
CN15	54	83	D7	B45	I	ST	
CN16	55	84	C7	A56	I	ST	
CN17	31	49	L10	B27	I	ST	
CN18	32	50	L11	A32	I	ST	
CN19	—	80	D8	A54	I	ST	
CN20	—	47	L9	B26	I	ST	
CN21	—	48	K9	A31	I	ST	
IC1	42	68	E9	B37	I	ST	Capture Inputs 1-5
IC2	43	69	E10	A45	I	ST	
IC3	44	70	D11	B38	I	ST	
IC4	45	71	C11	A46	I	ST	
IC5	52	79	A9	A60	I	ST	
OCFA	17	26	L1	A20	I	ST	Output Compare Fault A Input
OC1	46	72	D9	B39	O	—	Output Compare Output 1
OC2	49	76	A11	A52	O	—	Output Compare Output 2
OC3	50	77	A10	B42	O	—	Output Compare Output 3
OC4	51	78	B9	A53	O	—	Output Compare Output 4
OC5	52	81	C8	B44	O	—	Output Compare Output 5
OCFB	30	44	L8	A29	I	ST	Output Compare Fault B Input
INT0	46	72	D9	B39	I	ST	External Interrupt 0
INT1	42	18	G1	A11	I	ST	External Interrupt 1
INT2	43	19	G2	B10	I	ST	External Interrupt 2
INT3	44	66	E11	B36	I	ST	External Interrupt 3
INT4	45	67	E8	A44	I	ST	External Interrupt 4

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the “**Device Pin Tables**” section for device pin availability.

2: See **25.0 “Ethernet Controller”** for more information.

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. “CPU”** (DS60001113) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). Resources for the MIPS32® M4K® Processor Core are available at <http://www.imgtec.com>.

The MIPS32® M4K® Processor core is the heart of the PIC32MX5XX/6XX/7XX family processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2)
 - Multiply-accumulate and multiply-subtract instructions
 - Targeted multiply instruction
 - Zero/One detect instructions
 - WAIT instruction
 - Conditional move instructions (MOVN, MOVZ)
 - Vectored interrupts
 - Programmable exception vector base
 - Atomic interrupt enable/disable
 - GPR shadow registers to minimize latency for interrupt handlers
 - Bit field manipulation instructions
- MIPS16e® code compression
 - 16-bit encoding of 32-bit instructions to improve code density
 - Special PC-relative instructions for efficient loading of addresses and constants
 - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
 - Improved support for handling 8-bit and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- Simple dual bus interface
 - Independent 32-bit address and data busses
 - Transactions can be aborted to improve interrupt latency
- Autonomous multiply/divide unit
 - Maximum issue rate of one 32x16 multiply per clock
 - Maximum issue rate of one 32x32 multiply every other clock
 - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension-dependent)
- Power control
 - Minimum frequency: 0 MHz
 - Low-Power mode (triggered by WAIT instruction)
 - Extensive use of local gated clocks
- EJTAG debug and instruction trace
 - Support for single stepping
 - Virtual instruction and data address/value
 - Breakpoints
 - PC tracing with trace compression

FIGURE 3-1: MIPS32® M4K® PROCESSOR CORE BLOCK DIAGRAM

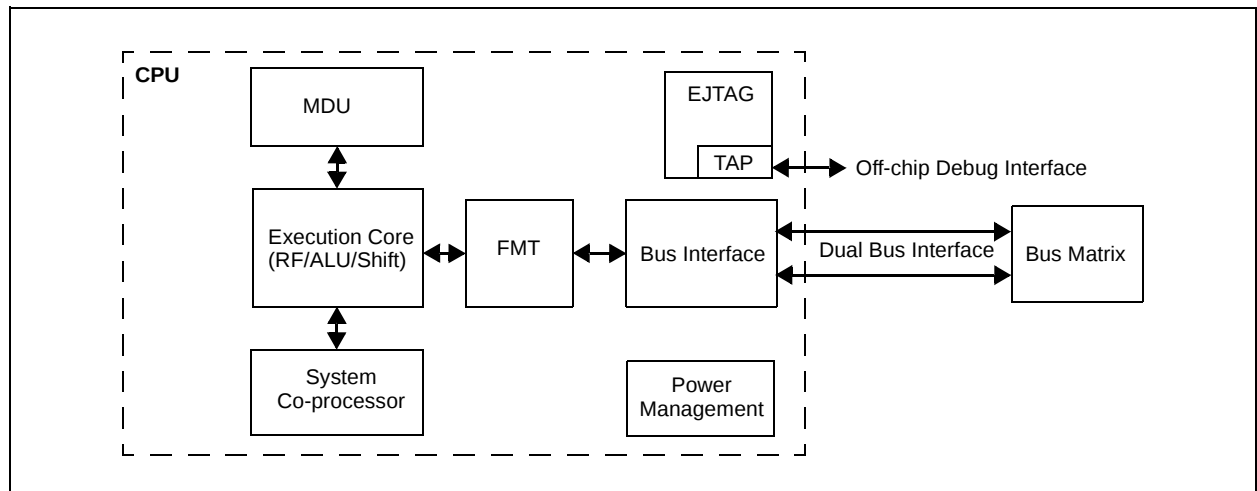
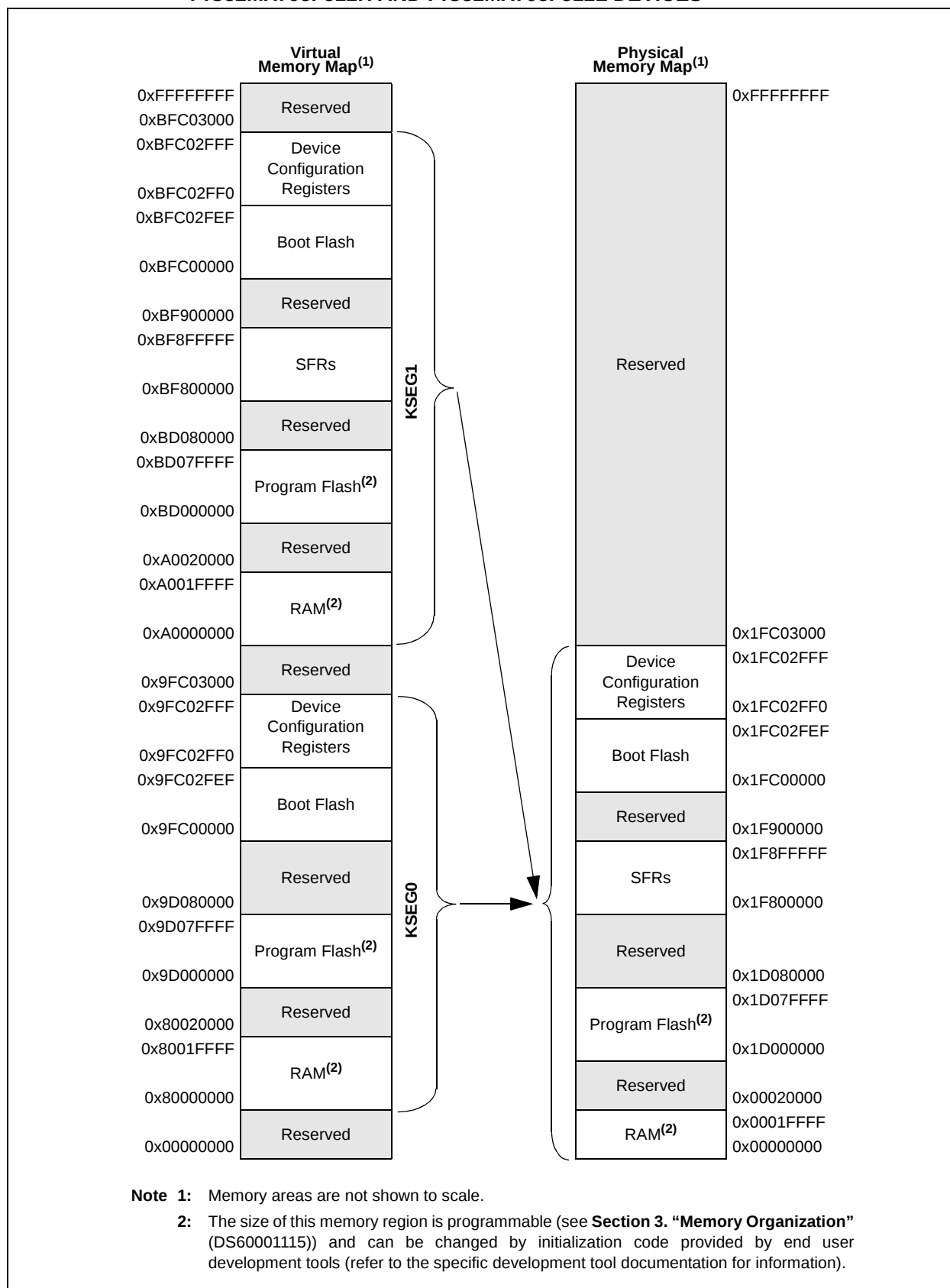


FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX695F512H, PIC32MX695F512L, PIC32MX795F512H AND PIC32MX795F512L DEVICES



REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDKPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDKPBA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits

When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** DRM Kernel Program Base Address Read-Only bits

Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

PIC32MX5XX/6XX/7XX

REGISTER 9-6: CHEW1: CACHE WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW1<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW1<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW1<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW1<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEW1<31:0>**: Word 1 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
 Readable only if the device is not code-protected.

REGISTER 9-7: CHEW2: CACHE WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW2<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW2<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW2<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW2<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEW2<31:0>**: Word 2 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
 Readable only if the device is not code-protected.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CHPDAT<7:0>									
32A0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
32B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>									CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—
32C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
32D0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
32E0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
32F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								
3360	DCH4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3370	DCH4ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>									CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—
3380	DCH4INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3390	DCH4SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
33A0	DCH4DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- Note 2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

TABLE 11-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
 - 2: This register does not have associated SET and INV registers.
 - 3: This register does not have associated CLR, SET and INV registers.
 - 4: Reset value for this bit is undefined.

20.1 Control Registers

TABLE 20-1: UART1 THROUGH UART6 REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	U1MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6010	U1STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6040	U1BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	BRG<15:0>																0000
6200	U4MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	—	—	—	—	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6210	U4STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6220	U4TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6230	U4RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6240	U4BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	BRG<15:0>																0000
6400	U3MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6410	U3STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6420	U3TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6430	U3RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6440	U3BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	BRG<15:0>																0000
6600	U6MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	—	—	—	—	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6610	U6STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

21.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. “Parallel Master Port (PMP)”** (DS60001128) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

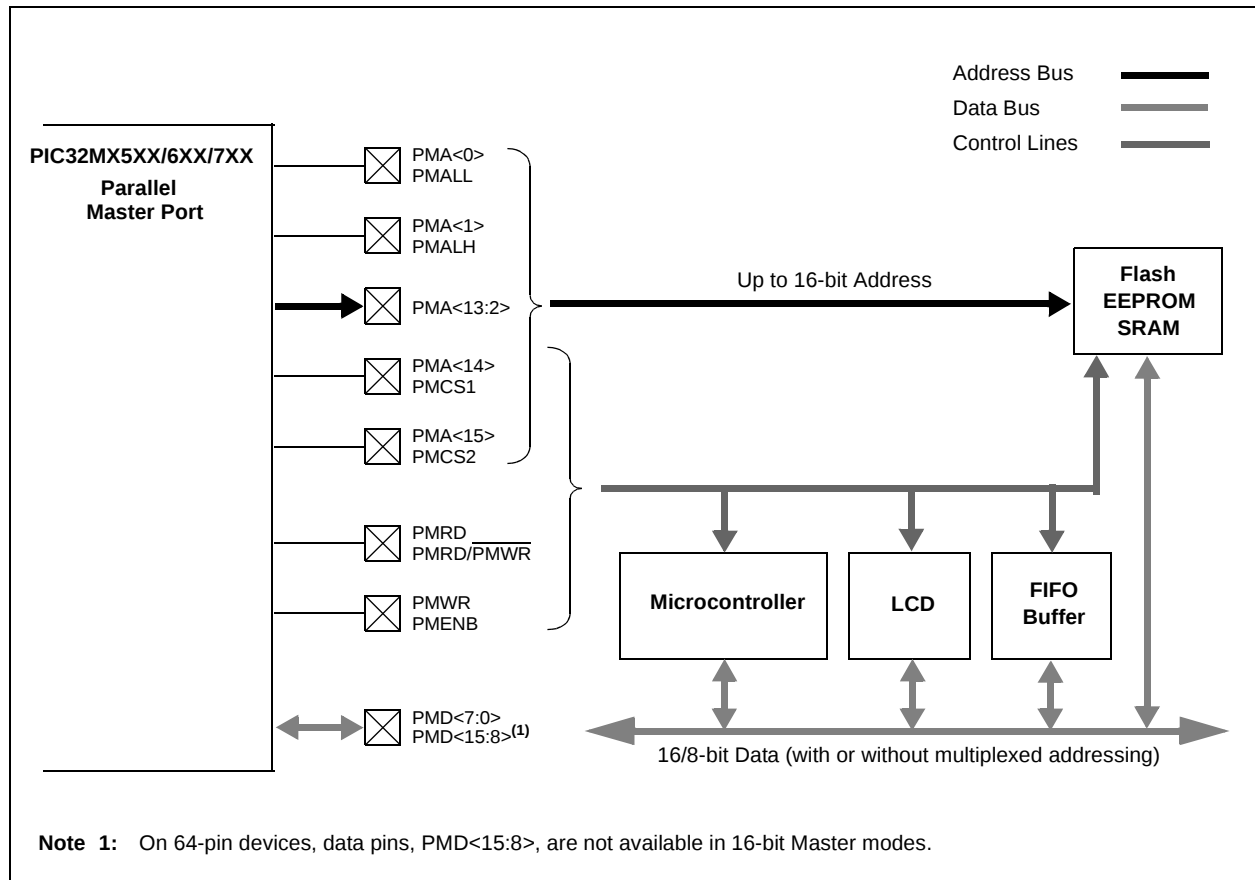
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable. Figure 21-1 shows the PMP module pinout and its connections to external devices.

The following are key features of the PMP module:

- 8-bit and 16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options
 - Individual read and write strobes, or
 - Read/Write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support
 - Legacy addressable
 - Address support
 - 4-byte deep auto-incrementing buffer
- Programmable wait states
- Operates during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Note: On 64-pin devices, the PMD<15:8> data pins are not available.

FIGURE 21-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



PIC32MX5XX/6XX/7XX

REGISTER 24-4: CIVEC: CAN INTERRUPT CODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	FILHIT<4:0>				
7:0	U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	—	ICODE<6:0> ⁽¹⁾						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bit

11111 = Filter 31
11110 = Filter 30

•
•
•

00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits⁽¹⁾

1111111 = Reserved

•
•
•

1001001 = Reserved
1001000 = Invalid message received (IVRIF)
1000111 = CAN module mode change (MODIF)
1000110 = CAN timestamp timer (CTMRIF)
1000101 = Bus bandwidth error (SERRIF)
1000100 = Address error interrupt (SERRIF)
1000011 = Receive FIFO overflow interrupt (RBOVIF)
1000010 = Wake-up interrupt (WAKIF)
1000001 = Error Interrupt (CERRIF)
1000000 = No interrupt
0111111 = Reserved

•
•
•

0100000 = Reserved
0011111 = FIFO31 Interrupt (CiFSTAT<31> set)
0011110 = FIFO30 Interrupt (CiFSTAT<30> set)

•
•
•

0000001 = FIFO1 Interrupt (CiFSTAT<1> set)
0000000 = FIFO0 Interrupt (CiFSTAT<0> set)

Note 1: These bits are only updated for enabled interrupts.

PIC32MX5XX/6XX/7XX

REGISTER 24-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN31	MSEL31<1:0>		FSEL31<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN30	MSEL30<1:0>		FSEL30<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN29	MSEL29<1:0>		FSEL29<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN28	MSEL28<1:0>		FSEL28<4:0>				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **FLTEN31:** Filter 31 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL31<1:0>:** Filter 31 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL31<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN30:** Filter 30 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL30<1:0>:** Filter 30 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL30<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 24-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' (n = 0 THROUGH 31)

- bit 6 **TXABAT:** Message Aborted bit⁽²⁾
 1 = Message was aborted
 0 = Message completed successfully
- bit 5 **TXLABB:** Message Lost Arbitration bit⁽³⁾
 1 = Message lost arbitration while being sent
 0 = Message did not lose arbitration while being sent
- bit 4 **TXERR:** Error Detected During Transmission bit⁽³⁾
 1 = A bus error occurred while the message was being sent
 0 = A bus error did not occur while the message was being sent
- bit 3 **TXREQ:** Message Send Request
 TXEN = 1: (FIFO configured as a Transmit FIFO)
 Setting this bit to '1' requests sending a message.
 The bit will automatically clear when all the messages queued in the FIFO are successfully sent.
 Clearing the bit to '0' while set ('1') will request a message abort.
 TXEN = 0: (FIFO configured as a receive FIFO)
 This bit has no effect.
- bit 2 **RTREN:** Auto RTR Enable bit
 1 = When a remote transmit is received, TXREQ will be set
 0 = When a remote transmit is received, TXREQ will be unaffected
- bit 1-0 **TXPR<1:0>:** Message Transmit Priority bits
 11 = Highest message priority
 10 = High intermediate message priority
 01 = Low intermediate message priority
 00 = Lowest message priority

- Note 1:** These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).
- 2:** This bit is updated when a message completes (or aborts) or when the FIFO is reset.
- 3:** This bit is reset on any read of this register or when the FIFO is reset.

REGISTER 26-1: CMxCON: COMPARATOR 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON ⁽¹⁾	COE	CPOL ⁽²⁾	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit⁽¹⁾

Clearing this bit does not affect the other bits in this register.

1 = Module is enabled. Setting this bit does not affect the other bits in this register

0 = Module is disabled and does not consume current.

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is driven on the output CxOUT pin

0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit⁽²⁾

1 = Output is inverted

0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit

1 = Output of the Comparator is a '1'

0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits

11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output

10 = Comparator interrupt is generated on a high-to-low transition of the comparator output

01 = Comparator interrupt is generated on a low-to-high transition of the comparator output

00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit

1 = Comparator non-inverting input is connected to the internal CVREF

0 = Comparator non-inverting input is connected to the CxIN+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator

11 = Comparator inverting input is connected to the IVREF

10 = Comparator inverting input is connected to the C2IN+ pin for C1 and C1IN+ pin for C2

01 = Comparator inverting input is connected to the C1IN+ pin for C1 and C2IN+ pin for C2

00 = Comparator inverting input is connected to the C1IN- pin for C1 and C2IN- pin for C2

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

PIC32MX5XX/6XX/7XX

TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp			
Param. No.	Typical ⁽²⁾	Max.	Units	Conditions		
Power-Down Current (IPD) ⁽¹⁾ for PIC32MX575/675/695/775/795 Family Devices						
DC40	10	40	μA	-40°C	2.3V Base Power-Down Current (Note 6)	
DC40a	36	100		+25°C		
DC40b	400	720		+85°C		
DC40h	900	1800		+105°C		
DC40c	41	120		+25°C	3.3V Base Power-Down Current	
DC40d	22	80		-40°C	3.6V Base Power-Down Current (Note 6)	
DC40e	42	120		+25°C		
DC40g	315	400 ⁽⁵⁾		+70°C		
DC40f	410	800		+85°C		
DC40i	1000	2000		+105°C		
Module Differential Current for PIC32MX575/675/695/775/795 Family Devices						
DC41	—	10	μA	—	2.3V Watchdog Timer Current: ΔI_{WDT} (Notes 3,6)	
DC41a	5	—		—	3.3V Watchdog Timer Current: ΔI_{WDT} (Note 3)	
DC41b	—	20		—	3.6V Watchdog Timer Current: ΔI_{WDT} (Note 3,6)	
DC42	—	40	μA	—	2.3V RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} (Notes 3,6)	
DC42a	23	—		—	3.3V RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} (Note 3)	
DC42b	—	50		—	3.6V RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} (Note 3,6)	
DC43	—	1300	μA	—	2.5V ADC: ΔI_{ADC} (Notes 3,4,6)	
DC43a	1100	—		—	3.3V ADC: ΔI_{ADC} (Notes 3,4)	
DC43b	—	1300		—	3.6V ADC: ΔI_{ADC} (Notes 3,4,6)	

Note 1: The test conditions for IPD current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0)
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to V_{SS}
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

FIGURE 32-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

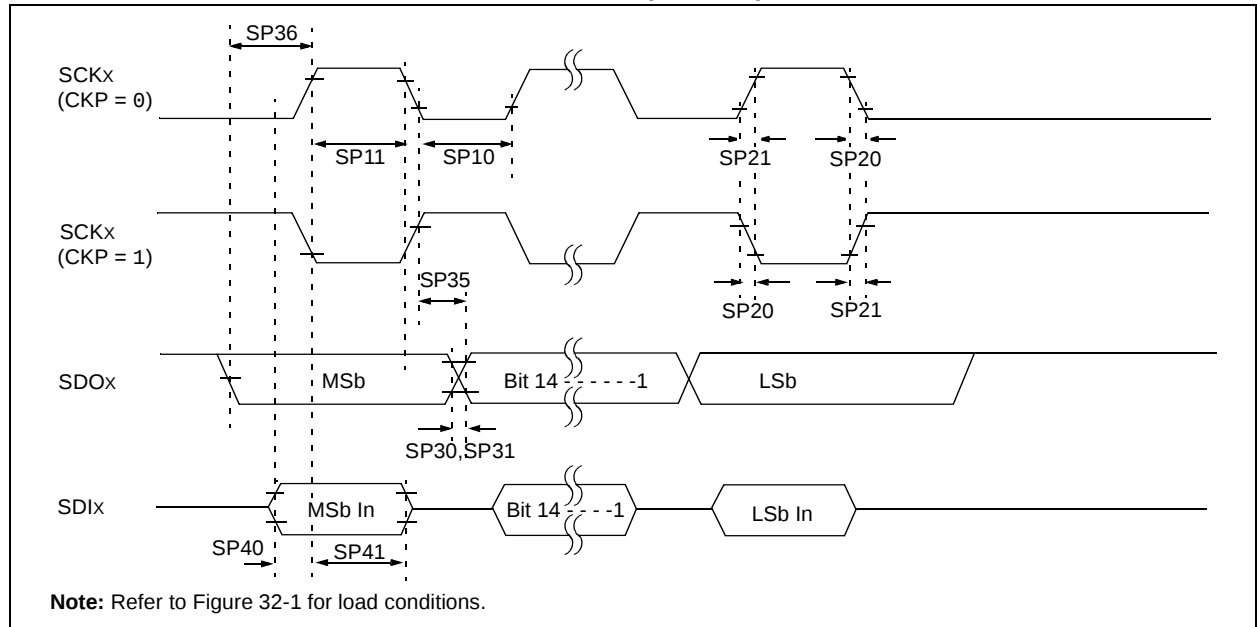


TABLE 32-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TsCL	SCKx Output Low Time ⁽³⁾	TsCK/2	—	—	ns	—
SP11	TsCH	SCKx Output High Time ⁽³⁾	TsCK/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP30	TDoF	SDOx Data Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP31	TDoR	SDOx Data Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP35	Tsch2DoV, TsCL2DoV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP36	TDoV2sc, TDoV2sCL	SDOx Data Output Setup to First SCKx Edge	15	—	—	ns	—
SP40	TDiV2sch, TDiV2sCL	Setup Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V
SP41	Tsch2DiL, TsCL2DiL	Hold Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V

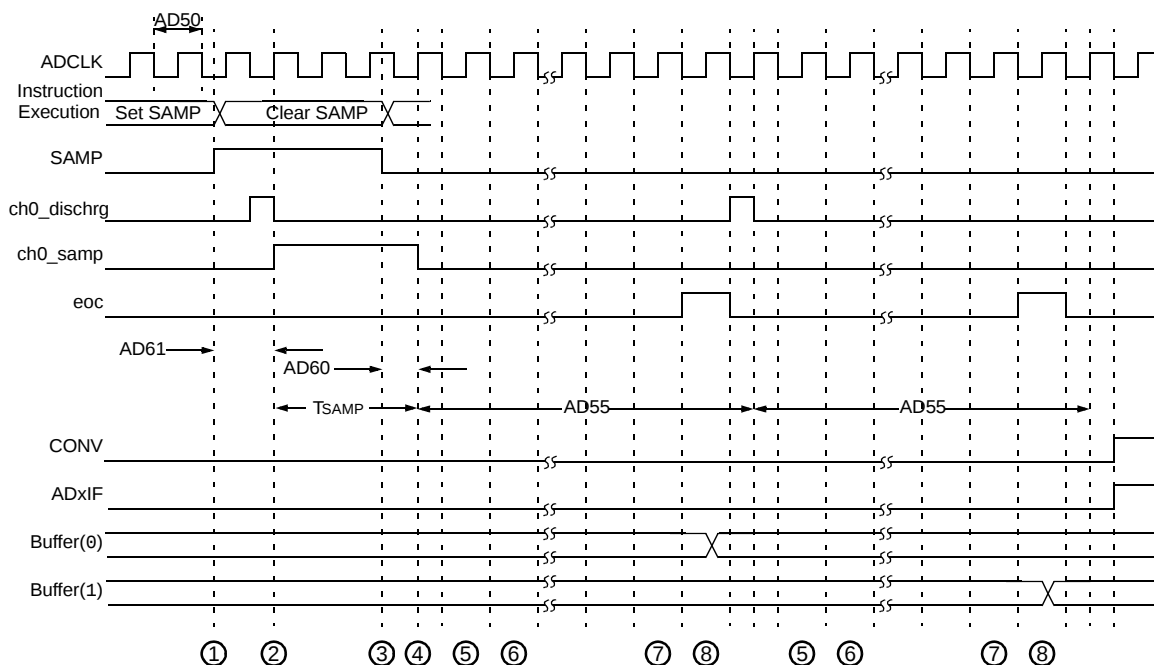
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 32-23: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)

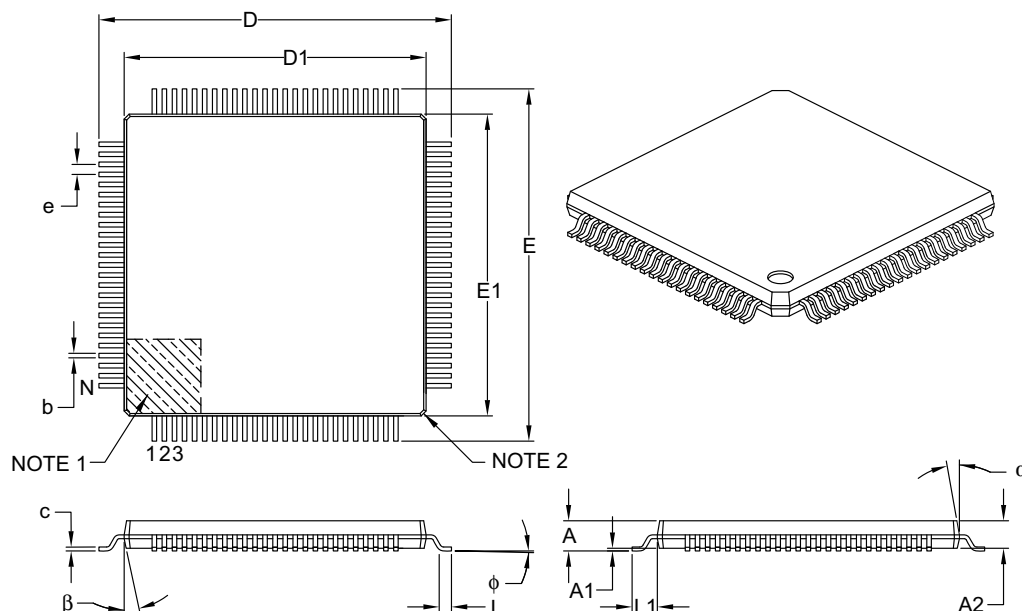


- ① – Software sets ADxCON.SAMP to start sampling.
- ② – Sampling starts after discharge period. TSAMP is described in Section 17. “10-bit A/D Converter” (DS60001104) of the “PIC32 Family Reference Manual”.
- ③ – Software clears ADxCON.SAMP to start conversion.
- ④ – Sampling ends, conversion sequence starts.
- ⑤ – Convert bit 9.
- ⑥ – Convert bit 8.
- ⑦ – Convert bit 0.
- ⑧ – One TAD for end of conversion.

PIC32MX5XX/6XX/7XX

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	100		
Lead Pitch	e	0.40 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E	14.00 BSC		
Overall Length	D	14.00 BSC		
Molded Package Width	E1	12.00 BSC		
Molded Package Length	D1	12.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

PIC32MX5XX/6XX/7XX

Revision H (March 2013)

This revision includes the following global updates:

- Where applicable, control register tables have been added to the document
- All references to VCORE were removed
- All occurrences of XBGA have been updated to: TFBGA

- All occurrences of VUSB have been updated to: VUSB3v3

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other significant changes are referenced by their respective section in Table B-6.

TABLE B-6: MAJOR SECTION UPDATES

Section Name	Update Description
“32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet”	Updated Core features. Added the VTLA to the Packages table. Added Note 5 to the Feature tables (see Table 1, Table 2, and Table 3).
Section 2.0 “Guidelines for Getting Started with 32-bit MCUs”	The Recommended Minimum Connection was updated (see Figure 2-1).
Section 5.0 “Flash Program Memory”	A note regarding Flash page size and row size was added.
Section 8.0 “Oscillator Configuration”	The R _P resistor was added and Note 1 was updated in the Oscillator Diagram (see Figure 8-1).
Section 31.0 “Electrical Characteristics”	Added Note 1 to Operating MIPS vs. Voltage (see Table 31-1). Added the VTLA package to Thermal Packaging Characteristics (see Table 31-3). Added Note 2 to DC Temperature and Voltage Specifications (see Table 31-4). Updated Note 2 in the Operating Current DC Characteristics (see Table 31-5). Updated Note 1 in the Idle Current DC Characteristics (see Table 31-6). Updated Note 1 in the Power-Down Current DC Characteristics (see Table 31-7). Updated the I/O Pin Output Specifications (see Table 31-9). Added Note 2 to the BOR Electrical Characteristics (see Table 31-10). Added Note 3 to the Comparator Specifications (see Table 31-13). Parameter D320 (VCORE) was removed (see Table 31-15). Updated the Minimum value for parameter OS50 (see Table 31-18). Parameter SY01 (TPWRT) was removed (see Table 31-22). Note 1 was added and the conditions for parameters ET3, ET4, ET7, and ET9 were updated in the Ethernet Module Specifications (see Table 31-35). Added Note 6 to the ADC Module Specifications (see Table 31-36). Added Note 3 to the 10-bit ADC Conversion Rate Parameter (see Table 31-37). Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 31-38). The following figures were added: Figure 31-19: “MDIO Sourced by the PIC32 Device” Figure 31-21: “Transmit Signal Timing Relationships at the MII” Figure 31-22: “Receive Signal Timing Relationships at the MII”
Section 32.0 “DC and AC Device Characteristics Graphs”	This new chapter was added.
Section 33.0 “Packaging Information”	Added the 124-lead VTLA package information (see Section 33.1 “Package Marking Information” and Section 33.2 “Package Details”).
“Product Identification System”	Added the TL definition for VTLA packages.