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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx695f512lt-80v-pt

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PIC32MX5XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUE
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		Pin Nun	nber ⁽¹⁾			Duffer	
Pin Name	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA	Pin Type	Buffer Type	Description
RA0	_	17	G3	B9	I/O	ST	PORTA is a bidirectional I/O port
RA1	_	38	J6	A26	I/O	ST	
RA2	_	58	H11	A39	I/O	ST	
RA3	_	59	G10	B32	I/O	ST	
RA4	_	60	G11	A40	I/O	ST	
RA5	_	61	G9	B33	I/O	ST	
RA6	_	91	C5	B51	I/O	ST	
RA7	_	92	B5	A62	I/O	ST	
RA9	_	28	L2	A21	I/O	ST	
RA10	_	29	K3	B17	I/O	ST	
RA14	_	66	E11	B36	I/O	ST	
RA15	_	67	E8	A44	I/O	ST	
RB0	16	25	K2	B14	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	K1	A15	I/O	ST	
RB2	14	23	J2	B13	I/O	ST	
RB3	13	22	J1	A13	I/O	ST	
RB4	12	21	H2	B11	I/O	ST	
RB5	11	20	H1	A12	I/O	ST	
RB6	17	26	L1	A20	I/O	ST	
RB7	18	27	J3	B16	I/O	ST	
RB8	21	32	K4	A23	I/O	ST	
RB9	22	33	L4	B19	I/O	ST	
RB10	23	34	L5	A24	I/O	ST	
RB11	24	35	J5	B20	I/O	ST	
RB12	27	41	J7	B23	I/O	ST	
RB13	28	42	L7	A28	I/O	ST	
RB14	29	43	K7	B24	I/O	ST	
RB15	30	44	L8	A29	I/O	ST	
RC1	—	6	D1	A5	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	E4	B4	I/O	ST	
RC3	—	8	E2	A6	I/O	ST	
RC4		9	E1	B5	I/O	ST	
RC12	39	63	F9	B34	I/O	ST	
RC13	47	73	C10	A47	I/O	ST	
RC14	48	74	B11	B40	I/O	ST	
RC15	40	64	F11	A42	I/O	ST	
Legend: C	CMOS = CMC	S compatib	le input or o	output S levels	A	nalog = A	Analog input P = Power

TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the "Device Pin Tables" section for device pin availability.

2: See 25.0 "Ethernet Controller" for more information.

2.9 Configuration of Analog and Digital Pins During ICSP Operations

If MPLAB ICD 3 or REAL ICE is selected as a debugger, it automatically initializes all of the Analog-to-Digital input pins (ANx) as "digital" pins by setting all bits in the AD1PCFG register.

The bits in this register that correspond to the Analogto-Digital pins that are initialized by MPLAB ICD 3 or REAL ICE, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain ADC pins as analog input pins during the debug session, the user application must clear the corresponding bits in the AD1PCFG register during initialization of the ADC module.

When MPLAB ICD 3 or REAL ICE is used as a programmer, the user application firmware must correctly configure the AD1PCFG register. Automatic initialization of this register is only done during debugger operation. Failure to correctly configure the register(s) will result in all ADC pins being recognized as analog input pins, resulting in the port value being read as a logic '0', which may affect user application functionality.

2.10 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

2.11 EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations

The use of LDO regulators is preferred to reduce overall system noise and provide a cleaner power source. However, when utilizing switching Buck/ Boost regulators as the local power source for PIC32 devices, as well as in electrically noisy environments or test conditions required for IEC 61000-4-4 and IEC 61000-4-2, users should evaluate the use of T-Filters (i.e., L-C-L) on the power pins, as shown in Figure 2-4. In addition to a more stable power source, use of this type of T-Filter can greatly reduce susceptibility to EMI sources and events.

FIGURE 2-4: EMI/EMC/EFT SUPPRESSION CIRCUIT



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	_	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—		—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0			
15:8				BMXDK	PBA<15:8>						
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
7:0	BMXDKPBA<7:0>										

REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** DRM Kernel Program Base Address Read-Only bits Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

7.0 INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupts"** (DS60001108) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX5XX/6XX/7XX devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The Interrupt Controller module includes the following features:

- Up to 96 interrupt sources
- Up to 64 interrupt vectors
- Single and multi-vector mode operations
- · Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable sub-priority levels within each priority
- Dedicated shadow set for user-selectable priority level
- Software can generate any interrupt
- User-configurable interrupt vector table location
- · User-configurable interrupt vector spacing

A simplified block diagram of the Interrupt Controller module is illustrated in Figure 7-1.





PIC32MX5XX/6XX/7XX

REGISTER 11-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	—	—	—	—	—	_	—	—
7.0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
7:0	UTEYE	UOEMON	_	USBSIDL	_	_	_	UASUSPND

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 UTEYE: USB Eye-Pattern Test Enable bit
 - 1 = Eye-Pattern Test is enabled
 - 0 = Eye-Pattern Test is disabled
- bit 6 **UOEMON:** USB OE Monitor Enable bit
 - $1 = \overline{OE}$ signal is active; it indicates intervals during which the D+/D- lines are driving
 - $0 = \overline{OE}$ signal is inactive
- bit 5 Unimplemented: Read as '0'
- bit 4 USBSIDL: Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode
- bit 3-1 Unimplemented: Read as '0'

bit 0 UASUSPND: Automatic Suspend Enable bit

- 1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 11-5.
- 0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock.

TABLE 12-13: CHANGE NOTICE AND PULL-UP REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512 AND PIC32MX795F512L DEVICES PIC32MX795F512L DEVICES

ess		â	Bits												\$				
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
C1 C0		31:16	_		_	_	—	_	_	_		_	_	_		_	_	_	0000
6100	CINCOIN	15:0	ON	—	SIDL	_	_	_	_	_	—	_	_	_	_	_	_	_	0000
6100		31:16	—	_		-				_	_		CNEN21	CNEN20	CNEN19	CNEN18	CNEN17	CNEN16	0000
6100	CINEIN	15:0	CNEN15	CNEN14	CNEN13	CNEN12	CNEN11	CNEN10	CNEN9	CNEN8	CNEN7	CNEN6	CNEN5	CNEN4	CNEN3	CNEN2	CNEN1	CNEN0	0000
6150		31:16	—										CNPUE21	CNPUE20	CNPUE19	CNPUE18	CNPUE17	CNPUE16	0000
OTEU	CINPUE	15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	CNPUE11	CNPUE10	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 12-14: CHANGE NOTICE AND PULL-UP REGISTER MAP FOR PIC32MX575F256H, PIC32MX575F512H, PIC32MX675F512H, PIC32MX675F512H, PIC32MX675F512H, PIC32MX775F512H, PIC32MX775F512H, PIC32MX795F512H, DEVICES

ess					Bits														
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6100	CNICON	31:16	-	_	_	-	—	-	—	-	-	_	-	—	_	—	-	—	0000
6100	CINCOIN	15:0	ON	_	SIDL	-		—	-	—	-	_	-	—	_	—	-		0000
6100		31:16		_	-	_	_	_	_		_	_	_		_	CNEN18	CNEN17	CNEN16	0000
0100	CINEIN	15:0	CNEN15	CNEN14	CNEN13	CNEN12	CNEN11	CNEN10	CNEN9	CNEN8	CNEN7	CNEN6	CNEN5	CNEN4	CNEN3	CNEN2	CNEN1	CNEN0	0000
6150		31:16		_	-	_	_	-	—	-	—	_	—	-	_	CNPUE18	CNPUE17	CNPUE16	0000
OTEU	CINPUE	15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	CNPUE11	CNPUE10	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

PIC32MX5XX/6XX/7XX



FIGURE 14-2: TIMER2/3 AND TIMER4/5 BLOCK DIAGRAM (32-BIT)

16.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 15. "Input Capture" (DS60001122) of the "*PIC32 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
 - Capture timer value on every falling edge of input at ICx pin
 - Capture timer value on every rising edge of input at ICx pin

- Capture timer value on every edge (rising and falling)
- Capture timer value on every edge (rising and falling), specified edge first.
- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input Capture module can also be used to provide additional sources of external interrupts



FIGURE 16-1: INPUT CAPTURE BLOCK DIAGRAM

17.1 **Control Registers**

ess										Bi	ts								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000	001000	31:16	_	—		—	—	_		_	_		—	-	—	_	_	_	0000
3000	OCICON	15:0	ON	_	SIDL	_	-	-	-		_		OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3010	OC1R	31:16								OC1R	<31:0>								xxxx
00.0		15:0								00.11	1011.07								XXXX
3020	OC1RS	31:16		OC1RS<31:0>											XXXX				
		15:0																	
3200	OC2CON	15.0		_		_	_	_		_	_	_	-				OCM<2:0>	_	0000
		31.16			OIDE								0002	OOLEI	OUTOLL		0011112.02		****
3210	OC2R	15:0								OC2R	<31:0>								xxxx
0000	000000	31:16																	
3220	UC2RS	15:0		OC2RS<31:0>										xxxx					
3400		31:16	-	_	_	—	—	_	_	_	_	—	—	-	—	_	—	_	0000
3400	003001	15:0	ON	_	SIDL	—	_			_	—	—	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3410	OC3R	31:16								OC3R	<31:0>								xxxx
		15:0																	XXXX
3420	OC3RS	31:16 15:0								OC3R5	<31:0>								XXXX
		31.16	_									_		_					0000
3600	OC4CON	15:0	ON	_	SIDL	_	_	_	_	_	_	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
		31:16]				xxxx
3610	OC4R	15:0								OC4R	<31:0>								xxxx
2620	OC 4 PS	31:16								0040	-21:0								xxxx
3020	004K3	15:0								00463	\$<31.0>								xxxx
3800	OC5CON	31:16	_	—		—	—	_		_	_	_	—	—	—		—		0000
0000		15:0	ON	ON - SIDL OC32 OCFLT OCTSEL OCM<2:0> 00										0000					
3810	OC5R	31:16	OC5R<31:0>										XXXX						
		15:0																	XXXX
3820	OC5RS	15.0		OC5RS<31:0>															
		10.0																	1 ~~~~~

PIC32MX5XX/6XX/7

TABLE 17-1: OUTPUT COMPARE 1-OUTPUT COMPARE 5 REGISTER MAP

Legend:

x = unknown value on Reset; ---- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more Note 1: information.

0 = Start condition is not in progress

I2CxCON: I²C CONTROL REGISTER (CONTINUED) REGISTER 19-1: **GCEN:** General Call Enable bit (when operating as I²C slave) bit 7 1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception) 0 = General call address is disabled STREN: SCLx Clock Stretch Enable bit (when operating as I²C slave) bit 6 Used in conjunction with SCLREL bit. 1 = Enable software or receive clock stretching 0 = Disable software or receive clock stretching bit 5 ACKDT: Acknowledge Data bit (when operating as I²C master, applicable during master receive) Value that is transmitted when the software initiates an acknowledge sequence. 1 = Send NACK during an acknowledge 0 = Send ACK during an acknowledge bit 4 ACKEN: Acknowledge Sequence Enable bit (when operating as I²C master, applicable during master receive) 1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence. 0 = Acknowledge sequence not in progress bit 3 **RCEN:** Receive Enable bit (when operating as I²C master) 1 = Enables Receive mode for l^2C . Hardware clear at end of eighth bit of master receive data byte. 0 = Receive sequence is not in progress **PEN:** Stop Condition Enable bit (when operating as I²C master) bit 2 1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence. 0 = Stop condition is not in progress **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master) bit 1 1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence. 0 = Repeated Start condition is not in progress **SEN:** Start Condition Enable bit (when operating as I²C master) bit 0 1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-1: UXMODE: UARTX MODE REGISTER (CONTINUED)

- bit 5 ABAUD: Auto-Baud Enable bit 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
 - 0 = Baud rate measurement disabled or completed
- bit 4 **RXINV:** Receive Polarity Inversion bit
 - 1 = UxRX Idle state is '0'
 - 0 = UxRX Idle state is '1'
- bit 3 BRGH: High Baud Rate Enable bit
 - 1 = High-Speed mode 4x baud clock enabled
 - 0 = Standard Speed mode 16x baud clock enabled
- bit 2-1 PDSEL<1:0>: Parity and Data Selection bits
 - 11 = 9-bit data, no parity
 - 10 = 8-bit data, odd parity
 - 01 = 8-bit data, even parity
 - 00 = 8-bit data, no parity
- bit 0 STSEL: Stop Selection bit
 - 1 = 2 Stop bits
 - 0 = 1 Stop bit
- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

- bit 7-0 ARPT<7:0>: Alarm Repeat Counter Value bits⁽²⁾
 11111111 = Alarm will trigger 256 times
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 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is only reset on a Power-on Reset (POR).

PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
31.24	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
22:46	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23.10	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
10.0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7.0	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0

REGISTER 24-7: CIRXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-0 RXOVF<31:0>: FIFOn Receive Overflow Interrupt Pending bit

1 = FIFO has overflowed

0 = FIFO has not overflowed

REGISTER 24-8: CITMR: CAN TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	CANTS<15:8>							
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	CANTS<7:0>							
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	CANTSPRE<15:8>							
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CANTSPRE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 CANTS<15:0>: CAN Time Stamp Timer bits

This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (CiCON<20>) is set.

bit 15-0 CANTSPRE<15:0>: CAN Time Stamp Timer Prescaler bits

1111 1111 1111 = CAN time stamp timer (CANTS) increments every 65,535 system clocks
.

0000 0000 0000 = CAN time stamp timer (CANTS) increments every system clock

Note 1: CiTMR will be paused when CANCAP = 0.

2: The CiTMR prescaler count will be reset on any write to CiTMR (CANTSPRE will be unaffected).

REGISTER 25-18: ETHSCOLFRM: ETHERNET CONTROLLER SINGLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—		—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	_	—
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	SCOLFRMCNT<15:8>							
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0				SCOLFRM	ICNT<7:0>			

Legend:

3			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 **SCOLFRMCNT<15:0>:** Single Collision Frame Count bits Increment count for frames that were successfully transmitted on the second try.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER (CONTINUED)

- VLANPAD: VLAN Pad Enable bit^(1,2) bit 6 1 = The MAC will pad all short frames to 64 bytes and append a valid CRC 0 = The MAC does not perform padding of short frames PADENABLE: Pad/CRC Enable bit^(1,3) bit 5 1 = The MAC will pad all short frames 0 = The frames presented to the MAC have a valid length bit 4 CRCENABLE: CRC Enable1 bit 1 = The MAC will append a CRC to every frame whether padding was required or not. Must be set if the PADENABLE bit is set. 0 = The frames presented to the MAC have a valid CRC bit 3 DELAYCRC: Delayed CRC bit This bit determines the number of bytes, if any, of proprietary header information that exist on the front of the IEEE 802.3 frames. 1 = Four bytes of header (ignored by the CRC function) 0 = No proprietary header bit 2 HUGEFRM: Huge Frame enable bit 1 = Frames of any length are transmitted and received 0 = Huge frames are not allowed for receive or transmit LENGTHCK: Frame Length checking bit bit 1 1 = Both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the transmit/receive statistics vector. 0 = Length/Type field check is not performed bit 0 FULLDPLX: Full-Duplex Operation bit 1 = The MAC operates in Full-Duplex mode 0 = The MAC operates in Half-Duplex mode
- Note 1: Table 25-6 provides a description of the pad function based on the configuration of this register.
 - 2: This bit is ignored if the PADENABLE bit is cleared.
 - **3:** This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

TABLE 25-6:PAD OPERATION

Туре	AUTOPAD	VLANPAD	PADENABLE	Action
Any	x	x	0	No pad, check CRC
Any	0	0	1	Pad to 60 Bytes, append CRC
Any	х	1	1	Pad to 64 Bytes, append CRC
Any	1	0	1	If untagged: Pad to 60 Bytes, append CRC If VLAN tagged: Pad to 64 Bytes, append CRC

REGISTER 25-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
7.0	_			B2	BIPKTGP<6:()>		

Legend:

Logona			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-7 Unimplemented: Read as '0'

bit 6-0 B2BIPKTGP<6:0>: Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 100 Mbps) (in 100 Mbps) or 9.6 μ s (in 100 Mbps) (in 100 Mbps) (in 100 Mbps) or 9.6 μ s (in 100 Mbps) (in

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE 32-35: ETHERNET MODULE SPECIFICATIONS

AC CHARACTERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param. No.	Characteristic	Min.	Typical	Max.	Units	Conditions
MIIM Tin	MIIM Timing Requirements					
ET1	MDC Duty Cycle	40		60	%	—
ET2	MDC Period	400	—	_	ns	—
ET3	MDIO Output Setup and Hold	10	—	10	ns	See Figure 32-19
ET4	MDIO Input Setup and Hold	0	—	300	ns	See Figure 32-20
MII Timi	MII Timing Requirements					
ET5	TX Clock Frequency	—	25	_	MHz	—
ET6	TX Clock Duty Cycle	35	_	65	%	—
ET7	ETXDx, ETEN, ETXERR Output Delay	0		25	ns	See Figure 32-21
ET8	RX Clock Frequency	—	25		MHz	—
ET9	RX Clock Duty Cycle	35		65	%	—
ET10	ERXDx, ERXDV, ERXERR Setup and Hold	10		30	ns	See Figure 32-22
RMII Tin	RMII Timing Requirements					
ET11	Reference Clock Frequency	_	50		MHz	—
ET12	Reference Clock Duty Cycle	35	_	65	%	_
ET13	ETXDx, ETEN, Setup and Hold	2	—	4	ns	—
ET14	ERXDx, ERXDV, ERXERR Setup and Hold	2	—	4	ns	—

Note 1: The Ethernet module is functional at VBORMIN < VDD < 2.9V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 32-19: MDIO SOURCED BY THE PIC32 DEVICE



FIGURE 32-20: MDIO SOURCED BY THE PHY



TABLE B-4: SECTION UPDATES (CONTINUED)

Section Name	Update Description
7.0 "Interrupt Controller"	 Updated the following Interrupt Sources in Table 7-1:
	- Changed IC2AM – I2C4 Master Event to: IC4M – I2C4 Master Event
	 Changed IC3AM – I2C5 Master Event to: IC5M – I2C4 Master Event
	- Changed U1E – UART1A Error to: U1E – UART1 Error
	- Changed U4E – UART1B Error to: U4E – UART4 Error
	- Changed U1RX – UART1A Receiver to: U1RX – UART1 Receiver
	- Changed U4RX – UART1B Receiver to: U4RX – UART4 Receiver
	- Changed U11X – UART1A Transmitter to: U11X – UART1 Transmitter
	- Changed U41X - UARTIB Transmitter to: U41X - UART4 Transmitter
	- Changed U6RX – UART2B End to: U6RX – UART6 Receiver
	Changed U6TX – UART2B Receiver to: U6TX – UART6 Transmitter
	- Changed USE – UART3B Error to: USE – UART5 Error
	- Changed U5RX – UART3B Receiver to: U5RX – UART5 Receiver
	- Changed U5TX – UART3B Transmitter to: U5TX – UART5 Transmitter
1.0 "Oscillator Configuration"	Updated Figure 1-1
1.0 "Output Compare"	Updated Figure 1-1
1.0 "Ethernet Controller"	Added a note on using the Ethernet controller pins (see note above
	Table 1-3)
1.0 "Comparator Voltage Reference	Updated the note in Figure 1-1
(CVREF)"	
1.0 "Special Features"	Updated the bit description for bit 10 in Register 1-2
	Added notes 1 and 2 to Register 1-4
1.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings:
	 Voltage on any 5V tolerant pin with respect to Vss when VDD < 2.3V - 0.3V to +3.6V was updated
	 Voltage on VBUS with respect to VSS - 0.3V to +5.5V was added
	Updated the maximum value of DC16 as 2.1 in Table 1-4
	Updated the Typical values for the following parameters: DC20b, DC20c, DC21c, DC22c and DC23c (see Table 1-5)
	Updated Table 1-11:
	 Removed the following DC Characteristics: Programming temperature 0°C ≤ TA ≤ +70°C (25°C recommended)
	• Updated the Minimum value for the Parameter number D131 as 2.3
	 Removed the Conditions for the following Parameter numbers: D130, D131, D132, D135, D136 and D137
	Updated the condition for the parameter number D130a and D132a
	Updated the Minimum, Typical and Maximum values for parameter D305 in Table 1-13
	Added note 2 to Table 1-18
	Updated the Minimum and Maximum values for parameter F20b (see Table 1-19)
	Updated the following figures:
	• Figure 1-4
	• Figure 1-9
	• Figure 1-22
	• Figure 1-23
Appendix A: "Migrating from PIC32MX3XX/4XX to PIC32MX5XX/ 6XX/7XX Devices"	Removed the A.3 Pin Assignments sub-section.

Revision J (September 2016)

This revision includes typographical and formatting updates throughout the data sheet text. In addition, all SFR Register maps were moved from the Memory chapter to their respective peripheral chapters.

All other major updates are referenced by their respective section in Table B-7.

TABLE B-7:	MAJOR	SECTION	UPDATES

Section Name	Update Description
"32-bit Microcontrollers (up to 512	Updated Communication Interfaces for LIN support to 2.1.
KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet"	Updated Qualification and Class B Support to AEC-Q100 REVH.
2.0 "Guidelines for Getting Started with 32-bit MCUs"	The Recommended Minimum Connection diagram was updated (see Figure 2-1).
	The Example of $\overline{\text{MCLR}}$ Pin Connections diagram was updated (see Figure 2-2).
	2.11 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations" was added.
4.0 "Memory Organization"	The SFR Memory Map was added (see Table 4-1).
7.0 "Interrupt Controller"	The UART interrupt sources were updated in the Interrupt IRQ, Vector, and Bit location table (see Table 7-1).
8.0 "Oscillator Configuration"	Updated the bit value definitions for the TUN<5:0> bits in the OCSTUN register (see Register 8-2).
15.0 "Watchdog Timer (WDT)"	The content in this chapter was relocated from the Special Features chapter to its own chapter.
18.0 "Serial Peripheral Interface (SPI)"	The register map tables were combined (see Table 18-1).
19.0 "Inter-Integrated Circuit (I ² C)"	The register map tables were combined (see Table 19-1).
	The PMADDR register was updated (see Register 21-3).
21.0 "Parallel Master Port (PMP)"	The bit value definitions for the ADRMUX<1:0> and CSF<1:0> bits in the PMCON register were updated (see Register 21-1).
29.0 "Special Features"	Removed the duplicate bit value definition for '010' in the DEVCFG2 register (see Register 29-3).
	Note 1 was added to the Programming, Debugging, and Trace Ports block diagram (see Figure 29-2).
	The DDPCON register was relocated (see Register 29-6).
	The Device ID, Revision, and Configuration Summary was updated (see Table 29-2).

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PIC32 MX 5XX F 512 H T - 80 I/PT - XXX Example: Microchip Brand		
Flash Memory Fan	nily	
Architecture	MX = 32-bit RISC MCU core	
Product Groups	5XX = General purpose microcontroller family 6XX = General purpose microcontroller family 7XX = General purpose microcontroller family	
Flash Memory Family	F = Flash program memory	
Program Memory Size	64 = 64K 128 = 128K 256 = 256K 512 = 512K	
Pin Count	H = 64-pin L = 100-pin, 121-pin, 124-pin	
Speed (see Note 1)	Blank or 80 = 80 MHz	
Temperature Range	I = -40°C to +85°C (Industrial) V = -40°C to +105°C (V-Temp)	
Package	PackagePT= 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) PTPT= 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) PFPF= 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack) MRMR= 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat) BGBG= 121-Lead (10x10x1.1 mm) TFBGA (Plastic Thin Profile Ball Grid Array) TLTL= 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array)	
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample	
Note 1: This opt	ion is not available for PIC32MX534/564/664/764 devices.	