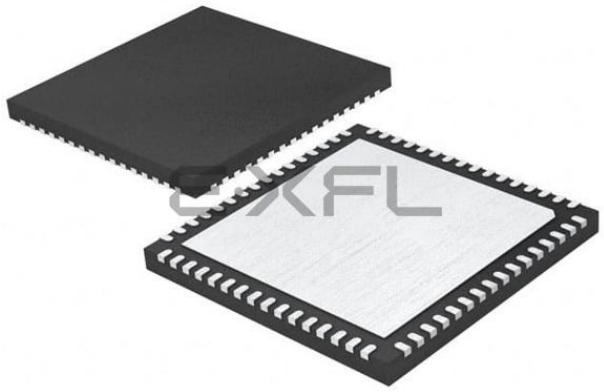

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx764f128h-v-mr

TABLE 8: PIN NAMES FOR 100-PIN USB AND ETHERNET DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MX664F064L
PIC32MX664F128L
PIC32MX675F256L
PIC32MX675F512L
PIC32MX695F512L

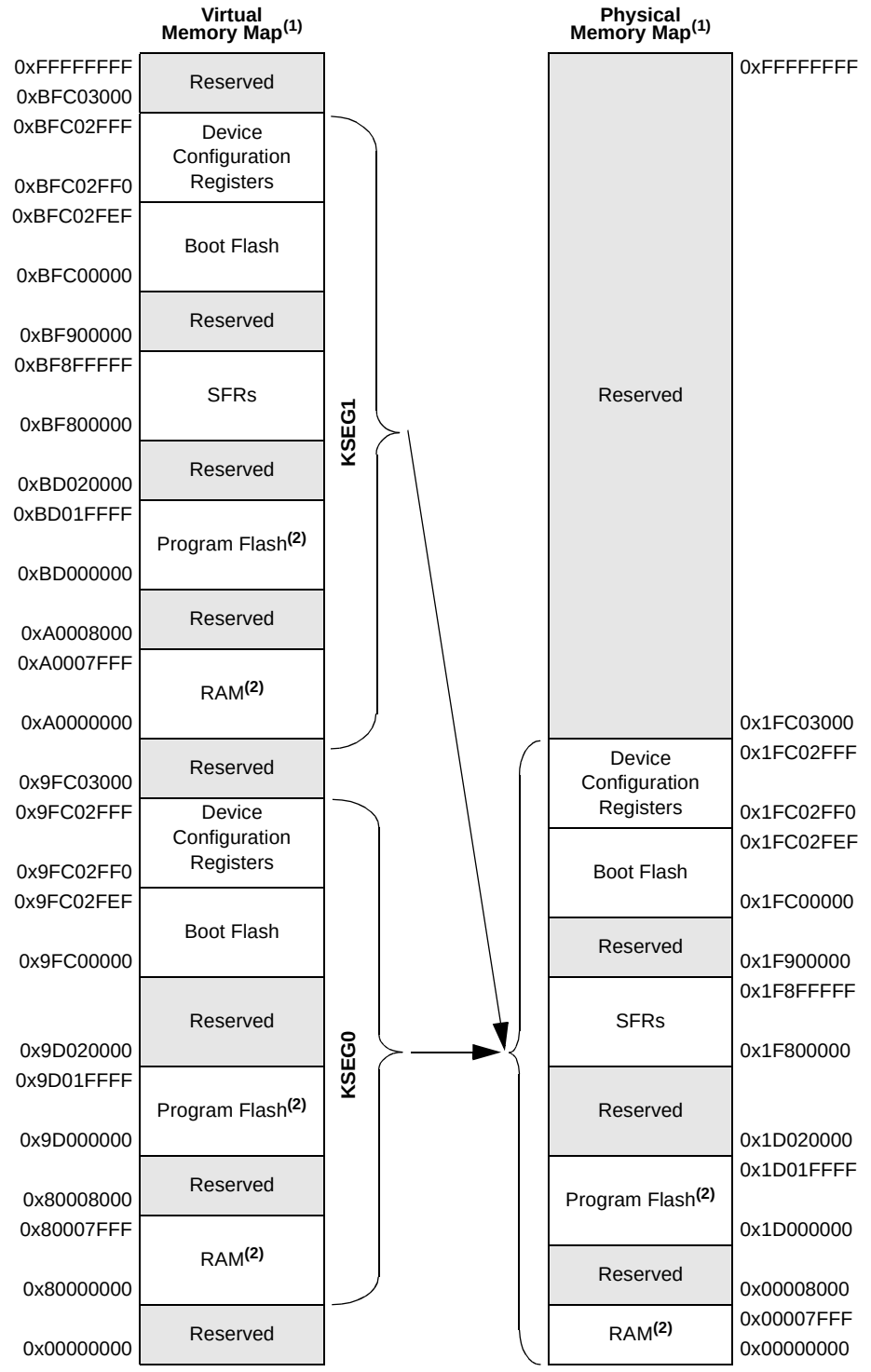
100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
71	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	86	VDD
72	SDO1/OC1/INT0/RD0	87	ETXD1/PMD11/RF0
73	SOSCI/CN1/RC13	88	ETXD0/PMD10/RF1
74	SOSCO/T1CK/CN0/RC14	89	ETXERR/PMD9/RG1
75	VSS	90	PMD8/RG0
76	OC2/RD1	91	TRCLK/RA6
77	OC3/RD2	92	TRD3/RA7
78	OC4/RD3	93	PMD0/RE0
79	ETXD2/IC5/PMD12/RD12	94	PMD1/RE1
80	ETXD3/PMD13/CN19/RD13	95	TRD2/RG14
81	OC5/PMWR/CN13/RD4	96	TRD1/RG12
82	PMRD/CN14/RD5	97	TRD0/RG13
83	ETXEN/PMD14/CN15/RD6	98	PMD2/RE2
84	ETXCLK/PMD15/CN16/RD7	99	PMD3/RE3
85	VCAP/VDDCORE	100	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.

FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX564F128H, PIC32MX564F128L, PIC32MX664F128H, PIC32MX664F128L, PIC32MX764F128H AND PIC32MX764F128L DEVICES



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 2 **UFRCEN:** USB FRC Clock Enable bit
- 1 = Enable FRC as the clock source for the USB clock source
- 0 = Use the Primary Oscillator or USB PLL as the USB clock source

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Enable Secondary Oscillator
- 0 = Disable Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
- 1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
- 0 = Oscillator switch is complete

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

100000 = Center frequency -12.5% for PIC32MX575/595/675/695/775/795 devices
100000 = Center frequency -1.5% for PIC32MX534/564/664/764 devices
100001 =
•
•
•
111111 =
000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)
000001 =
•
•
•
011110 =
011111 = Center frequency +12.5% for PIC32MX575/595/675/695/775/795 devices
011111 = Center frequency +1.5% for PIC32MX534/564/664/764 devices

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 9-4: CHEMSK: CACHE TAG MASK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LMASK<10:3>							
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	LMASK<2:0>			—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Write '0'; ignore read

bit 15-5 **LMASK<10:0>:** Line Mask bits

1 = Enables mask logic to force a match on the corresponding bit position in LTAG<19:0> bits (CHETAG<23:4>) and the physical address

0 = Only writeable for values of CHEIDX<3:0> bits (CHEACC<3:0>) equal to 0x0A and 0x0B (disables mask logic)

bit 4-0 **Unimplemented:** Write '0'; ignore read

REGISTER 9-5: CHEW0: CACHE WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW0<31:0>:** Word 0 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
Readable only if the device is not code-protected.

10.1 Control Registers

TABLE 10-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	DMACH<2:0>(2)			0000
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: DMACH<3> bit is not available on PIC32MX534/564/664/764 devices.

TABLE 10-2: DMA CRC REGISTER MAP(1)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
3040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
3050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 10-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All other modes:
Unused.

REGISTER 20-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON(1)	—	SIDL	IREN	RTSMD	—	UEN<1:0>	
7:0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:		HC = Cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit(1)
- 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits.
- 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal.

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation when device enters Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
- 1 = Wake-up is enabled
- 0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

Note 1: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 21-5: PMSTAT: PARALLEL PORT STATUS REGISTER (ONLY SLAVE MODES)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HS = Set by Hardware	SC = Cleared by software	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
- 0 = An overflow has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits
- 1 = Input buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = An underflow has not occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

REGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	—	—	SAMC<4:0>(1)				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
	ADCS<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = Clock derived from FRC
0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits(2)
11111111 = TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD
•
•
•
00000001 = TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD
00000000 = TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
2: This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

Table 25-1, Table 25-2, Table 25-3 and Table 25-4 show four interfaces and the associated pins that can be used with the Ethernet Controller.

TABLE 25-1: MII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXCLK	Transmit Clock
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
ETXD2	Transmit Data
ETXD3	Transmit Data
ETXERR	Transmit Error
ERXCLK	Receive Clock
ERXDV	Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXD2	Receive Data
ERXD3	Receive Data
ERXERR	Receive Error
ECRS	Carrier Sense
ECOL	Collision Indication

TABLE 25-2: RMII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
EREFCLK	Reference Clock
ECRSDV	Carrier Sense – Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXERR	Receive Error

Note: Ethernet controller pins that are not used by selected interface can be used by other peripherals.

TABLE 25-3: MII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 0)

Pin Name	Description
AEMDC	Management Clock
AEMDIO	Management I/O
AETXCLK	Transmit Clock
AETXEN	Transmit Enable
AETXD0	Transmit Data
AETXD1	Transmit Data
AETXD2	Transmit Data
AETXD3	Transmit Data
AETXERR	Transmit Error
AERXCLK	Receive Clock
AERXDV	Receive Data Valid
AERXD0	Receive Data
AERXD1	Receive Data
AERXD2	Receive Data
AERXD3	Receive Data
AERXERR	Receive Error
AECRS	Carrier Sense
AECOL	Collision Indication

Note: The MII mode Alternate Interface is not available on 64-pin devices.

TABLE 25-4: RMII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 0)

Pin Name	Description
AEMDC	Management Clock
AEMDIO	Management I/O
AETXEN	Transmit Enable
AETXD0	Transmit Data
AETXD1	Transmit Data
AEREFCLK	Reference Clock
AECRSDV	Carrier Sense – Receive Data Valid
AERXD0	Receive Data
AERXD1	Receive Data
AERXERR	Receive Error

REGISTER 25-29: EMAC1SUPP: ETHERNET CONTROLLER MAC PHY SUPPORT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
	—	—	—	—	RESETRMII(1)	—	—	SPEEDRMII(1)
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMII:** Reset RMII Logic bit(1)
1 = Reset the MAC RMII module
0 = Normal operation.

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPEEDRMII:** RMII Speed bit(1)
This bit configures the Reduced MII logic for the current operating speed.
1 = RMII is running at 100 Mbps
0 = RMII is running at 10 Mbps

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is only used for the RMII module.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 26-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	C2OUT	C1OUT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = All Comparator modules are disabled while in Idle mode
- 0 = All Comparator modules continue to operate while in Idle mode

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **C2OUT:** Comparator Output bit
- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit
- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

29.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 33. "Programming and Diagnostics"** (DS60001129) in the *"PIC32 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MX5XX/6XX/7XX family of devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. Key features include:

- Flexible device configuration
- Watchdog Timer (WDT)
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

29.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- DEVID: Device and Revision ID Register

TABLE 32-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O Pins:					
		with TTL Buffer	VSS	—	0.15 VDD	V	
		with Schmitt Trigger Buffer	VSS	—	0.2 VDD	V	
DI15		$\overline{MCLR}$(2)	VSS	—	0.2 VDD	V	
DI16		OSC1 (XT mode)	VSS	—	0.2 VDD	V	**(Note 4)**
DI17		OSC1 (HS mode)	VSS	—	0.2 VDD	V	**(Note 4)**
DI18		SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	VSS	—	0.8	V	SMBus enabled **(Note 4)**
	VIH	**Input High Voltage**					
DI20		I/O Pins not 5V-tolerant(5)	0.65 VDD	—	VDD	V	**(Note 4,6)**
		I/O Pins 5V-tolerant with PMP(5)	0.25 VDD + 0.8V	—	5.5	V	**(Note 4,6)**
		I/O Pins 5V-tolerant(5)	0.65 VDD	—	5.5	V	
DI28		SDAx, SCLx	0.65 VDD	—	5.5	V	SMBus disabled **(Note 4,6)**
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)**
DI30	ICNPU	**Change Notification Pull-up Current**	—	—	-50	µA	VDD = 3.3V, VPIN = VSS **(Note 3,6)**
DI31	ICNPD	**Change Notification Pull-down Current(4)**	—	50	—	µA	VDD = 3.3V, VPIN = VDD

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the **"Device Pin Tables"** section for the 5V-tolerant pins.

6: The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.

7: VIL source < (VSS - 0.3). Characterized but not tested.

8: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

9: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

10: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

11: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 8**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

32.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX5XX/6XX/7XX AC characteristics and timing parameters.

FIGURE 32-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

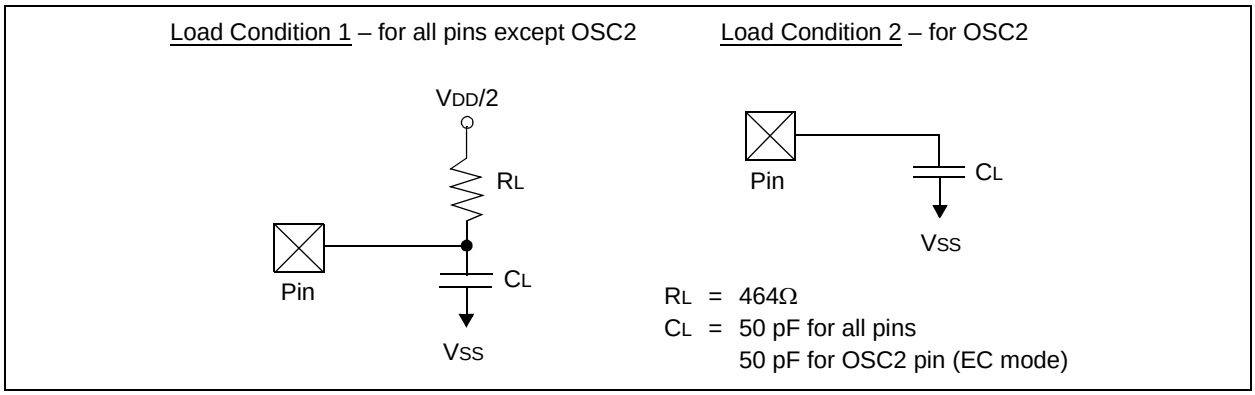


TABLE 32-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO50	Cosco	OSC2 pin	—	—	15	pF	In XT and HS modes when an external crystal is used to drive OSC1
DO56	CIO	All I/O pins and OSC2	—	—	50	pF	In EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 32-2: EXTERNAL CLOCK TIMING

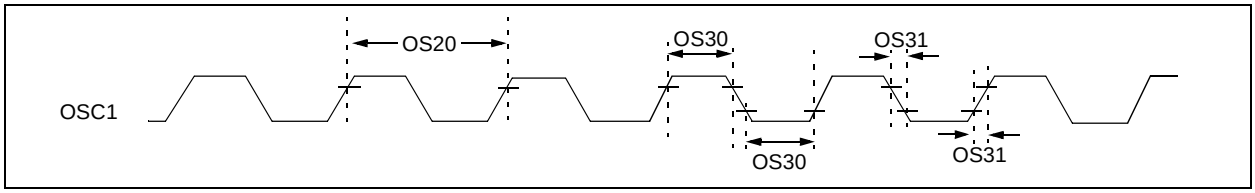


TABLE 32-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**		**Min.**	**Max.**	**Units**	**Conditions**	
TB10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter TB15	
TB15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of [(25 ns or 2 TPB)/N] + 30 ns	—	ns	VDD > 2.7V	
				[(Greater of [(25 ns or 2 TPB)/N] + 50 ns	—	ns	VDD < 2.7V	
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPB	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 32-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

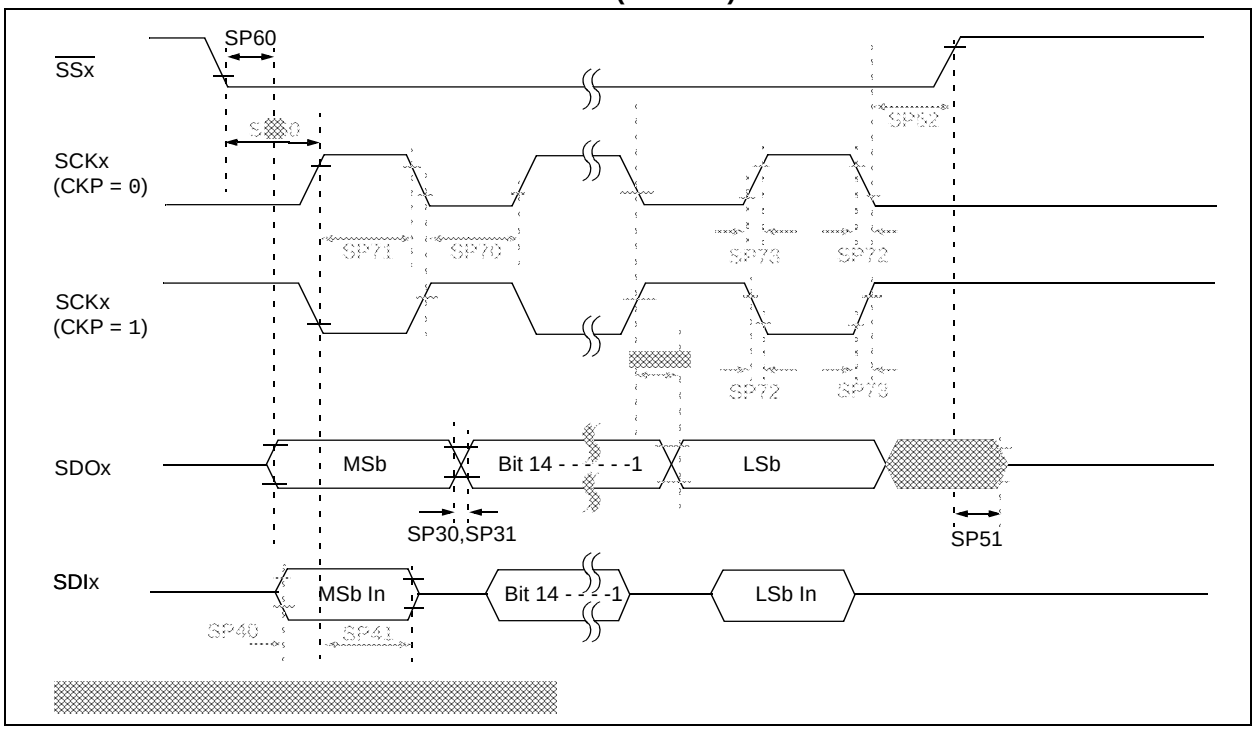


TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	5	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	5	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	20	ns	VDD > 2.7V
			—	—	30	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	175	—	—	ns	—

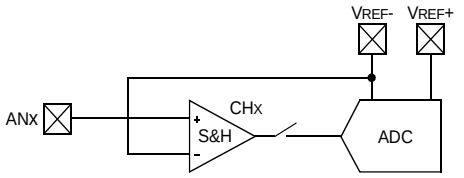
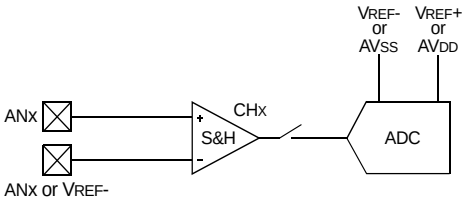
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

TABLE 32-37: 10-BIT ADC CONVERSION RATE PARAMETERS

Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp					
ADC Speed(2)	**TAD Minimum**	**Sampling Time Minimum**	**RS Maximum**	**VDD**	**ADC Channels Configuration**
1 Msps to 400 ksps(1)	65 ns	132 ns	500Ω	3.0V to 3.6V	
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	

Note 1: External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.

3: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

Revision J (September 2016)

This revision includes typographical and formatting updates throughout the data sheet text. In addition, all SFR Register maps were moved from the Memory chapter to their respective peripheral chapters.

All other major updates are referenced by their respective section in Table B-7.

TABLE B-7: MAJOR SECTION UPDATES

Section Name	Update Description
"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet"	Updated Communication Interfaces for LIN support to 2.1. Updated Qualification and Class B Support to AEC-Q100 REVH.
2.0 "Guidelines for Getting Started with 32-bit MCUs"	The Recommended Minimum Connection diagram was updated (see Figure 2-1). The Example of $\overline{\text{MCLR}}$ Pin Connections diagram was updated (see Figure 2-2). **2.11 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations"** was added.
4.0 "Memory Organization"	The SFR Memory Map was added (see Table 4-1).
7.0 "Interrupt Controller"	The UART interrupt sources were updated in the Interrupt IRQ, Vector, and Bit location table (see Table 7-1).
8.0 "Oscillator Configuration"	Updated the bit value definitions for the TUN<5:0> bits in the OCSTUN register (see Register 8-2).
15.0 "Watchdog Timer (WDT)"	The content in this chapter was relocated from the Special Features chapter to its own chapter.
18.0 "Serial Peripheral Interface (SPI)"	The register map tables were combined (see Table 18-1).
19.0 "Inter-Integrated Circuit (I^2C)"	The register map tables were combined (see Table 19-1). The PMADDR register was updated (see Register 21-3).
21.0 "Parallel Master Port (PMP)"	The bit value definitions for the ADRMUX<1:0> and CSF<1:0> bits in the PMCON register were updated (see Register 21-1).
29.0 "Special Features"	Removed the duplicate bit value definition for '010' in the DEVCFG2 register (see Register 29-3). Note 1 was added to the Programming, Debugging, and Trace Ports block diagram (see Figure 29-2). The DDPCON register was relocated (see Register 29-6). The Device ID, Revision, and Configuration Summary was updated (see Table 29-2).