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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx764f128l-v-pt

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		Pin Nun	nber <sup>(1)</sup>		<b>D</b> .				
Pin Name	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA	Pin Type	Buffer Type	Description		
AECRS		41	J7	B23	1	ST	Alternate Ethernet carrier sense <sup>(2)</sup>		
AEMDC	30	71	C11	A46	0	_	Alternate Ethernet Management Data clock <sup>(2)</sup>		
AEMDIO	49	68	E9	B37	I/O		Alternate Ethernet Management Data <sup>(2)</sup>		
TRCLK	—	91	C5	B51	0	—	Trace clock		
TRD0	—	97	A3	B55	0	—	Trace Data bits 0-3		
TRD1	_	96	C3	A65	0				
TRD2	—	95	C4	B54	0				
TRD3	—	92	B5	A62	0	—			
PGED1	16	25	K2	B14	I/O	ST	Data I/O pin for Programming/ Debugging Communication Channel 1		
PGEC1	15	24	K1	A15	I	ST	Clock input pin for Programming/ Debugging Communication Channel 1		
PGED2	18	27	J3	B16	I/O	ST	Data I/O pin for Programming/ Debugging Communication Channel 2		
PGEC2	17	26	L1	A20	I	ST	Clock input pin for Programming/ Debugging Communication Channel 2		
MCLR	7	13	F1	B7	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.		
AVdd	19	30	J4	A22	Р	Р	Positive supply for analog modules. This pin must be connected at all times.		
AVss	20	31	L3	B18	Р	Р	Ground reference for analog modules		
Vdd	10, 26, 38, 57	2, 16, 37, 46, 62, 86	A7, C2, C9, E5, K8, F8, G5, H4, H6	A10, A14, A30, A41, A48, A59, B1, B21, B53	Ρ	_	Positive supply for peripheral logic and I/O pins		
VCAP	56	85	B7	B48	Р		Capacitor for Internal Voltage Regulator		
Vss	9, 25, 41	15, 36, 45, 65, 75	A8, B10, D4, D5, E7, F5, F10, G6, G7, H3	A3, A25, A43, A63, B8, B12, B25, B41, B46	Ρ	_	Ground reference for logic and I/O pins. This pin must be connected at all times.		
VREF+	16	29	K3	B17	I	Analog	Analog voltage reference (high) input		
VREF-	15	28	L2	A21	I	Analog	Analog voltage reference (low) input		
Legend: C	.egend:       CMOS = CMOS compatible input or output       Analog = Analog input       P = Power         ST = Schmitt Trigger input with CMOS levels       O = Output       I = Input								

# TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

TTL = TTL input buffer
Note 1: Pin numbers are only provided for reference. See the "Device Pin Tables" section for device pin availability.

2: See 25.0 "Ethernet Controller" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
04.04	R	R	R	R	R	R	R	R					
31:24	BMXDRMSZ<31:24>												
22.16	R	R	R	R	R	R	R	R					
23.10	BMXDRMSZ<23:16>												
45.0	R	R	R	R	R	R	R	R					
15:8	BMXDRMSZ<15:8>												
7.0	R	R	R	R	R	R	R	R					
7:0				BMXDR	MSZ<7:0>								

## REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXDRMSZ<31:0>:** Data RAM Memory (DRM) Size bits Static value that indicates the size of the Data RAM in bytes: 0x00004000 = device has 16 KB RAM 0x00008000 = device has 32 KB RAM 0x00010000 = device has 64 KB RAM

# REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER<sup>(1,2)</sup>

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
31:24	—	—	—	—	—	—	—	—					
22.16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0					
23:16	—	—	—	— — ВМХРUРВА<19:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0					
15:8	BMXPUPBA<15:8>												
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
7:0				BMXPU	PBA<7:0>								

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 Unimplemented: Read as '0'

bit 19-11 BMXPUPBA<19:11>: Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>:** Program Flash (PFM) User Program Base Address Read-Only bits Value is always '0', which forces 2 KB increments

- **Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.
  - **2:** The value in this register must be less than or equal to BMXPFMSZ.

# 6.1 Control Registers

## TABLE 6-1: RESETS REGISTER MAP

ess										Bi	ts								(2)
Virtual Addr (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E000	DCON	31:16		—	—	—	—		—	—		—	—		—	—	-	—	0000
F600	RCON	15:0	_	_	_	-	-	_	CMR	VREGS	EXTR	SWR	_	WDTO	SLEEP	IDLE	BOR	POR	0000
E610	DOWDOT	31:16	_	_	_	-	-	_	_	_	_	_	_	_	-	_	_	_	0000
FOIU	ROWROI	15:0		_	-	-	_		-		-	_		-	_	-	_	SWRST	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

		Vector		Interru	ot Bit Location	
Interrupt Source <sup>(1)</sup>	Number	Number	Elog	Enable	Priority	Sub Briarity
		07	Flay			
AD1 – ADC1 Convert Done	33	27	IFS1<1>	IEC1<1>	IPC6<28:26>	IPC6<25:24>
PMP – Parallel Master Port	34	28	IFS1<2>	IEC1<2>	IPC7<4:2>	IPC7<1:0>
CMP1 – Comparator Interrupt	35	29	IFS1<3>	IEC1<3>	IPC7<12:10>	IPC7<9:8>
CMP2 – Comparator Interrupt	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>
U2E – UAR I2 Error SPI2E – SPI2 Fault I2C4B – I2C4 Bus Collision Event	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>
U2RX – UART2 Receiver SPI2RX – SPI2 Receive Done I2C4S – I2C4 Slave Event	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>
U2TX – UART2 Transmitter SPI2TX – SPI2 Transfer Done IC4M – I2C4 Master Event	39	31	IFS1<7>	IEC1<7>	IPC7<28:26>	IPC7<25:24>
U3E – UART3 Error SPI4E – SPI4 Fault I2C5B – I2C5 Bus Collision Event	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>
U3RX – UART3 Receiver SPI4RX – SPI4 Receive Done I2C5S – I2C5 Slave Event	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>
U3TX – UART3 Transmitter SPI4TX – SPI4 Transfer Done IC5M – I2C5 Master Event	42	32	IFS1<10>	IEC1<10>	IPC8<4:2>	IPC8<1:0>
I2C2B – I2C2 Bus Collision Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>
I2C2S – I2C2 Slave Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>
I2C2M – I2C2 Master Event	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>
FSCM – Fail-Safe Clock Monitor	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>
RTCC – Real-Time Clock and Calendar	47	35	IFS1<15>	IEC1<15>	IPC8<28:26>	IPC8<25:24>
DMA0 – DMA Channel 0	48	36	IFS1<16>	IEC1<16>	IPC9<4:2>	IPC9<1:0>
DMA1 – DMA Channel 1	49	37	IFS1<17>	IEC1<17>	IPC9<12:10>	IPC9<9:8>
DMA2 – DMA Channel 2	50	38	IFS1<18>	IEC1<18>	IPC9<20:18>	IPC9<17:16>
DMA3 – DMA Channel 3	51	39	IFS1<19>	IEC1<19>	IPC9<28:26>	IPC9<25:24>
DMA4 – DMA Channel 4	52	40	IFS1<20>	IEC1<20>	IPC10<4:2>	IPC10<1:0>
DMA5 – DMA Channel 5	53	41	IFS1<21>	IEC1<21>	IPC10<12:10>	IPC10<9:8>
DMA6 – DMA Channel 6	54	42	IFS1<22>	IEC1<22>	IPC10<20:18>	IPC10<17:16>
DMA7 – DMA Channel 7	55	43	IFS1<23>	IEC1<23>	IPC10<28:26>	IPC10<25:24>
FCE – Flash Control Event	56	44	IFS1<24>	IEC1<24>	IPC11<4:2>	IPC11<1:0>
USB – USB Interrupt	57	45	IFS1<25>	IEC1<25>	IPC11<12:10>	IPC11<9:8>
CAN1 – Control Area Network 1	58	46	IFS1<26>	IEC1<26>	IPC11<20:18>	IPC11<17:16>
CAN2 – Control Area Network 2	59	47	IFS1<27>	IEC1<27>	IPC11<28:26>	IPC11<25:24>
ETH – Ethernet Interrupt	60	48	IFS1<28>	IEC1<28>	IPC12<4:2>	IPC12<1:0>
IC1E – Input Capture 1 Error	61	5	IFS1<29>	IEC1<29>	IPC1<12:10>	IPC1<9:8>
IC2E – Input Capture 2 Error	62	9	IFS1<30>	IEC1<30>	IPC2<12:10>	IPC2<9:8>

## TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX5XX USB and CAN Features", TABLE 2: "PIC32MX6XX USB and Ethernet Features" and TABLE 3: "PIC32MX7XX USB, Ethernet, and CAN Features" for the list of available peripherals.

## REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
  - 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
  - 0 = No interrupt is pending
- bit 4 CHDHIF: Channel Destination Half Full Interrupt Flag bit
  - 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
     0 = No interrupt is pending

#### bit 3 CHBCIF: Channel Block Transfer Complete Interrupt Flag bit

- 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
- 0 = No interrupt is pending

## bit 2 CHCCIF: Channel Cell Transfer Complete Interrupt Flag bit

- 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
- 0 = No interrupt is pending
- bit 1 CHTAIF: Channel Transfer Abort Interrupt Flag bit
  - 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
  - 0 = No interrupt is pending

## bit 0 CHERIF: Channel Address Error Interrupt Flag bit

- 1 = A channel address error has been detected (either the source or the destination address is invalid)
- 0 = No interrupt is pending

# TABLE 11-1: USB REGISTER MAP (CONTINUED)

ess				Bits															
Virtual Addr (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5280	LI1ERMI (3)	31:16	_	_	—	—	—	_	—	_	—	—	_	—	_	_	—	—	0000
5200	OTINIE	15:0	—	—	—	—	—	—	—	—				FRML<	7:0>				0000
5290	U1FRMH <sup>(3)</sup>	31:16	—	_	—	—	_	—	—	_	_	—	—	—	_	_	—	—	0000
0200	0	15:0	—	_	_	-	-	_	—	—	_	-	_	—	_		FRMH<2:0>		0000
52A0	U1TOK	31:16	—	_	—	—	_	—	—	_	_	—	_	—	_	—	—	—	0000
02/10	onok	15:0	—	—	—	—	—	_	—	—		PID<	:3:0>			EP	<3:0>		0000
52P0		31:16	_	-	—	—	—	_	—	—	_	—	—	—	_	_	—	—	0000
5260	0130F	15:0	-		-	_	_		_	_				CNT<7	<b>'</b> :0>				0000
5000		31:16			-	-	_		_	_		—	—	—			_	_	0000
5200	UIBDIP2	15:0	-		-	_	_		_	_				BDTPTRF	H<7:0>				0000
5200		31:16		-	—	_	_		_	_	_	—	_	—	-	-	—	—	0000
52D0	UIBDIP3	15:0	_			_	—			_				BDTPTRU	J<7:0>				0000
5250		31:16		-	—	_	_		_	_	_	—	_	—	-	-	—	—	0000
52EU	UTCINFGT	15:0		_	_	-	-	_	_	_	UTEYE	UOEMON	_	USBSIDL	_	_	_	UASUSPND	0001
5200		31:16	-	_	_	-	_	_	-	_	_	—	_	—	—	_	—	_	0000
5300	UTEPU	15:0		_	_	-	-	_	_	_	LSPD	RETRYDIS	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
524.0		31:16	-	_	-	-	-	_	_	_	_	-	_	_	_	_	_	_	0000
5310	UTEPT	15:0	_	_	_	_	_	_	_		—	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	-	_	-	-	-	_	_	_	_	-	_	_	_	_	_	_	0000
5320	UTEP2	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	_	_	_	_	_	_	_		—	—	_	—	_	_	—	—	0000
5330	UTEP3	15:0		_	_	-	-	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5240		31:16	-	_	-	-	-	_	_	_	_	-	_	_	_	_	_	_	0000
5540	UIEP4	15:0	-	_	-	-	_	_	-	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5250		31:16		_	_	-	-	_	_	_	_	—	_	—	_	_	_	_	0000
5350	UIEP5	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	_	_	_	_	_	_	_	_	—	_	_	—	_	_	—	_	0000
5360	UIEPo	15:0	-	_	-	-	-	_	_	_	_	-	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5070		31:16	_	_	_	_	_	_	_	_	_	_	_	—	_	_	_	_	0000
5370	U1EP7	15:0	_		_	_	_		_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	_	_	_	_	_	_	—	_	_	_	_	—	—	—	—	—	0000
5380	U1EP8	15:0	_	_	_	_	_	_	_	_	_		_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
		31:16		_	_	_	_	_	—	_	_	_	_	—	—	_		_	0000
5390	U1EP9	15:0	_	_	_	_	_	_	—	—	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

 5390
 U1EP9

 Legend:
 x =

 Note
 1:
 All n

end: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—		—			—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—		—			_	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—		—			_	_
7.0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	LSPD	RETRYDIS		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK

## REGISTER 11-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER

#### Legend:

bit 1

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## bit 31-8 Unimplemented: Read as '0'

- bit 7 LSPD: Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)
  - 1 = Direct connection to a low-speed device enabled
  - 0 = Direct connection to a low-speed device disabled; hub required with PRE\_PID
- bit 6 **RETRYDIS:** Retry Disable bit (Host mode and U1EP0 only)
  - 1 = Retry NACK'd transactions disabled
  - 0 = Retry NACK'd transactions enabled; retry done in hardware
- bit 5 Unimplemented: Read as '0'
- bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
  - If EPTXEN = 1 and EPRXEN = 1:
  - 1 = Disable Endpoint 'n' from control transfers; only TX and RX transfers are allowed
  - 0 = Enable Endpoint 'n' for control (SETUP) transfers; TX and RX transfers are also allowed Otherwise, this bit is ignored.
- bit 3 EPRXEN: Endpoint Receive Enable bit
  - 1 = Endpoint 'n' receive is enabled
  - 0 = Endpoint 'n' receive is disabled
- bit 2 EPTXEN: Endpoint Transmit Enable bit
  - 1 = Endpoint 'n' transmit is enabled
  - 0 = Endpoint 'n' transmit is disabled
  - EPSTALL: Endpoint Stall Status bit
  - 1 = Endpoint 'n' was stalled
  - 0 = Endpoint 'n' was not stalled
- bit 0 **EPHSHK:** Endpoint Handshake Enable bit
  - 1 = Endpoint Handshake is enabled
  - 0 = Endpoint Handshake is disabled (typically used for isochronous endpoints)

# PIC32MX5XX/6XX/7XX

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
15:8	ON <sup>(1)</sup>	—	SIDL	IREN	RTSMD	—	UEN	<1:0>
7.0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL	_<1:0>	STSEL

## **REGISTER 20-1: UXMODE: UARTX MODE REGISTER**

Legend:		HC = Cleared by hard	HC = Cleared by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

## bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** UARTx Enable bit<sup>(1)</sup>
  - 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits.
  - 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal.
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
  - 1 = Discontinue operation when device enters Idle mode
  - 0 = Continue operation when device enters Idle mode
- bit 12 IREN: IrDA Encoder and Decoder Enable bit
  - 1 = IrDA is enabled
  - 0 = IrDA is disabled
- bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit
  - $1 = \overline{\text{UxRTS}}$  pin is in Simplex mode
  - $0 = \overline{\text{UxRTS}}$  pin is in Flow Control mode
- bit 10 Unimplemented: Read as '0'
- bit 9-8 UEN<1:0>: UARTx Enable bits
  - 11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
  - 10 = UxTX, UxRX,  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$  pins are enabled and used
  - 01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
  - 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register
- bit 7 WAKE: Enable Wake-up on Start bit Detect During Sleep Mode bit
  - 1 = Wake-up is enabled
  - 0 = Wake-up is disabled
- bit 6 LPBACK: UARTx Loopback Mode Select bit
  - 1 = Loopback mode is enabled
  - 0 = Loopback mode is disabled
- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

- bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)
  - 1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
  - 0 = Normal operation, buffer contents will be overwritten by the next conversion sequence
- bit 3 Unimplemented: Read as '0'
- bit 2 ASAM: ADC Sample Auto-Start bit
  - 1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
  - 0 = Sampling begins when SAMP bit is set
- bit 1 SAMP: ADC Sample Enable bit<sup>(2)</sup>
  - 1 = The ADC S&H circuit is sampling
  - 0 = The ADC S&H circuit is holding
  - When ASAM = 0, writing '1' to this bit starts sampling.
  - When SSRC < 2:0 > = 000, writing '0' to this bit will end sampling and start conversion.

## bit 0 **DONE:** Analog-to-Digital Conversion Status bit<sup>(3)</sup>

- Clearing this bit will not affect any operation in progress.
  - 1 = Analog-to-digital conversion is done
  - 0 = Analog-to-digital conversion is not done or has not started
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write a '0' to end sampling and start conversion. If SSRC<2:0> ≠ '000', this bit is automatically cleared by hardware to end sampling and start conversion.
  - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

## REGISTER 24-14: CIFLTCON4: CAN FILTER CONTROL REGISTER 4 (CONTINUED)

bit 15	FLTEN17: Filter 13 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 14-13	MSEL17<1:0>: Filter 17 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask U selected
bit 12-8	FSEL17<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 7	FLTEN16: Filter 16 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 6-5	MSEL16<1:0>: Filter 16 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 4-0	FSEL16<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

# PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24	FLTEN27	MSEL2	27<1:0> FSEL27<4:0>		FSEL27<4:0>				
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	FLTEN26	MSEL26<1:0>		FSEL26<4:0>					
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15.6	FLTEN25	MSEL25<1:0>		FSEL25<4:0>					
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0	FLTEN24	MSEL2	24<1:0>		FSEL24<4:0>				

## REGISTER 24-16: CIFLTCON6: CAN FILTER CONTROL REGISTER 6

## Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31	FLTEN27: Filter 27 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL27<1:0>: Filter 27 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
hit 20 24	
DIL 20-24	<b>FSEL2/&lt;4.0&gt;.</b> FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buller 31
	• •
	•
	00001 = Message matching filter is stored in FIFO buffer 1
hit 00	ELTEN26. Eiter 26 Enchlo bit
DIL 23	FLIENZO. FIREI ZO ENADIE DI
	0 = Filter is disabled
bit 22-21	MSEL26<1:0>: Filter 26 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 20-16	FSEL26<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—	—	—	—	—	_	_	
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	BUFCNT<7:0>								
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15.0	—	—	—	—	—	—	-		
7.0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
7.0	ETHBUSY <sup>(1)</sup>	TXBUSY <sup>(2)</sup>	RXBUSY <sup>(2)</sup>	_	_	_	_	_	
	•	•	•	•	•				

# REGISTER 25-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

# Legend:

Logena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## bit 31-24 Unimplemented: Read as '0'

## bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x000. When software attempts to decrement the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

- **Note:** BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.
- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 ETHBUSY: Ethernet Module busy bit<sup>(1)</sup>

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction 0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

- bit 6 **TXBUSY:** Transmit Busy bit<sup>(2)</sup>
  - 1 = TX logic is receiving data
  - 0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

- **Note 1:** This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
  - **2:** This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

# REGISTER 25-22: ETHALGNERR: ETHERNET CONTROLLER ALIGNMENT ERRORS STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	ALGNERRCNT<15:8>								
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0				ALGNERR	CNT<7:0>				

# Legend:

Logona.					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

## bit 31-16 Unimplemented: Read as '0'

bit 15-0 ALGNERRCNT<15:0>: Alignment Error Count bits

Increment count for frames with alignment errors. Note that an alignment error is a frame that has an FCS error and the frame length in bits is not an integral multiple of 8 bits (a.k.a., dribble nibble)

## **Note 1:** This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

## REGISTER 25-26: EMAC1IPGR: ETHERNET CONTROLLER MAC NON-BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—	—	—	—	—	—	—	
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
15.0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	
0.61	—	NB2BIPKTGP1<6:0>							
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	
7.0				NB2E	BIPKTGP2<6:	0>			

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

## bit 31-15 Unimplemented: Read as '0'

## bit 14-8 NB2BIPKTGP1<6:0>: Non-Back-to-Back Interpacket Gap Part 1 bits

This is a programmable field representing the optional carrierSense window referenced in section 4.2.3.2.1 "Deference" of the IEEE 80.23 Specification. If the carrier is detected during the timing of IPGR1, the MAC defers to the carrier. If, however, the carrier comes after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision, thus ensuring fair access to the medium. Its range of values is 0x0 to IPGR2. Its recommend value is 0xC (12d).

#### bit 7 Unimplemented: Read as '0'

# bit 6-0 NB2BIPKTGP2<6:0>: Non-Back-to-Back Interpacket Gap Part 2 bits

This is a programmable field representing the non-back-to-back Inter-Packet-Gap. Its recommended value is 0x12 (18d), which represents the minimum IPG of 0.96  $\mu$ s (in 100 Mbps) or 9.6  $\mu$ s (in 10 Mbps).

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

## REGISTER 25-33: EMAC1MADR: ETHERNET CONTROLLER MAC MII MANAGEMENT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	_	_	_	—		_	_	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	_	
15.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	
15.0	—	—	—		PHYADDR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0			_		RE	GADDR<4:0	)>		

## Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## bit 31-13 Unimplemented: Read as '0'

- bit 12-8 **PHYADDR<4:0>:** MII Management PHY Address bits This field represents the 5-bit PHY Address field of Management cycles. Up to 31 PHYs can be addressed (0 is reserved).
- bit 7-5 Unimplemented: Read as '0'
- bit 4-0 **REGADDR<4:0>:** MII Management Register Address bits This field represents the 5-bit Register Address field of Management cycles. Up to 32 registers can be accessed.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

DC CHA	RACTERIST	ICS	Standard (unless o Operating	Operating Conditions: 2.3Vtherwise stated)temperature $-40^{\circ}C \le TA \le +8$ $-40^{\circ}C \le TA \le +7$	<b>to 3.6V</b> 85°C for Ind 105°C for V-	ustrial Temp	
Param. No.	Typical <sup>(3)</sup>	Max.	Units	Conditions			
Operati	Operating Current (IDD) <sup>(1,2,4)</sup> for PIC32MX575/675/695/775/795 Family Devices						
DC20	6	9	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC		4 MHz
DC20b	7	10			+105⁰C		
DC20a	4	—		Code executing from SRAM			
DC21	37	40	mΔ	Code executing from Flash	_	_	25 MHz
DC21a	25	—		Code executing from SRAM			
DC22	64	70	m۸	Code executing from Flash		_	60 MHz
DC22a	61	—	IIIA	Code executing from SRAM	—		
DC23	85	98	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	_	80 MHz
DC23b	90	120			+105⁰C		
DC23a	85	_		Code executing from SRAM			
DC25a	125	150	μΑ	_	+25°C	3.3V	LPRC (31 kHz)

## TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

- 2: The test conditions for IDD measurements are as follows:
  - Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)</li>
  - OSC2/CLKO is configured as an I/O input pin
  - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
  - CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
  - No peripheral modules are operating, (ON bit = 0)
  - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
  - All I/O pins are configured as inputs and pulled to Vss
  - MCLR = VDD
  - CPU executing while(1) statement from Flash
  - RTCC and JTAG are disabled
- **3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.
- **4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

# 100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Chamfers at corners are optional; size may vary.
- 3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

# 121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimensior	l Limits	MIN	NOM	MAX
Contact Pitch	E1	0.80 BSC		
Contact Pitch	E2	0.80 BSC		
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D

# APPENDIX A: MIGRATING FROM PIC32MX3XX/4XX TO PIC32MX5XX/6XX/7XX DEVICES

This appendix provides an overview of considerations for migrating from PIC32MX3XX/4XX devices to the PIC32MX5XX/6XX/7XX family of devices. The code developed for the PIC32MX3XX/4XX devices can be ported to the PIC32MX5XX/6XX/7XX devices after making the appropriate changes outlined below.

# A.1 DMA

PIC32MX5XX/6XX/7XX devices do not support stopping DMA transfers in Idle mode.

# A.2 Interrupts

PIC32MX5XX/6XX/7XX devices have persistent interrupts for some of the peripheral modules. This means that the interrupt condition for these peripherals must be cleared before the interrupt flag can be cleared.

For example, to clear a UART receive interrupt, the user application must first read the UART Receive register to clear the interrupt condition and then clear the associated UXIF flag to clear the pending UART interrupt. In other words, the UXIF flag cannot be cleared by software until the UART Receive register is read.

Table A-1 outlines the peripherals and associated interrupts that are implemented differently on PIC32MX5XX/6XX/7XX versus PIC32MX3XX/4XX devices.

In addition, on the SPI module, the IRQ numbers for the receive done interrupts were changed from 25 to 24 and the transfer done interrupts were changed from 24 to 25.

# TABLE A-1: PIC32MX3XX/4XX VERSUS PIC32MX5XX/6XX/7XX INTERRUPT IMPLEMENTATION DIFFERENCES

Module	Interrupt Implementation
Input Capture	To clear an interrupt source, read the Buffer Result (ICxBUF) register to obtain the number of capture results in the buffer that are below the interrupt threshold (specified by ICI<1:0> bits).
SPI	Receive and transmit interrupts are controlled by the SRXISEL<1:0> and STXISEL<1:0> bits, respectively. To clear an interrupt source, data must be written to, or read from, the SPIxBUF register to obtain the number of data to receive/transmit below the level specified by the SRXISEL<1:0> and STXISEL<1:0> bits.
UART	TX interrupt will be generated as soon as the UART module is enabled. Receive and transmit interrupts are controlled by the URXISEL<1:0> and UTXISEL<1:0> bits, respectively. To clear an interrupt source, data must be read from, or written to, the UxRXREG or UxTXREG registers to obtain the number of data to receive/transmit below the level specified by the URXISEL<1:0> and UTXISEL<1:0> bits.
ADC	All samples must be read from the result registers (ADC1BUFx) to clear the interrupt source.
PMP	To clear an interrupt source, read the Parallel Master Port Data Input/Output (PMDIN/PMDOUT) register.