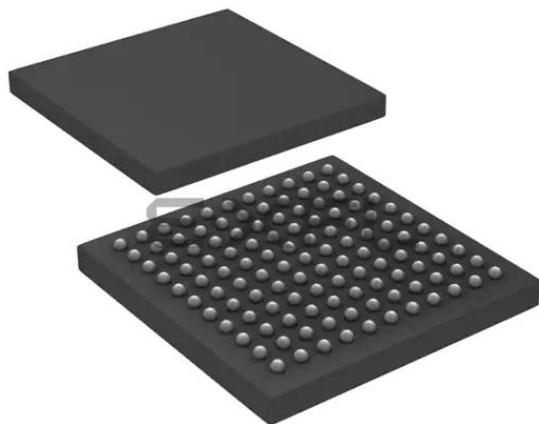




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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx764f128lt-i-bg

REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
BMXPFMSZ<31:24>								
23:16	R	R	R	R	R	R	R	R
BMXPFMSZ<23:16>								
15:8	R	R	R	R	R	R	R	R
BMXPFMSZ<15:8>								
7:0	R	R	R	R	R	R	R	R
BMXPFMSZ<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **BMXPFMSZ<31:0>**: Program Flash Memory (PFM) Size bits

Static value that indicates the size of the PFM in bytes:

0x00010000 = device has 64 KB Flash
0x00020000 = device has 128 KB Flash
0x00040000 = device has 256 KB Flash
0x00080000 = device has 512 KB Flash

REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
BMXBOOTSZ<31:24>								
23:16	R	R	R	R	R	R	R	R
BMXBOOTSZ<23:16>								
15:8	R	R	R	R	R	R	R	R
BMXBOOTSZ<15:8>								
7:0	R	R	R	R	R	R	R	R
BMXBOOTSZ<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **BMXBOOTSZ<31:0>**: Boot Flash Memory (BFM) Size bits

Static value that indicates the size of the Boot PFM in bytes:

0x00003000 = device has 12 KB boot Flash

TABLE 7-5: INTERRUPT REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L PIC32MX575F512L AND PIC32MX575F256L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>			—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000	
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>			—	—	—	T4IP<2:0>			T4IS<1:0>		0000	
10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>			—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000	
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>			—	—	—	T5IP<2:0>			T5IS<1:0>		0000	
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>			—	—	—	CNIP<2:0>			CNIS<1:0>		0000	
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>			—	—	—	U1IP<2:0>			U1IS<1:0>		0000	
															SPI3IP<2:0>			SPI3IS<1:0>			
															I2C3IP<2:0>			I2C3IS<1:0>			
1100	IPC7	31:16	—	—	—	U3IP<2:0>			U3IS<1:0>			—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000	
						SPI2IP<2:0>			SPI2IS<1:0>												
						I2C4IP<2:0>			I2C4IS<1:0>												
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>			—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000	
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>			—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000	
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>			—	—	—	U2IP<2:0>			U2IS<1:0>		0000	
															SPI4IP<2:0>			SPI4IS<1:0>			
															I2C5IP<2:0>			I2C5IS<1:0>			
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>			—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000	
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>			—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000	
1130	IPC10	31:16	—	—	—	DMA7IP<2:0> ⁽²⁾			DMA7IS<1:0> ⁽²⁾			—	—	—	DMA6IP<2:0> ⁽²⁾			DMA6IS<1:0> ⁽²⁾		0000	
		15:0	—	—	—	DMA5IP<2:0> ⁽²⁾			DMA5IS<1:0> ⁽²⁾			—	—	—	DMA4IP<2:0> ⁽²⁾			DMA4IS<1:0> ⁽²⁾		0000	
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		0000	
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>			—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000	
1150	IPC12	31:16	—	—	—	U5IP<2:0>			U5IS<1:0>			—	—	—	U6IP<2:0>			U6IS<1:0>		0000	
		15:0	—	—	—	U4IP<2:0>			U4IS<1:0>			—	—	—	—	—	—	—	—	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: These bits are not available on PIC32MX534/564 devices.

3: This register does not have associated CLR, SET, and INV registers.

PIC32MX5XX/6XX/7XX

REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RIPL<2:0> ⁽¹⁾		
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	VEC<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **RIPL<2:0>:** Requested Priority Level bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits⁽¹⁾

11111-00000 = The interrupt vector that is presented to the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single-vector mode.

REGISTER 7-3: TPTMR: TEMPORAL PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TPTMR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **TPTMR<31:0>:** Temporal Proximity Timer Reload bits

Used by the Temporal Proximity Timer as a reload value when the Temporal Proximity timer is triggered by an interrupt event.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
2: Reset value is dependent on DEVCFGx configuration.

PIC32MX5XX/6XX/7XX

REGISTER 9-1: CHECON: CACHE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	CHECOH
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DCSZ<1:0>	
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	PREFEN<1:0>		—	PFMWS<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-17 **Unimplemented:** Write '0'; ignore read

bit 16 **CHECOH:** Cache Coherency Setting on a PFM Program Cycle bit

1 = Invalidate all data and instruction lines

0 = Invalidate all data lines and instruction lines that are not locked

bit 15-10 **Unimplemented:** Write '0'; ignore read

bit 9-8 **DCSZ<1:0>:** Data Cache Size in Lines bits

Changing these bits causes all lines to be reinitialized to the "invalid" state.

11 = Enable data caching with a size of 4 lines

10 = Enable data caching with a size of 2 lines

01 = Enable data caching with a size of 1 line

00 = Disable data caching

bit 7-6 **Unimplemented:** Write '0'; ignore read

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits

11 = Enable predictive prefetch for both cacheable and non-cacheable regions

10 = Enable predictive prefetch only for non-cacheable regions

01 = Enable predictive prefetch only for cacheable regions

00 = Disable predictive prefetch

bit 3 **Unimplemented:** Write '0'; ignore read

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSLK Wait States bits

111 = Seven Wait states

110 = Six Wait states

101 = Five Wait states

100 = Four Wait states

011 = Three Wait states

010 = Two Wait states

001 = One Wait state

000 = Zero Wait state

10.1 Control Registers

TABLE 10-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	000
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	DMACH<2:0> ⁽²⁾			000
3020	DMAADDR	31:16	DMAADDR<31:0>																000
		15:0																	000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

2: DMACH<3> bit is not available on PIC32MX534/564/664/764 devices.

TABLE 10-2: DMA CRC REGISTER MAP⁽¹⁾

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	000	
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>		000	
3040	DCRCDATA	31:16	DCRCDATA<31:0>																000
		15:0																	000
3050	DCRCXOR	31:16	DCRCXOR<31:0>																000
		15:0																	000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
35F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

TABLE 12-7: PORTE REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	00FF
6110	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6130	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 12-8: PORTE REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
6110	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6130	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

PIC32MX5XX/6XX/7XX

FIGURE 19-1: I²C BLOCK DIAGRAM

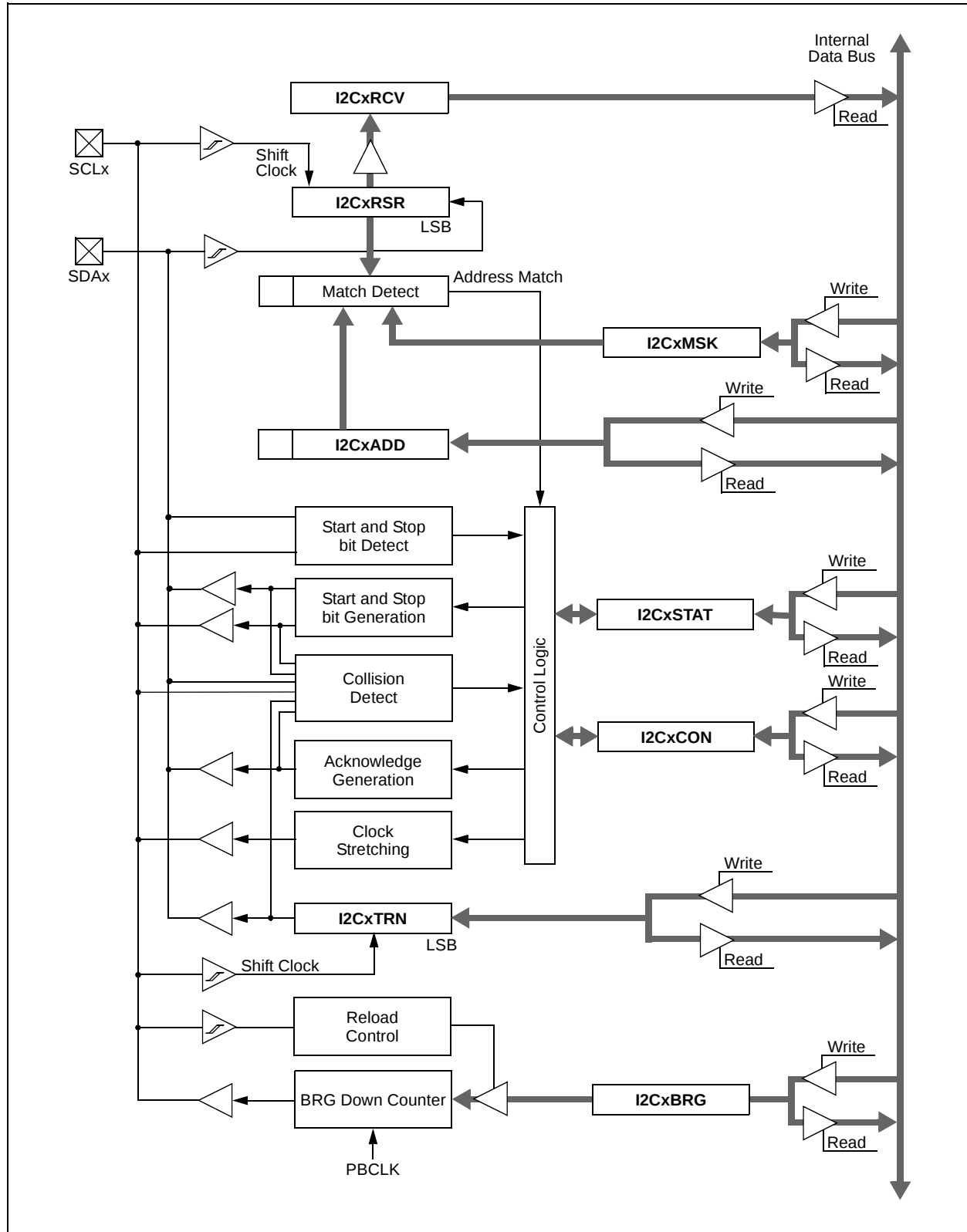


TABLE 24-1: CAN1 REGISTER SUMMARY FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B0F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>				FSEL15<4:0>			FLTEN14	MSEL14<1:0>			FSEL14<4:0>				0000
		15:0	FLTEN13	MSEL13<1:0>				FSEL13<4:0>			FLTEN12	MSEL12<1:0>			FSEL12<4:0>				0000
B100	C1FLTCON4	31:16	FLTEN19	MSEL19<1:0>				FSEL19<4:0>			FLTEN18	MSEL18<1:0>			FSEL18<4:0>				0000
		15:0	FLTEN17	MSEL17<1:0>				FSEL17<4:0>			FLTEN16	MSEL16<1:0>			FSEL16<4:0>				0000
B110	C1FLTCON5	31:16	FLTEN23	MSEL23<1:0>				FSEL23<4:0>			FLTEN22	MSEL22<1:0>			FSEL22<4:0>				0000
		15:0	FLTEN21	MSEL21<1:0>				FSEL21<4:0>			FLTEN20	MSEL20<1:0>			FSEL20<4:0>				0000
B120	C1FLTCON6	31:16	FLTEN27	MSEL27<1:0>				FSEL27<4:0>			FLTEN26	MSEL26<1:0>			FSEL26<4:0>				0000
		15:0	FLTEN25	MSEL25<1:0>				FSEL25<4:0>			FLTEN24	MSEL24<1:0>			FSEL24<4:0>				0000
B130	C1FLTCON7	31:16	FLTEN31	MSEL31<1:0>				FSEL31<4:0>			FLTEN30	MSEL30<1:0>			FSEL30<4:0>				0000
		15:0	FLTEN29	MSEL29<1:0>				FSEL29<4:0>			FLTEN28	MSEL28<1:0>			FSEL28<4:0>				0000
B140	C1RXFn (n = 0-31)	31:16	SID<10:0>											—	EXID	—	EID<17:16>	xxxx	
		15:0	EID<15:0>																xxxx
B340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0	C1FIFOBA<31:0>																0000
B350	C1FIFOCOn (n = 0-31)	31:16	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000	
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>	0000	
B360	C1FIFOINTn (n = 0-31)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
B370	C1FIFOUAn (n = 0-31)	31:16	C1FIFOUA<31:0>																0000
		15:0	C1FIFOUA<31:0>																0000
B380	C1FIFOCIn (n = 0-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 24-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>**: Propagation Time Segment bits⁽⁴⁾

111 = Length is 8 x T_Q

•
•
•

000 = Length is 1 x T_Q

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits⁽³⁾

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

111111 = T_Q = (2 x 64)/F_{SYS}

111110 = T_Q = (2 x 63)/F_{SYS}

•
•
•

000001 = T_Q = (2 x 2)/F_{SYS}

000000 = T_Q = (2 x 1)/F_{SYS}

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

2: 3 Time bit sampling is not allowed for BRP < 2.

3: SJW ≤ SEG2PH.

4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

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REGISTER 24-7: CîRXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **RXOVF<31:0>**: FIFO n Receive Overflow Interrupt Pending bit

1 = FIFO has overflowed
 0 = FIFO has not overflowed

REGISTER 24-8: CîTMR: CAN TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CANTS<15:0>**: CAN Time Stamp Timer bits

This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (CiCON<20>) is set.

bit 15-0 **CANTSPRE<15:0>**: CAN Time Stamp Timer Prescaler bits

1111 1111 1111 1111 = CAN time stamp timer (CANTS) increments every 65,535 system clocks

•
•
•

0000 0000 0000 0000 = CAN time stamp timer (CANTS) increments every system clock

Note 1: CîTMR will be paused when CANCAP = 0.

2: The CîTMR prescaler count will be reset on any write to CîTMR (CANTSPRE will be unaffected).

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REGISTER 24-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	TXNFULLIF ⁽¹⁾	TXHALFIF	TXEMPTYIF ⁽¹⁾
7:0	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
	—	—	—	—	RXOVFLIF	RXFULLIF ⁽¹⁾	RXHALFIF ⁽¹⁾	RXNEMPTYIF ⁽¹⁾

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit⁽¹⁾
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

Note 1: This bit is read-only and reflects the status of the FIFO.

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REGISTER 25-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR6<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR5<7:0>							

Legend:

R = Readable bit

-n = Value at POR

W = Writable bit

'1' = Bit is set

P = Programmable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits

These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits

These bits hold the fifth transmitted octet of the station address.

- Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.
- 2:** This register is loaded at reset from the factory preprogrammed station address.

PIC32MX5XX/6XX/7XX

NOTES:

29.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 33. “Programming and Diagnostics”** (DS60001129) in the *“PIC32 Family Reference Manual”*, which are available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MX5XX/6XX/7XX family of devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. Key features include:

- Flexible device configuration
- Watchdog Timer (WDT)
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

29.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

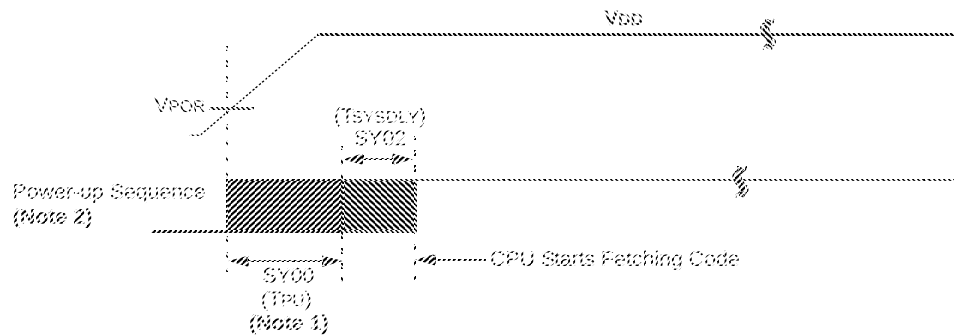
- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- DEVID: Device and Revision ID Register

PIC32MX5XX/6XX/7XX

FIGURE 32-4: POWER-ON RESET TIMING CHARACTERISTICS

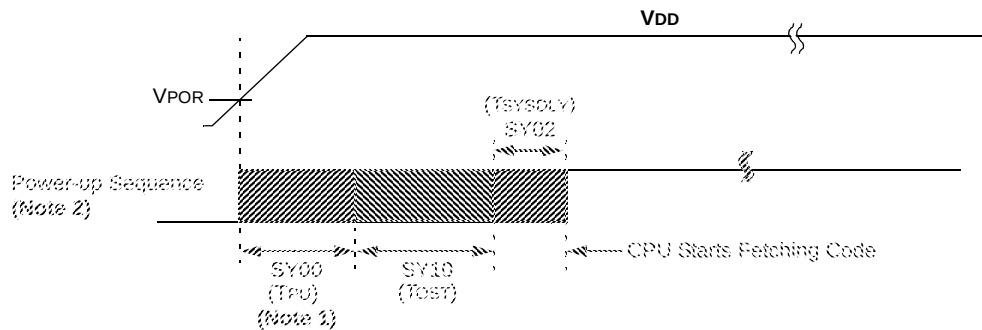
Internal Voltage Regulator Enabled

Clock Sources = {FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC}



Internal Voltage Regulator Enabled

Clock Sources = {NS, NSPLL, XT, XTPLL and Sosc}



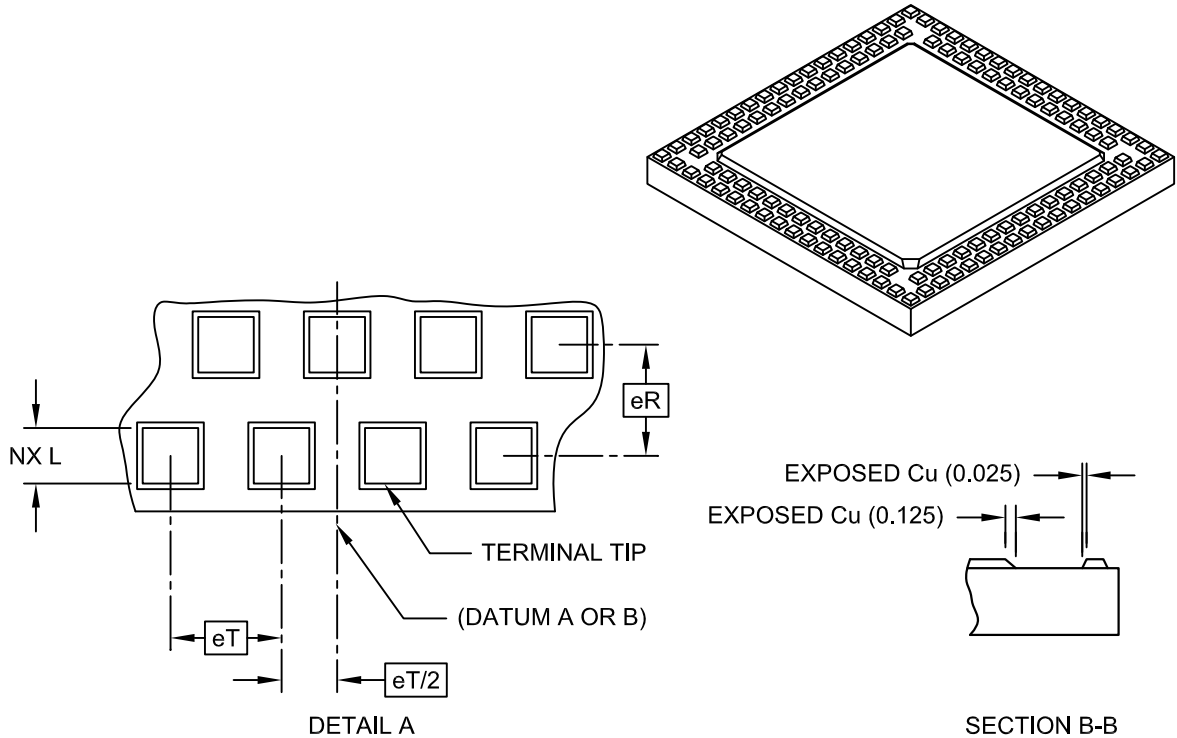
Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{DDMIN}$).

2: Includes interval voltage regulator stabilization delay.

PIC32MX5XX/6XX/7XX

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	124		
Pitch	eT	0.50 BSC		
Pitch (Inner to outer terminal ring)	eR	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	-	0.05
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	6.40	6.55	6.70
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	6.40	6.55	6.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

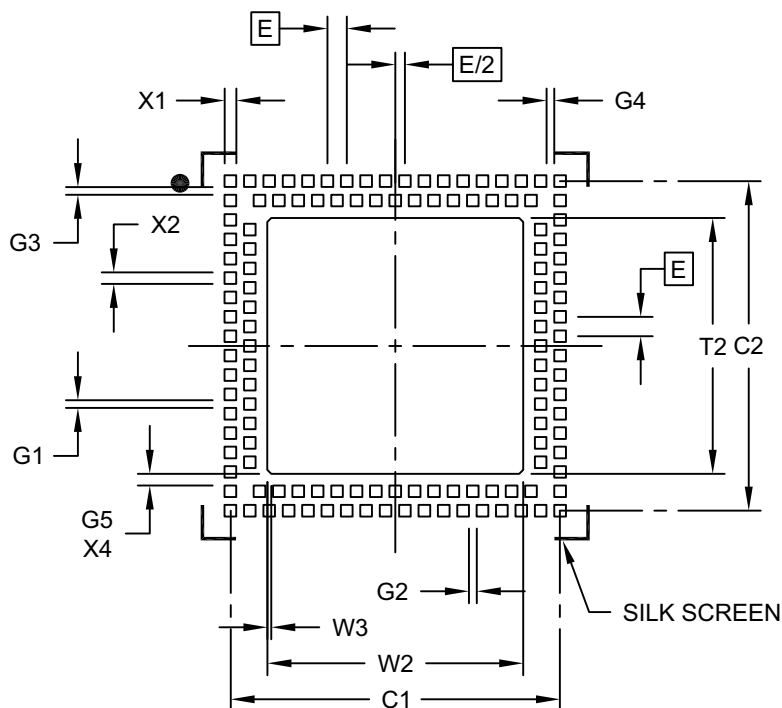
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2

PIC32MX5XX/6XX/7XX

124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Pad Clearance	G1	0.20		
Pad Clearance	G2	0.20		
Pad Clearance	G3	0.20		
Pad Clearance	G4	0.20		
Contact to Center Pad Clearance (X4)	G5	0.30		
Optional Center Pad Width	T2			6.60
Optional Center Pad Length	W2			6.60
Optional Center Pad Chamfer (X4)	W3		0.10	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X124)	X1			0.30
Contact Pad Length (X124)	X2			0.30

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A

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