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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx775f256h-80i-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC32MX795F512L

TABLE 12: PIN NAMES FOR USB, ETHERNET, AND CAN DEVICES

121-PIN TFBGA (BOTTOM VIEW)		L11
PIC32MX764F128L PIC32MX775F256L PIC32MX775F512L	L1	A11

A1

Note: The TFBGA package skips from row "H" to row "J" and has no "I" row.

Pin #	Full Pin Name	Pin #	Full Pin Name
A1	PMD4/RE4	E2	T4CK/AC2RX ⁽¹⁾ /RC3
A2	PMD3/RE3	E3	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6
A3	TRD0/RG13	E4	T3CK/AC2TX ⁽¹⁾ /RC2
A4	PMD0/RE0	E5	Vdd
A5	C2RX ⁽¹⁾ /PMD8/RG0	E6	C2TX ⁽¹⁾ /ETXERR/PMD9/RG1
A6	C1TX/ETXD0/PMD10/RF1	E7	Vss
A7	VDD	E8	AETXEN/SDA1/INT4/RA15
A8	Vss	E9	RTCC/EMDIO/AEMDIO/IC1/RD8
A9	ETXD2/IC5/PMD12/RD12	E10	SS1/IC2/RD9
A10	OC3/RD2	E11	AETXCLK/SCL1/INT3/RA14
A11	OC2/RD1	F1	MCLR
B1	No Connect (NC)	F2	ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8
B2	AERXERR/RG15	F3	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9
B3	PMD2/RE2	F4	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7
B4	PMD1/RE1	F5	Vss
B5	TRD3/RA7	F6	No Connect (NC)
B6	C1RX/ETXD1/PMD11/RF0	F7	No Connect (NC)
B7	VCAP	F8	Vdd
B8	PMRD/CN14/RD5	F9	OSC1/CLKI/RC12
B9	OC4/RD3	F10	Vss
B10	Vss	F11	OSC2/CLKO/RC15
B11	SOSCO/T1CK/CN0/RC14	G1	AERXD0/INT1/RE8
C1	PMD6/RE6	G2	AERXD1/INT2/RE9
C2	VDD	G3	TMS/RA0
C3	TRD1/RG12	G4	No Connect (NC)
C4	TRD2/RG14	G5	VDD
C5	TRCLK/RA6	G6	Vss
C6		G7	VSS
07	ETXCLK/PMD15/CN16/RD7	G8	
08	UC5/PMWR/CN13/RD4	G9	IDU/RA5
C10		GIU	
C10	SUSCI/CNT/RCTS		
D1	T2CK/RC1	H2	ANA/C1IN-/CN6/RB4
D2	PMD7/RF7	H3	Vss
D3	PMD5/RE5	H4	Von
D4	Vss	H5	No Connect (NC)
D5	Vss	H6	VDD
D6	No Connect (NC)	H7	No Connect (NC)
D7	ETXEN/PMD14/CN15/RD6	H8	VBUS
D8	ETXD3/PMD13/CN19/RD13	H9	VUSB3V3
D9	SDO1/OC1/INT0/RD0	H10	D+/RG2
D10	No Connect (NC)	H11	SCL2/RA2
D11	SCK1/IC3/PMCS2/PMA15/RD10	J1	AN3/C2IN+/CN5/RB3
E1	T5CK/SDI1/RC4	J2	AN2/C2IN-/CN4/RB2
Note	1: This pin is not available on PIC32MX76	4F128L devi	265

2: Shaded pins are 5V tolerant.

		Pin Nun	nber ⁽¹⁾			, 	
Pin Name	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA	Pin Type	Buffer Type	Description
PMD0	60	93	A4	B52	I/O	TTL/ST	Parallel Master Port data
PMD1	61	94	B4	A64	I/O	TTL/ST	(Demultiplexed Master mode) or
PMD2	62	98	B3	A66	I/O	TTL/ST	address/data (Multiplexed Master
PMD3	63	99	A2	B56	I/O	TTL/ST	modes)
PMD4	64	100	A1	A67	I/O	TTL/ST	
PMD5	1	3	D3	B2	I/O	TTL/ST	
PMD6	2	4	C1	A4	I/O	TTL/ST	
PMD7	3	5	D2	B3	I/O	TTL/ST	
PMD8	_	90	A5	A61	I/O	TTL/ST	
PMD9	_	89	E6	B50	I/O	TTL/ST	
PMD10		88	A6	A60	I/O	TTL/ST	
PMD11		87	B6	B49	I/O	TTL/ST	
PMD12	_	79	A9	B43	I/O	TTL/ST	
PMD13	_	80	D8	A54	I/O	TTL/ST	
PMD14	—	83	D7	B45	I/O	TTL/ST	
PMD15	—	84	C7	A56	I/O	TTL/ST	
PMALL	30	44	L8	A29	0	_	Parallel Master Port address latch enable low byte (Multiplexed Master modes)
PMALH	29	43	K7	B24	0		Parallel Master Port address latch enable high byte (Multiplexed Master modes)
PMRD	53	82	B8	A55	0		Parallel Master Port read strobe
PMWR	52	81	C8	B44	0		Parallel Master Port write strobe
VBUS	34	54	H8	A37	I	Analog	USB bus power monitor
VUSB3V3	35	55	H9	B30	Р	_	USB internal transceiver supply. If the USB module is <i>not</i> used, this pin must be connected to VDD.
VBUSON	11	20	H1	A12	0		USB Host and OTG bus power control output
D+	37	57	H10	B31	I/O	Analog	USB D+
D-	36	56	J11	A38	I/O	Analog	USB D-
USBID	33	51	K10	A35	I	ST	USB OTG ID detect
C1RX	58	87	B6	B49	I	ST	CAN1 bus receive pin
C1TX	59	88	A6	A60	0		CAN1 bus transmit pin
AC1RX	32	40	K6	A27	I	ST	Alternate CAN1 bus receive pin
AC1TX	31	39	L6	B22	0		Alternate CAN1 bus transmit pin
C2RX	29	90	A5	A61	Ι	ST	CAN2 bus receive pin
C2TX	21	89	E6	B50	0		CAN2 bus transmit pin
AC2RX	_	8	E2	A6	1	ST	Alternate CAN2 bus receive pin
Legend: C	CMOS = CMC ST = Schmitt T	S compatib	le input or c t with CMOS	output S levels	A O	nalog = A = Outpu	nalog input P = Power t I = Input

PINOLIT I/O DESCRIPTIONS (CONTINUED)

TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the "Device Pin Tables" section for device pin availability.

2: See 25.0 "Ethernet Controller" for more information.

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Program Memory" (DS60001121) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32). PIC32MX5XX/6XX/7XX devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming[™] (ICSP[™])

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual"*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "*PIC32 Flash Programming Specification*" (DS60001145), which can be downloaded from the Microchip web site.

Note: For PIC32MX5XX/6XX/7XX devices, the Flash page size is 4 KB and the row size is 512 bytes (1024 IW and 128 IW, respectively).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0						
31:24	_			—	—		_	_
00.40	U-0	U-0						
23.10	—	—	—	—	—		Bit Bit 0/2 25/17/9/1 24/16/8/0 U-0 U-0 U-0 U-0 U-0 U-0 R/W-0, HS R/W-0 CMR VREGS HS R/W-1, HS BOR ⁽¹⁾ POR ⁽¹⁾	
45.0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
10.0	—	—	—	—	—		CMR	VREGS
7.0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
31:24 23:16 15:8 7:0	EXTR	SWR	_	WDTO	SLEEP	IDLE	BOR ⁽¹⁾	POR ⁽¹⁾

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Legend:	HS = Set by hardware						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-10	Unimplemented: Read as '	n'
	eninplemented. Read as	

bit 9	CMR: Configuration Mismatch Reset Flag bit 1 = Configuration mismatch Reset has occurred 0 = Configuration mismatch Reset has not occurred
bit 8	VREGS: Voltage Regulator Standby Enable bit 1 = Regulator is enabled and is on during Sleep mode 0 = Regulator is set to Stand-by Tracking mode
bit 7	EXTR: External Reset (MCLR) Pin Flag bit 1 = Master Clear (pin) Reset has occurred 0 = Master Clear (pin) Reset has not occurred
bit 6	SWR: Software Reset Flag bit 1 = Software Reset was executed 0 = Software Reset was not executed
bit 5	Unimplemented: Read as '0'
bit 4	WDTO: Watchdog Timer Time-out Flag bit
	1 = WDT Time-out has occurred 0 = WDT Time-out has not occurred
bit 3	SLEEP: Wake From Sleep Flag bit 1 = Device was in Sleep mode 0 = Device was not in Sleep mode
bit 2	IDLE: Wake From Idle Flag bit
	1 = Device was in Idle mode 0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit ⁽¹⁾ 1 = Brown-out Reset has occurred 0 = Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit ⁽¹⁾
	1 = Power-on Reset has occurred0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view the next detection.

TABLE 7-7: INTERRUPT REGISTER MAP FOR PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

ess										В	its					Bits													
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets										
4000		31:16	_		_		INT4IP<2:0>	`	INT4IS	S<1:0>	—	_	_		OC4IP<2:0>	•	OC4IS	S<1:0>	0000										
1000	IPC4	15:0	_	_	_		IC4IP<2:0>		IC4IS	<1:0>	_	_	_		T4IP<2:0>		T4IS	<1:0>	0000										
1050	IDOF	31:16		—	_		SPI1IP<2:0>	`	SPI1IS	S<1:0>	_	_	—		OC5IP<2:0>	•	OC5IS	S<1:0>	0000										
10E0	IPC5	15:0	_	_	_		IC5IP<2:0>		IC5IS	<1:0>	_	_	_		T5IP<2:0>		T5IS	<1:0>	0000										
		31:16	_	_	_		AD1IP<2:0>		AD1IS	S<1:0>	_	_	_		CNIP<2:0>		CNIS	<1:0>	0000										
1050	IDCC														U1IP<2:0>		U1IS	<1:0>											
TUFU	IPC6	15:0	_	—	—	_		I2C1IP<2:0>	•	I2C118	S<1:0>	—	_	_		SPI3IP<2:0>	>	SPI3I	S<1:0>	0000									
														12C3IP<2:0>			12C31	S<1:0>											
							U3IP<2:0>		U3IS	<1:0>																			
1100		31:16	—	—	—		SPI2IP<2:0>	`	SPI2IS	S<1:0>	—	—	—		CMP2IP<2:0	>	CMP2	S<1:0>	0000										
1100	11 07	07				I2C4IP<2:0>		I2C4IS<1:0>																					
		15:0		—		(CMP1IP<2:0	>	CMP1I	S<1:0>	-	_			PMPIP<2:0>		PMPIS<1:0>		0000										
		31:16	-	—	—	F	RTCCIP<2:0	>	RTCCI	S<1:0>	—	—	—		SCMIP<2:0	>	FSCM	S<1:0>	0000										
1110															U2IP<2:0>		U2IS	<1:0>											
1110	11 00	15:0	_	—	—		I2C2IP<2:0>		12C218	S<1:0>	-	-	—		SPI4IP<2:0>	>	SPI4I	S<1:0>	0000										
															I2C5IP<2:0>	•	12C51	S<1:0>											
1120	IPCO	31:16	-	—	—	[DMA3IP<2:0	>	DMA3I	S<1:0>	—	—	—		DMA2IP<2:0	>	DMA2	S<1:0>	0000										
1120	11 03	15:0		—		[DMA1IP<2:0	>	DMA1I	S<1:0>	-	_			DMA0IP<2:0	>	DMA0	S<1:0>	0000										
1120		31:16	_	—	—	D	MA7IP<2:0>	(2)	DMA7IS	S<1:0> ⁽²⁾	—	—	—	D	MA6IP<2:0>	(2)	DMA6IS	S<1:0> ⁽²⁾	0000										
1130	IFCIU	15:0		_	—	D	MA5IP<2:0>	(2)	DMA5IS	S<1:0> ⁽²⁾	_	—	—	D	MA4IP<2:0>	(2)	DMA4IS	S<1:0> ⁽²⁾	0000										
1140		31:16		—	—	C	CAN2IP<2:0> ⁽²⁾		CAN2IS	5<1:0> ⁽²⁾	—	—	—		CAN1IP<2:0>		CAN1I	S<1:0>	0000										
1140	IFUII	15:0		_	—		USBIP<2:0>		USBIS	S<1:0>	_	_	—		FCEIP<2:0>		FCEIP<2:0>		FCEIS<1:0>		0000								
1150		31:16		_	—		U5IP<2:0>		U5IS	<1:0>	_	-	_		U6IP<2:0>		U6IS	<1:0>	0000										
1150	IFUIZ	15:0	_	_	_		U4IP<2:0>		U4IS	<1:0>	—	-	_		ETHIP<2:0>	,	ETHIS	S<1:0>	0000										

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Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Note 1: Registers" for more information.

2: This bit is unimplemented on PIC32MX764F128L device.

3: This register does not have associated CLR, SET, and INV registers.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	—	—	—	—	—		—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
23.10	—	—	—	—	—	—	—	SS0
45.0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
15:8	—	—	—	MVEC	—		TPC<2:0>	
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8 7:0	_	_	_	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-17 Unimplemented: Read as '0'

- bit 16 **SS0:** Single Vector Shadow Register Set bit
 - 1 = Single vector is presented with a shadow register set
 - 0 = Single vector is not presented with a shadow register set
- bit 15-13 Unimplemented: Read as '0'
- bit 12 MVEC: Multiple Vector Configuration bit
 - 1 = Interrupt controller configured for Multi-vector mode
 - 0 = Interrupt controller configured for Single-vector mode
- bit 11 Unimplemented: Read as '0'
- bit 10-8 TPC<2:0>: Interrupt Proximity Timer Control bits
 - 111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer 110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer 101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer 100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer 011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
 - 010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
 - 001 = Interrupts of group priority 1 start the Interrupt Proximity timer
 - 000 = Disables Interrupt Proximity timer
- bit 7-5 Unimplemented: Read as '0'
- bit 4 INT4EP: External Interrupt 4 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge
- bit 3 INT3EP: External Interrupt 3 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge
- bit 2 INT2EP: External Interrupt 2 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge
- bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge
- bit 0 INTOEP: External Interrupt 0 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge

TABLE 11-1: USB REGISTER MAP (CONTINUED)

ess		0		Bits															ø
Virtual Add (BF88_# Register Name ⁽¹⁾	Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset	
5340	A0 U1EP10	31:16	—	_	_	—	—	—	—	_	—	—	—	_	_	_		_	0000
55A0	UTEI 10	15:0	—	-	—	—	-	_	—	—	_	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5200	U1EP11	31:16	_	-	_	_	-	—	—	—	—	—	_	—	—	_	_	-	0000
5560		15:0	_		_	_		_		—	_	_		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5200		31:16		-			-	_		_	—	—	-	_	_	-	_		0000
5300	UIEPIZ	15:0	_	_	-	_	_	_	—	_	_	-	-	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5000		31:16	—	_	_	—	_	—	—	—	_	_	_	—	—	_	_	_	0000
53D0	UTEP13	15:0	_	_	_	_	_	_	_	—	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
53EU	UTEP14	15:0	_	_	_	_	_	_	_	—	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5250		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
53F0	UIEP15	15:0	_	—	_	_	—	—		—	_	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend:

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Note 1:

All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

This register does not have associated SET and INV registers. 2:

3: This register does not have associated CLR, SET and INV registers.

Reset value for this bit is undefined. 4:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—		—	—	
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		_	_	_			_	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—		—	—	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

REGISTER 11-4: U10TGCON: USB OTG CONTROL REGISTER

Legend:

bit 7

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

DPPULUP: D+ Pull-Up Enable bit 1 = D+ data line pull-up resistor is enabled 0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

- 1 = D- data line pull-up resistor is enabled
 0 = D- data line pull-up resistor is disabled
- bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
 - 1 = D+ data line pull-down resistor is enabled
 - 0 = D+ data line pull-down resistor is disabled

bit 4 DMPULDWN: D- Pull-Down Enable bit

- 1 = D- data line pull-down resistor is enabled
- 0 = D- data line pull-down resistor is disabled

bit 3 VBUSON: VBUS Power-on bit

- 1 = VBUS line is powered
- 0 = VBUS line is not powered
- bit 2 **OTGEN:** OTG Functionality Enable bit
 - 1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
 - 0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 VBUSCHG: VBUS Charge Enable bit

- 1 = VBUS line is charged through a pull-up resistor
- 0 = VBUS line is not charged through a resistor

bit 0 VBUSDIS: VBUS Discharge Enable bit

- 1 = VBUS line is discharged through a pull-down resistor
- 0 = VBUS line is not discharged through a resistor

PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	—	—	—		
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	—	—		—		—		
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15:8	—	—	—	—		—		—		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7.0		CNT<7:0>								

REGISTER 11-16: U1SOF: USB SOF THRESHOLD REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-0 CNT<7:0>: SOF Threshold Value bits
 - Typical values of the threshold are: 01001010 = 64-byte packet 00101010 = 32-byte packet 00011010 = 16-byte packet

00010010 = 8-byte packet

REGISTER 11-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
7.0	BDTPTRL<15:9>							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-1 BDTPTRL<15:9>: BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 Unimplemented: Read as '0'

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The UART module is one of the serial I/O modules available in the PIC32MX5XX/6XX/7XX family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN 1.2 and IrDA[®]. The module also supports the hardware flow control option, with UXCTS and UXRTS pins, and also includes an IrDA encoder and decoder.

The following are primary features of the UART module:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- · One or two Stop bits
- Hardware auto-baud feature
- · Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 20 Mbps at 80 MHz
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (ninth bit = 1)
- · Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN 2.1 Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 20-1 illustrates a simplified block diagram of the UART module.



FIGURE 20-1: UART SIMPLIFIED BLOCK DIAGRAM

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	
31.24	—	—	—	—	—	—	CAL<9):8>	
22.46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	CAL<7:0>								
15.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
10.0	ON ^(1,2)	—	SIDL	—	—	—	—	—	
7.0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0	
7:0	RTSECSEL ⁽³⁾	RTCCLKON	—	—	RTCWREN ⁽⁴⁾	RTCSYNC	HALFSEC ⁽⁵⁾	RTCOE	

REGISTER 22-1: RTCCON: RTC CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 Unimplemented: Read as '0'

bit 25-16 CAL<9:0>: RTC Drift Calibration bits, which contain a signed 10-bit integer value

	<pre>1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute</pre>
	100000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute 0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute
	•
L11 4 5	• 000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute 000000000 = No adjustment
DIT 15	1 = RTCC module is enabled 0 = RTCC module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Stop in Idle Mode bit
	 1 = Disables the PBCLK to the RTCC when CPU enters in Idle mode 0 = Continue normal operation in Idle mode
bit 12-8	Unimplemented: Read as '0'
bit 7	RTSECSEL: RTCC Seconds Clock Output Select bit ⁽³⁾
	 1 = RTCC Seconds Clock is selected for the RTCC pin 0 = RTCC Alarm Pulse is selected for the RTCC pin
bit 6	RTCCLKON: RTCC Clock Enable Status bit
	1 = RTCC Clock is actively running
	0 = RTCC Clock is not running
bit 5-4	Unimplemented: Read as '0'
Note 1:	The ON bit is only writable when RTCWREN = 1.
2:	When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
3:	Requires $RTCOE = 1$ (RTCCON<0>) for the output to be active.
4:	The RTCWREN bit can only be set when the write sequence is enabled.
5:	This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is only reset on a Power-on Reset (POR).

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PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

REGISTER 24-10: CIFLTCON0: CAN FILTER CONTROL REGISTER 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN3: Filter 3 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL3<1:0>: Filter 3 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 28-24	FSEL3<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN2: Filter 2 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 22-21	MSEL2<1:0>: Filter 2 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 20-16	FSEL2<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN31	MSEL31<1:0>		FSEL31<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN30	MSEL30<1:0>		FSEL30<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN29	MSEL29<1:0>		FSEL29<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN28	MSEL28<1:0>		FSEL28<4:0>				

REGISTER 24-17: CIFLTCON7: CAN FILTER CONTROL REGISTER 7

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

h ii 04	ELTENDA: Eller 04 Enchla bit
bit 31	FLIEN31: Flitter 31 Enable bit
	1 = Filter is enabled 0 = Filter is disabled
hit 30-20	MSEL 31-1:0-: Filter 31 Mask Select hits
bit 30-29	11 - Accentance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 28-24	FSEL31<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN30: Filter 30Enable bit
	1 = Filter is enabled
bit 22-21	MSEL30<1:0>: Filter 30Mask Select bits
	11 = Acceptance Mask 3 selected
	01 = Acceptance Mask 2 selected
	00 = Acceptance Mask 0 selected
bit 20-16	FSEL30<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 24-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' (n = 0 THROUGH 31)

- bit 6 TXABAT: Message Aborted bit⁽²⁾ 1 = Message was aborted 0 = Message completed successfully bit 5 TXLARB: Message Lost Arbitration bit⁽³⁾ 1 = Message lost arbitration while being sent 0 = Message did not lose arbitration while being sent TXERR: Error Detected During Transmission bit⁽³⁾ bit 4 1 = A bus error occured while the message was being sent 0 = A bus error did not occur while the message was being sent bit 3 **TXREQ:** Message Send Request TXEN = 1: (FIFO configured as a Transmit FIFO) Setting this bit to '1' requests sending a message. The bit will automatically clear when all the messages queued in the FIFO are successfully sent. Clearing the bit to '0' while set ('1') will request a message abort. TXEN = 0: (FIFO configured as a receive FIFO) This bit has no effect. bit 2 RTREN: Auto RTR Enable bit 1 = When a remote transmit is received, TXREQ will be set 0 = When a remote transmit is received, TXREQ will be unaffected bit 1-0 TXPR<1:0>: Message Transmit Priority bits 11 = Highest message priority 10 = High intermediate message priority 01 = Low intermediate message priority 00 = Lowest message priority Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).
 - 2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
 - 3: This bit is reset on any read of this register or when the FIFO is reset.

31:24 U-0 U-0 </th <th>I-0 U-0 U-0 U-0 </th> <th>U-0 —</th> <th>U-0</th> <th>U-0</th> <th>U-0</th> <th>U-0</th> <th></th>	I-0 U-0 U-0 U-0 	U-0 —	U-0	U-0	U-0	U-0	
31.24	 N-0 R/W-0 R/W-0 R/W-0	— 	—				
23:16 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0	W-0 R/W-0 R/W-0 R/W-0	P/W_0				—	31:24
23.10 BUFCNT<7:0>		10/00-0	R/W-0	R/W-0	R/W-0	R/W-0	00.40
		23:16					
15-8 U-0 U-0 U-0 U-0 U-0 U-0 U-0	-0 U-0 U-0 U-0	U-0	U-0	U-0	U-0	U-0	15:8
		_	-		—	—	
7-0 R/W-0 R/W-0 R/W-0 U-0 U-0 U-0 U-0	-0 U-0 U-0 U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	7:0
ETHBUSY ⁽¹⁾ TXBUSY ⁽²⁾ RXBUSY ⁽²⁾		_	_	RXBUSY ⁽²⁾	TXBUSY ⁽²⁾	ETHBUSY ⁽¹⁾	

REGISTER 25-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

Legend:

Logena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 Unimplemented: Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x000. When software attempts to decrement the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

- **Note:** BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.
- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 ETHBUSY: Ethernet Module busy bit⁽¹⁾

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction 0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

- bit 6 **TXBUSY:** Transmit Busy bit⁽²⁾
 - 1 = TX logic is receiving data
 - 0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

- **Note 1:** This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
 - **2:** This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

REGISTER 25-27: EMAC1CLRT: ETHERNET CONTROLLER MAC COLLISION WINDOW/RETRY LIMIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	CWINDOW<5:0>					
7:0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
		_	_	_		RETX<	<3:0>	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

bit 13-8 **CWINDOW<5:0>:** Collision Window bits

This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

bit 7-4 Unimplemented: Read as '0'

bit 3-0 RETX<3:0>: Retransmission Maximum bits

This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts (attemptLimit) to be 0xF (15d). Its default is '0xF'.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

30.0 INSTRUCTION SET

The PIC32MX5XX/6XX/7XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core Extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to "MIPS32[®] Architecture for Programmers Volume II: The MIPS32[®] Instruction Set" at www.imgtec.com for more information.

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimensior	l Limits	MIN	NOM	MAX
Contact Pitch	E1		0.80 BSC	
Contact Pitch	E2		0.80 BSC	
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D

Revision H (March 2013)

This revision includes the following global updates:

- Where applicable, control register tables have been added to the document
- All references to VCORE were removed
- All occurrences of XBGA have been updated to: TFBGA

TABLE B-6: MAJOR SECTION UPDATES

• All occurrences of VUSB have been updated to: VUSB3V3

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other significant changes are referenced by their respective section in Table B-6.

Section Name	Update Description
"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet"	Updated Core features. Added the VTLA to the Packages table. Added Note 5 to the Feature tables (see Table 1, Table 2, and Table 3).
Section 2.0 "Guidelines for Getting Started with 32-bit MCUs"	The Recommended Minimum Connection was updated (see Figure 2-1).
Section 5.0 "Flash Program Memory"	A note regarding Flash page size and row size was added.
Section 8.0 "Oscillator Configuration"	The RP resistor was added and Note 1 was updated in the Oscillator Diagram (see Figure 8-1).
Section 31.0 "Electrical Characteristics"	Added Note 1 to Operating MIPS vs. Voltage (see Table 31-1). Added the VTLA package to Thermal Packaging Characteristics (see Table 31-3). Added Note 2 to DC Temperature and Voltage Specifications (see Table 31-4). Updated Note 2 in the Operating Current DC Characteristics (see Table 31-5). Updated Note 1 in the Idle Current DC Characteristics (see Table 31-6). Updated Note 1 in the Power-Down Current DC Characteristics (see Table 31-7). Updated the I/O Pin Output Specifications (see Table 31-9). Added Note 2 to the BOR Electrical Characteristics (see Table 31-10). Added Note 3 to the Comparator Specifications (see Table 31-13). Parameter D320 (VCORE) was removed (see Table 31-15). Updated the Minimum value for parameter OS50 (see Table 31-18). Parameter SY01 (TPWRT) was removed (see Table 31-22). Note 1 was added and the conditions for parameters ET3, ET4, ET7, and ET9 were updated in the Ethernet Module Specifications (see Table 31-35). Added Note 3 to the 10-bit ADC Conversion Rate Parameter (see Table 31-37). Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 31-38). The following figures were added: Figure 31-19: "MDIO Sourced by the PIC32 Device" Figure 31-21: "Transmit Signal Timing Relationships at the MII" Figure 31-22: "Receive Signal Timing Relationships at the MII"
Device Characteristics Graphs"	
Section 33.0 "Packaging Information"	Added the 124-lead VTLA package information (see Section 33.1 "Package Marking Information" and Section 33.2 "Package Details").
"Product Identification System"	Added the TL definition for VTLA packages.

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