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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx775f256h-80v-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# 1.0 DEVICE OVERVIEW

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

FIGURE 1-1: BLOCK DIAGRAM<sup>(1,2)</sup>

This document contains device-specific information for PIC32MX5XX/6XX/7XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX5XX/6XX/7XX family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.



# 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUS

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

## 2.1 Basic Connection Requirements

Getting started with the PIC32MX5XX/6XX/7XX family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins even if the ADC module is not used (see 2.2 "Decoupling Capacitors")
- VCAP pin (see 2.3 "Capacitor on Internal Voltage Regulator (VCAP)")
- MCLR pin (see 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>) and debugging purposes (see **2.5** "ICSP Pins")
- OSC1 and OSC2 pins when external oscillator source is used (see 2.8 "External Oscillator Pins")

The following pin may be required, as well: VREF+/ VREF- pins used when external voltage reference for ADC module is implemented.

**Note:** The AVDD and AVSS pins must be connected, regardless of the ADC use and the ADC voltage reference source.

# 2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A value of 0.1  $\mu$ F (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended to use ceramic capacitors.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high frequency noise: If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01  $\mu$ F to 0.001  $\mu$ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1  $\mu$ F in parallel with 0.001  $\mu$ F.
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.





# **Note 1:** If the USB module is not used, this pin must be connected to VDD.

2: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than  $3\Omega$  and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2}$$
 (i.e., ADC conversion rate/2)  
$$f = \frac{1}{(2\pi\sqrt{LC})}$$
$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

3: Aluminum or electrolytic capacitors should not be used. ESR  $\leq 3\Omega$  from -40°C to 125°C @ SYSCLK frequency (i.e., MIPS).

## 2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7  $\mu F$  to 47  $\mu F$ . This capacitor should be located as close to the device as possible.

# 2.3 Capacitor on Internal Voltage Regulator (VCAP)

### 2.3.1 INTERNAL REGULATOR MODE

A low-ESR (1 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 32.0 "Electrical Characteristics"** for additional information on CEFC specifications.

# 2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

### FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

- 2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.
- **3:** No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
	U-0	R/W-1	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1
7:0	_	BMX WSDRM	_	_	_	E	3MXARB<2:0	>

## REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

# bit 31-21 **Unimplemented:** Read as '0'

bit 20	BMXERRIXI: Enable Bus Error from IXI bit
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus</li> </ul>
bit 19	BMXERRICD: Enable Bus Error from ICD Debug Unit bit
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from ICD</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from ICD</li> </ul>
bit 18	BMXERRDMA: Bus Error from DMA bit
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from DMA</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from DMA</li> </ul>
bit 17	BMXERRDS: Bus Error from CPU Data Access bit (disabled in Debug mode)
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access</li> </ul>
bit 16	BMXERRIS: Bus Error from CPU Instruction Access bit (disabled in Debug mode)
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access</li> </ul>
bit 15-7	Unimplemented: Read as '0'
bit 6	BMXWSDRM: CPU Instruction or Data Access from Data RAM Wait State bit
	<ul> <li>1 = Data RAM accesses from CPU have one wait state for address setup</li> <li>0 = Data RAM accesses from CPU have zero wait states for address setup</li> </ul>
bit 5-3	Unimplemented: Read as '0'
bit 2-0	BMXARB<2:0>: Bus Matrix Arbitration Mode bits
	111 = Reserved (using these Configuration modes will produce undefined behavior)
	•
	011 = Reserved (using these Configuration modes will produce undefined behavior)
	010 = Arbitration Node 2 0.01 = Arbitration Mode 1 (default)
	000 = Arbitration Mode 0

# 9.0 PREFETCH CACHE

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 4. "Prefetch Cache" (DS60001119) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

Prefetch cache increases performance for applications executing out of the cacheable program Flash memory regions by implementing instruction caching, constant data caching and instruction prefetching.

# 9.1 Features

- 16 fully-associative lockable cache lines
- 16-byte cache lines
- Up to four cache lines allocated to data
- Two cache lines with address mask to hold repeated instructions
- Pseudo-LRU replacement policy
- All cache lines are software writable
- 16-byte parallel memory fetch
- Predictive instruction prefetch

A simplified block diagram of the Prefetch Cache module is illustrated in Figure 9-1.



## FIGURE 9-1: PREFETCH CACHE MODULE BLOCK DIAGRAM

# TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP

ess		â								Bi	its								6
Virtual Addr (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3060		31:16	_	—	—	_	_	_	—	—	—	—	—	—	—	—	_	—	0000
5000	DOI1000IN	15:0	CHBUSY	_	—	_	_	_	_	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPR	l<1:0>	0000
3070	DCH0ECON	31:16	_	—	—	—	—	—	—	—		1	1	CHAIR	Q<7:0>				00FF
		15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3080	DCH0INT	31:16	_		_						CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHIAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHIAIF	CHERIF	0000
3090	D90 DCH0SSA 31:16 CHSSA<31:0>							0000											
		31.16																	0000
30A0	DCH0DSA	15.0								CHDSA	A<31:0>								0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
30B0	DCH0SSIZ	15:0								CHSSIZ	Z<15:0>								0000
		31:16	_	_	_	_	_	—	_	_	_	_	_	_	_	_	_	_	0000
30C0	DCH0DSIZ	15:0								CHDSIZ	Z<15:0>								0000
2000		31:16	_	—	—	—	_	—	—	—	—	—	—	_	—	_	_	—	0000
3000	DCHUSPIK	15:0								CHSPT	R<15:0>								0000
30E0		31:16	-	_	—			_		—	_	—	_	—	—	_	-		0000
3020		15:0								CHDPT	R<15:0>								0000
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
00.0	501100012	15:0								CHCSIZ	Z<15:0>								0000
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0								CHCPT	R<15:0>								0000
3110	DCH0DAT	31:16	_		_							—					_	_	0000
		15:0		_	_	_	_	_	_	_				CHPDA	\I<7:0>				0000
3120	DCH1CON	31:16																	0000
		31.16	CHB031								CHEN	CHAED	CHCHN	CHAIR	0-7:0>	CHEDET	CHER	1<1.0>	0000
3130	DCH1ECON	15.0				CHSIR	0<7:0>				CEORCE	CABORT	PATEN	SIROEN		_	_	_	1100
		31:16	_	_	_	_	_	_	_	_	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
3140	DCH1INT	15:0	_	_	_	_	_	_	_	_	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
		31:16											-				-	-	0000
3150	DCH1SSA	15:0								CHSSA	A<31:0>								0000
24.00	DOUMDOA	31:16																	0000
3160	DCHIDSA	15:0								CHDSA	4<31:0>								0000
3170		31:16		—		_	_	_		—	_		_			_	_		0000
3170	00013312	15:0								CHSSIZ	Z<15:0>								0000
Legen	d: x=u	unknowr	value on R	eset; — = ur	nimplemente	d, read as '0	'. Reset valu	ues are show	vn in hexade	ecimal.									

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more Note 1: information.

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2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—		—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	—	—	—	—	—	—	—	—
7.0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
7.0	UACTPND	_	_	USLPGRD	USBBUSY		USUSPEND	USBPWR

#### REGISTER 11-5: U1PWRC: USB POWER CONTROL REGISTER

## Legend:

Logonan						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

#### bit 31-8 Unimplemented: Read as '0'

- bit 7 UACTPND: USB Activity Pending bit
  - 1 = USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
  - 0 = An interrupt is not pending

#### bit 6-5 Unimplemented: Read as '0'

- bit 4 USLPGRD: USB Sleep Entry Guard bit
  - 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
  - 0 = USB module does not block Sleep entry

#### bit 3 USBBUSY: USB Module Busy bit

- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled
  - **Note:** When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

#### bit 2 Unimplemented: Read as '0'

#### bit 1 USUSPEND: USB Suspend Mode bit

- 1 = USB module is placed in Suspend mode
  - (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally
- bit 0 USBPWR: USB Operation Enable bit
  - 1 = USB module is turned on
  - 0 = USB module is disabled

(Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	-	-						
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	—	_								
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15:8	—	—								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
		BDTPTRH<23:16>								

### REGISTER 11-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

#### Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-8 Unimplemented: Read as '0'

#### bit 7-0 BDTPTRH<23:16>: BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

#### REGISTER 11-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—		—		-				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—		_						
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15:8	—	—		—						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
		BDTPTRU<31:24>								

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-8 Unimplemented: Read as '0'

#### bit 7-0 BDTPTRU<31:24>: BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

0 = Start condition is not in progress

#### I2CxCON: I<sup>2</sup>C CONTROL REGISTER (CONTINUED) REGISTER 19-1: **GCEN:** General Call Enable bit (when operating as I<sup>2</sup>C slave) bit 7 1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception) 0 = General call address is disabled STREN: SCLx Clock Stretch Enable bit (when operating as I<sup>2</sup>C slave) bit 6 Used in conjunction with SCLREL bit. 1 = Enable software or receive clock stretching 0 = Disable software or receive clock stretching bit 5 ACKDT: Acknowledge Data bit (when operating as I<sup>2</sup>C master, applicable during master receive) Value that is transmitted when the software initiates an acknowledge sequence. 1 = Send NACK during an acknowledge 0 = Send ACK during an acknowledge bit 4 ACKEN: Acknowledge Sequence Enable bit (when operating as I<sup>2</sup>C master, applicable during master receive) 1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence. 0 = Acknowledge sequence not in progress bit 3 **RCEN:** Receive Enable bit (when operating as I<sup>2</sup>C master) 1 = Enables Receive mode for $l^2C$ . Hardware clear at end of eighth bit of master receive data byte. 0 = Receive sequence is not in progress **PEN:** Stop Condition Enable bit (when operating as I<sup>2</sup>C master) bit 2 1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence. 0 = Stop condition is not in progress **RSEN:** Repeated Start Condition Enable bit (when operating as I<sup>2</sup>C master) bit 1 1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence. 0 = Repeated Start condition is not in progress **SEN:** Start Condition Enable bit (when operating as I<sup>2</sup>C master) bit 0 1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

# PIC32MX5XX/6XX/7XX





# PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
	SID<10:3>									
00.40	R/W-x	R/W-x	R/W-x	U-0	R/W-0	U-0	R/W-x	R/W-x		
23.10		SID<2:0>		—	EXID	—	EID<17:16>			
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15:8	EID<15:8>									
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
				EID<	:7:0>					

### REGISTER 24-18: CIRXFn: CAN ACCEPTANCE FILTER 'n' REGISTER 7 (n = 0 THROUGH 31)

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 SID<10:0>: Standard Identifier bits

- 1 = Message address bit SIDx must be '1' to match filter
- 0 = Message address bit SIDx must be '0' to match filter
- bit 20 Unimplemented: Read as '0'
- bit 19 **EXID:** Extended Identifier Enable bits
  - 1 = Match only messages with extended identifier addresses
  - 0 = Match only messages with standard identifier addresses
- bit 18 Unimplemented: Read as '0'
- bit 17-0 EID<17:0>: Extended Identifier bits
  - 1 = Message address bit EIDx must be '1' to match filter
  - 0 = Message address bit EIDx must be '0' to match filter

**Note:** This register can only be modified when the filter is disabled (FLTENn = 0).

#### TABLE 25-5: ETHERNET CONTROLLER REGISTER SUMMARY FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX695F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX764F128H, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

ess										В	its								
Virtual Addr (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0050	ETURTAT	31:16			_	_	_		_					BUFCN	NT<7:0>				0000
90E0	EIHSIAI	15:0	—	-	—	—	_	-	-	1	BUSY	TXBUSY	RXBUSY	—	—	—	-	—	0000
9100	ETH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0.00	RXOVFLOW	15:0								RXOVFLW	/CNT<15:0>								0000
9110	ETH	31:16	—	—	—	—	—	—	-	—	—		_	—	_	—	_	—	0000
	FRMIXOK	15:0								FRMTXOK	CNT<15:0>								0000
9120	ETH SCOLERM	31:16	—	_	—	—	_	_	-	-	-			-		—	_	—	0000
		15:0								SCOLFRM	ICN I <15:0>								0000
9130	ETH MCOLFRM	15:0		—		_	_	—	_			_		—		_	—	_	0000
	сты	31.16	_	_	_	_	_	_	_		_	_	_	_	_	_	_	_	0000
9140	FRMRXOK	15:0								FRMRXOK	CNT<15:0>								0000
	FTH	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	—	0000
9150	FCSERR	15:0								FCSERRO	CNT<15:0>								0000
0160	ETH	31:16		_		_	_	_	—	_		_	_	_	_		_		0000
9100	ALGNERR	15:0								ALGNERR	CNT<15:0>	-	-		-				0000
	EMAC1	31:16	—	—	—	—	—	—	—	-	—	—	—	-	—	—	—	—	0000
9200	CFG1	15:0	SOFT RESET	SIM RESET		_	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN		_		LOOPBACK	TXPAUSE	RXPAUSE	PASSALL	RXENABLE	800D
	EMAC1	31:16	—	_	—	—	_	_	_		—	_				—	_	—	0000
9210	CFG2	15:0	—	EXCESS DFR	BP NOBKOFF	NOBKOFF	_	_	LONGPRE	PUREPRE	AUTOPAD	VLANPAD	PAD ENABLE	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX	4082
0220	EMAC1	31:16	—	_	_	_	_	_	_		—	_	_	—	_	_	_	—	0000
3220	IPGT	15:0	—	_	_	_	_	_	_	_	_			B	2BIPKTGP<6	:0>			0012
9230	EMAC1	31:16	—	—	—	-	—	—	-	—	-	_	—	—	—	—	-	—	0000
0200	IPGR	15:0	—			NB2	2BIPKTGP1<6	6:0>			—			NB:	2BIPKTGP2<	6:0>			0C12
9240	EMAC1	31:16	—	_	—	—	—	—	—	_	_	_	—	-	—	—	—	—	0000
	CLKI	15:0	—	_			CWINDO	DW<5:0>			_	_	_	_		RETX	<3:0>		370F
9250	EMAC1	31:16	—	—	—	—	-	_	-	—		—	—	-	—	—	—	—	0000
	IVIAAF	15:0								MACMA	X⊦<15:0>								05EE

PIC32MX5XX/6XX/7XX

x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

Reset values default to the factory programmed value. 2:

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#### REGISTER 25-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
10.0	—	—	—	—	—	—	—	—
7.0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
7.0	_			B2	BIPKTGP<6:(	)>		

#### Legend:

Logona			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-7 Unimplemented: Read as '0'

#### bit 6-0 B2BIPKTGP<6:0>: Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96  $\mu$ s (in 100 Mbps) or 9.6  $\mu$ s (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96  $\mu$ s (in 100 Mbps) or 9.6  $\mu$ s (in 100 Mbps) (in 100 Mbps) or 9.6  $\mu$ s (in 100 Mbps) (in 100 Mbps) (in 100 Mbps) or

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

#### REGISTER 29-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	
31:24	—	—	—	—	—	-	—	—	
00.40	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P	
23:16	—	—	—	—	—	FPLLODIV<2:0>			
45.0	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P	
15:8	UPLLEN	—	—	—	—	UPLLIDIV<2:0>			
7.0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P	
7:0		F	PLLMUL<2:0	>	_	FPLLIDIV<2:0>			

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-19 Reserved: Write '1'

bit 18-16 **FPLLODIV<2:0>:** PLL Output Divider bits 111 = PLL output divided by 256

- 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2
- 000 = PLL output divided by 1
- bit 15 UPLLEN: USB PLL Enable bit 1 = Disable and bypass USB PLL 0 = Enable USB PLL
- bit 14-11 Reserved: Write '1'
- bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits
  - 111 = 12x divider
  - 110 = 10x divider
  - 101 = 6x divider
  - 100 = 5x divider
  - 011 = 4x divider
  - 010 = 3x divider
  - 001 = 2x divider 000 = 1x divider
- bit 7 **Reserved:** Write '1'
- bit 6-4 FPLLMUL<2:0>: PLL Multiplier bits
  - 111 = 24x multiplier
  - 110 = 21x multiplier
  - 101 = 20x multiplier
  - 100 = 19x multiplier
  - 011 = 18x multiplier
  - 010 = 17x multiplier 001 = 16x multiplier
  - 001 = 10x multiplier
- bit 3 **Reserved:** Write '1'



### TABLE 32-22: RESETS TIMING

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical <sup>(2)</sup>	Max.	Units	Conditions	
SY00	Τρυ	Power-up Period Internal Voltage Regulator Enabled	_	400	600	μS	-40°C to +85°C	
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.		1 μs + 8 SYSCLK cycles		_	-40°C to +85°C	
SY20	TMCLR	MCLR Pulse Width (low)	_	2	_	μS	-40°C to +85°C	
SY30	TBOR	BOR Pulse Width (low)	_	1	_	μS	-40°C to +85°C	

**Note 1:** These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

# 64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]



### DETAIL 1

	Units	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Number of Leads	N		64		
Lead Pitch	е		0.50 BSC		
Overall Height	Α	-	-	1.20	
Molded Package Thickness	A2	0.95	1.00	1.05	
Standoff	A1	0.05	-	0.15	
Foot Length	L	0.45	0.60	0.75	
Footprint	L1	1.00 REF			
Foot Angle	ø	0°	3.5°	7°	
Overall Width	E		12.00 BSC		
Overall Length	D		12.00 BSC		
Molded Package Width	E1		10.00 BSC		
Molded Package Length	D1		10.00 BSC		
Lead Thickness	С	0.09	-	0.20	
Lead Width	b	0.17	0.22	0.27	
Mold Draft Angle Top	α	11°	12°	13°	
Mold Draft Angle Bottom	β	11°	12°	13°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or

protrusions shall not exceed 0.25mm per side. 4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е	0.50 BSC		
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

# 121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







DETAIL B

	Units	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Number of Contacts	Ν		121		
Contact Pitch	е		0.80 BSC		
Overall Height	Α	1.00	1.10	1.20	
Ball Height	A1	0.25	0.30	0.35	
Overall Width	E		10.00 BSC		
Array Width	E1		8.00 BSC		
Overall Length	D	10.00 BSC			
Array Length	D1	8.00 BSC			
Contact Diameter	b	0.35	0.40	0.45	

Notes:

- 1. Ball A1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 3. The outer rows and colums of balls are located with respect to datums A and B.
- 4. Ball interface to package body: 0.37mm nominal diameter.

Microchip Technology Drawing C04-148 Rev F Sheet 2 of 2

## 121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimensior	n Limits	MIN	NOM	MAX	
Contact Pitch	E1		0.80 BSC		
Contact Pitch	E2		0.80 BSC		
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Diameter (X121)	X			0.32	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D

# PIC32MX5XX/6XX/7XX

SPIx Slave Mode (CKE = 1)379	1
Timer1, 2, 3, 4, 5 External Clock	
UART Reception	
UART Transmission (8-bit or 9-bit Data)	
Timing Requirements	
CLKO and I/O	1
Timing Specifications	
CAN I/O Requirements	
I2Cx Bus Data Requirements (Master Mode)	
I2Cx Bus Data Requirements (Slave Mode)	
Input Capture Requirements	
Output Compare Requirements	
Simple OCx/PWM Mode Requirements	,
SPIx Master Mode (CKE = 0) Requirements	i
SPIx Master Mode (CKE = 1) Requirements	
SPIx Slave Mode (CKE = 1) Requirements	,
SPIx Slave Mode Requirements (CKE = 0)	

# U

UART	
USB On-The-Go (OTG)	

# V

VCAP pin	
Voltage Reference Specifications	365
Voltage Regulator (On-Chip)	343

# W

Watchdog Timer (WDT)	
WWW Address	
WWW, On-Line Support	