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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx775f256lt-80i-bg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 3: PIC32MX7XX USB, ETHERNET, AND CAN FEATURES

	USB, Ethernet, and CAN																
Device	Pins	Program Memory (KB)	Data Memory (KB)	USB	Ethernet	CAN	Timers/Capture/Compare	DMA Channels (Program mable/Dedicated)	UART ^(2,3)	SPI ⁽³⁾	l ² C ⁽³⁾	10-bit 1 Msps ADC (Channels)	Comparators	PMP/PSP	JTAG	Trace	Packages ⁽⁴⁾
PIC32MX764F128H	64	128 + 12 ⁽¹⁾	32	1	1	1	5/5/5	4/8	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX775F256H	64	256 + 12 ⁽¹⁾	64	1	1	2	5/5/5	8/8	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX775F512H	64	512 + 12 ⁽¹⁾	64	1	1	2	5/5/5	8/8	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX795F512H	64	512 + 12 ⁽¹⁾	128	1	1	2	5/5/5	8/8	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX764F128L	100	128 + 12 ⁽¹⁾	32	1	1	1	5/5/5	4/6	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX775F256L	100	256 + 12 ⁽¹⁾	64	1	1	2	5/5/5	8/8	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX775F512L	100	512 + 12 ⁽¹⁾	64	1	1	2	5/5/5	8/8	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX795F512L	100	512 + 12 ⁽¹⁾	128	1	1	2	5/5/5	8/8	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG, TL

Legend: PF, PT = TQFP

MR = QFN

BG = TFBGA

 $TL = VTLA^{(5)}$

Note 1: This device features 12 KB boot Flash memory.

^{2:} CTS and RTS pins may not be available for all UART modules. Refer to the "Device Pin Tables" section for more information.

^{3:} Some pins between the UART, SPI and I²C modules may be shared. Refer to the "Device Pin Tables" section for more information.

^{4:} Refer to Section 34.0 "Packaging Information" for more information.

^{5: 100-}pin devices other than those listed here are available in the VTLA package upon request. Please contact your local Microchip Sales Office for details.

Device Pin Tables

TABLE 4: PIN NAMES FOR 64-PIN USB AND CAN DEVICES

64-PIN QFN⁽²⁾ AND TQFP (TOP VIEW)

PIC32MX534F064H PIC32MX564F064H PIC32MX564F128H PIC32MX575F256H PIC32MX575F512H

64 1

QFN⁽²⁾
64
TQFP

Pin#	Full Pin Name
1	PMD5/RE5
2	PMD6/RE6
3	PMD7/RE7
4	SCK2/U6TX/U3RTS/PMA5/CN8/RG6
5	SDA4/SDI2/U3RX/PMA4/CN9/RG7
6	SCL4/SDO2/U3TX/PMA3/CN10/RG8
7	MCLR
8	SS2/U6RX/U3CTS/PMA2/CN11/RG9
9	Vss
10	VDD
11	AN5/C1IN+/VBUSON/CN7/RB5
12	AN4/C1IN-/CN6/RB4
13	AN3/C2IN+/CN5/RB3
14	AN2/C2IN-/CN4/RB2
15	PGEC1/AN1/VREF-/CVREF-/CN3/RB1
16	PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0
17	PGEC2/AN6/OCFA/RB6
18	PGED2/AN7/RB7
19	AVDD
20	AVss
21	AN8/SS4/U5RX/U2CTS/C1OUT/RB8
22	AN9/C2OUT/PMA7/RB9
23	TMS/AN10/CVREFOUT/PMA13/RB10
24	TDO/AN11/PMA12/RB11
25	Vss
26	VDD
27	TCK/AN12/PMA11/RB12
28	TDI/AN13/PMA10/RB13
29	AN14/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14
30	AN15/OCFB/PMALL/PMA0/CN12/RB15
31	AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4
32	AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5

Pin # Full Pin Name		
34 VBUS 35 VUSB3V3 36 D-/RG3 37 D+/RG2 38 VDD 39 OSC1/CLKI/RC12 40 OSC2/CLKO/RC15 41 VSS 42 RTCC/IC1/INT1/RD8 43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	Pin#	Full Pin Name
35 VUSB3V3 36 D-/RG3 37 D+/RG2 38 VDD 39 OSC1/CLKI/RC12 40 OSC2/CLKO/RC15 41 Vss 42 RTCC/IC1/INT1/RD8 43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	33	USBID/RF3
36 D-/RG3 37 D+/RG2 38 VDD 39 OSC1/CLKI/RC12 40 OSC2/CLKO/RC15 41 Vss 42 RTCC/IC1/INT1/RD8 43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	34	VBUS
37 D+/RG2 38 VDD 39 OSC1/CLKI/RC12 40 OSC2/CLKO/RC15 41 Vss 42 RTCC/IC1/INT1/RD8 43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	35	VUSB3V3
38 VDD 39 OSC1/CLKI/RC12 40 OSC2/CLKO/RC15 41 Vss 42 RTCC/IC1/INT1/RD8 43 \$\overline{SS3}/U4RX/\overline{U1CTS}/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/\overline{U1RTS}/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	36	D-/RG3
39 OSC1/CLKI/RC12 40 OSC2/CLKO/RC15 41 Vss 42 RTCC/IC1/INT1/RD8 43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	37	D+/RG2
40 OSC2/CLKO/RC15 41 Vss 42 RTCC/IC1/INT1/RD8 43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	38	VDD
41 Vss 42 RTCC/IC1/INT1/RD8 43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VcAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	39	OSC1/CLKI/RC12
42 RTCC/IC1/INT1/RD8 43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	40	OSC2/CLKO/RC15
43 SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	41	Vss
44 SCL1/IC3/PMCS2/PMA15/INT3/RD10 45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/\textstyle{	42	RTCC/IC1/INT1/RD8
45 IC4/PMCS1/PMA14/INT4/RD11 46 OC1/INT0/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	43	SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9
46 OC1/INTO/RD0 47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD3/RE3	44	SCL1/IC3/PMCS2/PMA15/INT3/RD10
47 SOSCI/CN1/RC13 48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/Ū1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VcAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD3/RE3	45	IC4/PMCS1/PMA14/INT4/RD11
48 SOSCO/T1CK/CN0/RC14 49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	46	OC1/INT0/RD0
49 SCK3/U4TX/U1RTS/OC2/RD1 50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	47	SOSCI/CN1/RC13
50 SDA3/SDI3/U1RX/OC3/RD2 51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD3/RE3	48	SOSCO/T1CK/CN0/RC14
51 SCL3/SDO3/U1TX/OC4/RD3 52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD3/RE3	49	SCK3/U4TX/U1RTS/OC2/RD1
52 OC5/IC5/PMWR/CN13/RD4 53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	50	SDA3/SDI3/U1RX/OC3/RD2
53 PMRD/CN14/RD5 54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	51	SCL3/SDO3/U1TX/OC4/RD3
54 CN15/RD6 55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	52	OC5/IC5/PMWR/CN13/RD4
55 CN16/RD7 56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	53	PMRD/CN14/RD5
56 VCAP 57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	54	CN15/RD6
57 VDD 58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	55	CN16/RD7
58 C1RX/RF0 59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	56	VCAP
59 C1TX/RF1 60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	57	VDD
60 PMD0/RE0 61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	58	C1RX/RF0
61 PMD1/RE1 62 PMD2/RE2 63 PMD3/RE3	59	C1TX/RF1
62 PMD2/RE2 63 PMD3/RE3	60	PMD0/RE0
63 PMD3/RE3	61	PMD1/RE1
	62	PMD2/RE2
64 PMD4/RE4	63	PMD3/RE3
	64	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

Table of Contents

1.0	Device Overview	25
2.0	Guidelines for Getting Started with 32-bit MCUs	37
3.0	CPU	41
4.0	Memory Organization	47
5.0	Flash Program Memory	63
6.0	Resets	
7.0	Interrupt Controller	73
8.0	Oscillator Configuration	95
9.0	Prefetch Cache	101
10.0	Direct Memory Access (DMA) Controller	111
11.0	USB On-The-Go (OTG)	133
12.0	VO Ports	157
13.0	Timer1	167
14.0	Timer2/3, Timer4/5	171
15.0	Watchdog Timer (WDT)	177
16.0	Input Capture	181
17.0	Output Compare	185
18.0	Serial Peripheral Interface (SPI)	189
19.0	Inter-Integrated Circuit (I ² C)	195
20.0	Universal Asynchronous Receiver Transmitter (UART)	203
21.0	Parallel Master Port (PMP)	211
22.0	Real-Time Clock and Calendar (RTCC)	221
23.0	10-bit Analog-to-Digital Converter (ADC)	231
24.0	Controller Area Network (CAN)	241
25.0	Ethernet Controller	279
26.0	Comparator	323
27.0	Comparator Voltage Reference (CVREF)	327
28.0	Power-Saving Features	331
29.0	Special Features	333
30.0	Instruction Set	345
31.0	Development Support	347
32.0	Electrical Characteristics	351
	DC and AC Device Characteristics Graphs	
34.0	Packaging Information	401
The N	Microchip Web Site	437
Custo	omer Change Notification Service	437
Custo	omer Support	437
חיים או	ust Identification System	120

REGISTER 10-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	_	_	_	_	_	_	-	_		
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	_	_	_	_	_	_	_	_		
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
15:8	CHSPTR<15:8>									
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
7:0		_		CHSPTF	R<7:0>	_				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSPTR<15:0>: Channel Source Pointer bits

111111111111111 = Points to byte 65,535 of the source

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0000000000000000 = Points to byte 1 of the source 000000000000000 = Points to byte 0 of the source

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 10-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
		_	_	_	_		_	_			
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:16		_	_	_	_		_	_			
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
15.6	CHDPTR<15:8>										
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
7:0				CHDPTF	R<7:0>						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHDPTR<15:0>: Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination

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REGISTER 11-4: U10TGCON: USB OTG CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	_	_	_	_	-
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	-	-	_		-	-	-	1
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	_	_	_	-
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

Legend:

bit 6

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 DPPULUP: D+ Pull-Up Enable bit

1 = D+ data line pull-up resistor is enabled

0 = D+ data line pull-up resistor is disabled

DMPULUP: D- Pull-Up Enable bit

1 = D- data line pull-up resistor is enabled0 = D- data line pull-up resistor is disabled

bit 5 DPPULDWN: D+ Pull-Down Enable bit

1 = D+ data line pull-down resistor is enabled0 = D+ data line pull-down resistor is disabled

bit 4 DMPULDWN: D- Pull-Down Enable bit

1 = D- data line pull-down resistor is enabled

0 = D- data line pull-down resistor is disabled

bit 3 VBUSON: VBUS Power-on bit

1 = VBUS line is powered

0 = VBUS line is not powered

bit 2 OTGEN: OTG Functionality Enable bit

1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control

0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 VBUSCHG: VBUS Charge Enable bit

1 = VBUS line is charged through a pull-up resistor

0 = VBUS line is not charged through a resistor

bit 0 VBUSDIS: VBUS Discharge Enable bit

1 = VBUS line is discharged through a pull-down resistor

0 = VBUS line is not discharged through a resistor

REGISTER 11-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	_	-	_	-	_	-	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	1	1	1		1	1	1	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	_	_	_	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	LSPDEN			D	EVADDR<6:0)>		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 LSPDEN: Low-Speed Enable Indicator bit

1 = Next token command to be executed at low-speed0 = Next token command to be executed at full-speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 11-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_	_	_	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_				1	-	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
13.6	_	_	-	-	-	1	-	_
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				FRML	.<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 FRML<7:0>: 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 20-2: UxSTA: UARTX STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0			
31:24	_	_	_		_	-	_	ADM_EN			
22.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:16	ADDR<7:0>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R-0	R-1			
15:8	UTXISE	L<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT			
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0, HS	R-0			
	URXISE	L<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA			

Legend:HS = Set by hardwareHC = Cleared by hardwareR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-25 Unimplemented: Read as '0'

bit 24 ADM EN: Automatic Address Detect Mode Enable bit

1 = Automatic Address Detect mode is enabled

0 = Automatic Address Detect mode is disabled

bit 23-16 ADDR<7:0>: Automatic Address Mask bits

When the ADM_EN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 UTXISEL<1:0>: TX Interrupt Mode Selection bits

11 = Reserved, do not use

10 = Interrupt is generated and asserted while the transmit buffer is empty

01 = Interrupt is generated and asserted when all characters have been transmitted

00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 UTXINV: Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):

1 = UxTX Idle state is '0'

0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):

1 = IrDA encoded UxTX Idle state is '1'

0 = IrDA encoded UxTX Idle state is '0'

bit 12 URXEN: Receiver Enable bit

1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)

0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module. UxRX pin is controlled by port.

bit 11 UTXBRK: Transmit Break bit

1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion.

0 = Break transmission is disabled or completed

bit 10 UTXEN: Transmit Enable bit

1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)

0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset. UxTX pin is controlled by port.

bit 9 UTXBF: Transmit Buffer Full Status bit (read-only)

1 = Transmit buffer is full

0 = Transmit buffer is not full, at least one more character can be written

REGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		_	_	_			_	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	-	_	-	-	_	-	_	_
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ADRC	_	_			SAMC<4:0> ⁽¹⁾		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
7:0				ADCS<	7:0> ⁽²⁾			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 ADRC: ADC Conversion Clock Source bit

1 = Clock derived from FRC

0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 Unimplemented: Read as '0'

bit 12-8 **SAMC<4:0>**: Auto-Sample Time bits⁽¹⁾

11111 = 31 TAD

•

00001 = 1 TAD

00000 = 0 TAD (Not allowed)

bit 7-0 ADCS<7:0>: ADC Conversion Clock Select bits⁽²⁾

11111111 =TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD

.

.

•

00000001 =TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD 00000000 =TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.

2: This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

REGISTER 24-16: CIFLTCON6: CAN FILTER CONTROL REGISTER 6 (CONTINUED)

```
bit 15
          FLTEN25: Filter 25 Enable bit
          1 = Filter is enabled
          0 = Filter is disabled
bit 14-13 MSEL25<1:0>: Filter 25 Mask Select bits
          11 = Acceptance Mask 3 selected
          10 = Acceptance Mask 2 selected
          01 = Acceptance Mask 1 selected
          00 = Acceptance Mask 0 selected
          FSEL25<4:0>: FIFO Selection bits
bit 12-8
          11111 = Message matching filter is stored in FIFO buffer 31
          11110 = Message matching filter is stored in FIFO buffer 30
          00001 = Message matching filter is stored in FIFO buffer 1
          00000 = Message matching filter is stored in FIFO buffer 0
bit 7
          FLTEN24: Filter 24 Enable bit
          1 = Filter is enabled
          0 = Filter is disabled
bit 6-5
          MSEL24<1:0>: Filter 24 Mask Select bits
          11 = Acceptance Mask 3 selected
          10 = Acceptance Mask 2 selected
          01 = Acceptance Mask 1 selected
          00 = Acceptance Mask 0 selected
          FSEL24<4:0>: FIFO Selection bits
bit 4-0
          11111 = Message matching filter is stored in FIFO buffer 31
          11110 = Message matching filter is stored in FIFO buffer 30
          00001 = Message matching filter is stored in FIFO buffer 1
          00000 = Message matching filter is stored in FIFO buffer 0
```

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 25-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	-	-	_	-	
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.16	_	_	_	-	-	_	-	
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15.6	_	TXBUSE	RXBUSE	_	_	_	EWMARK	FWMARK
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONE	PKTPEND	RXACT	_	TXDONE	TXABORT	RXBUFNA	RXOVFLW

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-15 Unimplemented: Read as '0'

bit 14 **TXBUSE:** Transmit BVCI Bus Error Interrupt bit

1 = BVCI Bus Error has occurred

0 = BVCI Bus Error has not occurred

This bit is set when the TX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 13 RXBUSE: Receive BVCI Bus Error Interrupt bit

1 = BVCI Bus Error has occurred

0 = BVCI Bus Error has not occurred

This bit is set when the RX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 12-10 Unimplemented: Read as '0'

bit 9 **EWMARK:** Empty Watermark Interrupt bit

1 = Empty Watermark pointer reached

0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a '0' or a '1' has no effect.

bit 8 FWMARK: Full Watermark Interrupt bit

1 = Full Watermark pointer reached

0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 7 RXDONE: Receive Done Interrupt bit

1 = RX packet was successfully received

0 = No interrupt pending

This bit is set whenever an RX packet is successfully received. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

Note: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-17: ETHFRMTXOK: ETHERNET CONTROLLER FRAMES TRANSMITTED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	_	_	_	_	_	_		-	
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	_	_	_	_	_	_		-	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15.6	FRMTXOKCNT<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
				FRMTXOK	(CNT<7:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 **FRMTXOKCNT<15:0>:** Frame Transmitted OK Count bits Increment counter for frames successfully transmitted.

Note 1: This register is only used for TX operations.

- 2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.
- **3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	_	_	-	_	_	_	-		
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	_	_	-	_	_	_	-		
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	FRMRXOKCNT<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
				FRMRXO	(CNT<7:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 FRMRXOKCNT<15:0>: Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

- **Note 1:** This register is only used for RX operations.
 - 2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.
 - 3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-36: EMAC1MIND: ETHERNET CONTROLLER MAC MII MANAGEMENT INDICATORS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	_	_	_	-	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	_	_	-	_
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_	_	LINKFAIL	NOTVALID	SCAN	MIIMBUSY

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-4 Unimplemented: Read as '0'

bit 3 LINKFAIL: Link Fail bit

When '1' is returned - indicates link fail has occurred. This bit reflects the value last read from the PHY status register.

bit 2 NOTVALID: MII Management Read Data Not Valid bit

When '1' is returned - indicates an MII management read cycle has not completed and the Read Data is not yet valid.

bit 1 SCAN: MII Management Scanning bit

When '1' is returned - indicates a scan operation (continuous MII Management Read cycles) is in progress.

bit 0 MIIMBUSY: MII Management Busy bit

When '1' is returned - indicates MII Management module is currently performing an MII Management Read or Write cycle.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

29.2 On-Chip Voltage Regulator

All PIC32MX5XX/6XX/7XX devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX-5XX/6XX/7XX family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 29-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 32.1** "**DC Characteristics**".

Note: It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

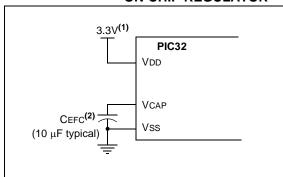
29.2.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

29.2.2 ON-CHIP REGULATOR AND BOR

PIC32MX5XX/6XX/7XX devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset (BOR). This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specified in **Section 32.1 "DC Characteristics"**.

FIGURE 29-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



Note 1: These are typical operating voltages. Refer to Section 32.1 "DC Characteristics" for the full operating ranges of VDD.

2: It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

29.3 Programming and Diagnostics

PIC32MX5XX/6XX/7XX devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 29-2: PROGRAMMING,
DEBUGGING, AND TRACE
PORTS BLOCK DIAGRAM

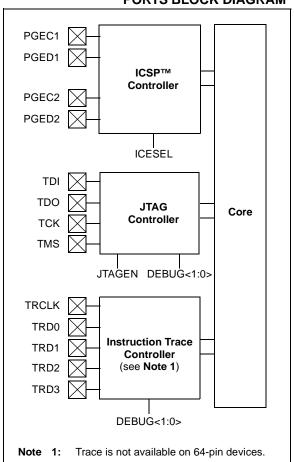
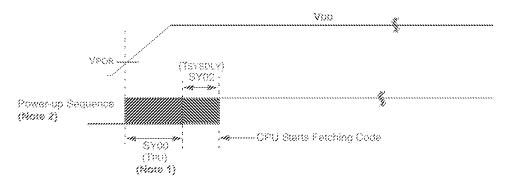
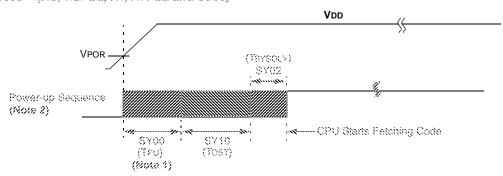


FIGURE 32-4: POWER-ON RESET TIMING CHARACTERISTICS

Internal Voltage Regulator Enabled
Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)



Internal Voltage Regulator Enabled Clock Sources = (NS, MSPLL, XT, XTPLL and Sosc)



Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR (VDD < VDDMIN).

2: Includes interval voltage regulator stabilization delay.

FIGURE 32-25: PARALLEL SLAVE PORT TIMING

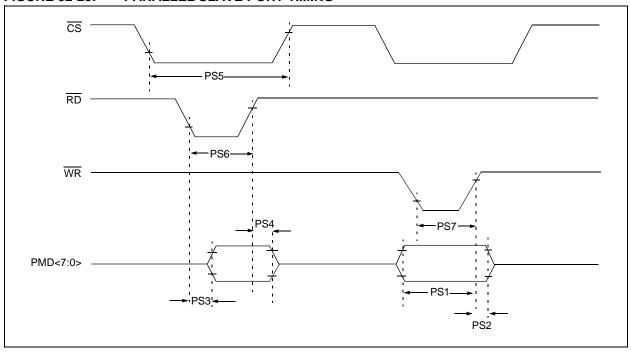


TABLE 32-39: PARALLEL SLAVE PORT REQUIREMENTS

AC CHA	ARACTERIS	STICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PS1	TdtV2wrH	Data In Valid before WR or CS Inactive (setup time)	20	_	_	ns	_
PS2	TwrH2dtl	WR or CS Inactive to Data-In Invalid (hold time)	40	_	_	ns	_
PS3	TrdL2dtV	RD and CS Active to Data-Out Valid	_	_	60	ns	_
PS4	TrdH2dtl	RD Active or CS Inactive to Data-Out Invalid	0	_	10	ns	_
PS5	Tcs	CS Active Time	TpB + 40	_	_	ns	_
PS6	Twr	WR Active Time	TPB + 25	_		ns	_
PS7	TRD	RD Active Time	TPB + 25	_	_	ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

DS60001156J-page 399

33.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 33-1: VOH – 4x DRIVER PINS

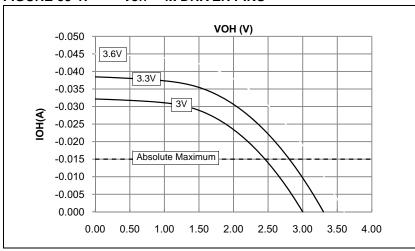


FIGURE 33-3: VOL - 4x DRIVER PINS VOL (V) 0.050 3.6V 0.045 0.040 3.3V 0.035 3V 0.030 IOH(A) 0.025 0.020 Absolute Maximum 0.015 0.010 0.005 0.000 0.50 1.00 1.50 2.00 2.50 3.00 3.50

FIGURE 33-2: VoH – 8x DRIVER PINS

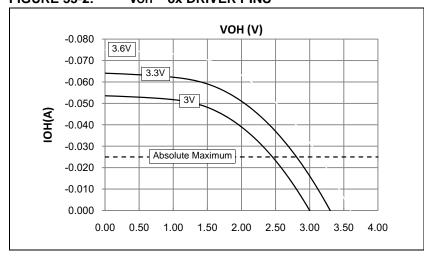


FIGURE 33-4: Vol – 8x DRIVER PINS

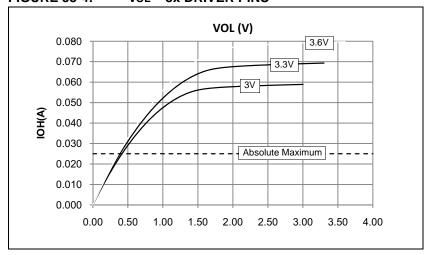


TABLE B-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
4.0 "Memory Organization"	Updated all register tables to include the Virtual Address and All Resets
	columns.
	Updated the title of Figure 4-4 to include the PIC32MX575F256L device.
	Updated the title of Figure 4-6 to include the PIC32MX695F512L and PIC32MX695F512H devices. Also changed PIC32MX795F512L to PIC32MX795F512H.
	Updated the title of Table 4-3 to include the PIC32MX695F512H device.
	Updated the title of Table 4-5 to include the PIC32MX575F5256L device.
	Updated the title of Table 4-6 to include the PIC32MX695F512L device.
	Reversed the order of Table 4-11 and Table 4-12.
	Reversed the order of Table 4-14 and Table 4-15.
	Updated the title of Table 4-15 to include the PIC32MX575F256L and PIC32MX695F512L devices.
	Updated the title of Table 4-45 to include the PIC32MX575F256L device.
	Updated the title of Table 4-47 to include the PIC32MX695F512H and PIC32MX695F512L devices.
1.0 "I/O Ports"	Updated the second paragraph of 1.1.2 "Digital Inputs" and removed Table 12-1.
22.0 "10-bit Analog-to-Digital Converter (ADC)"	Updated the ADC Conversion Clock Period Block Diagram (see Figure 22-2).
1.0 "Special Features"	Removed references to the ENVREG pin in 1.3 "On-Chip Voltage Regulator".
	Updated the first sentence of 1.3.1 "On-Chip Regulator and POR" and 1.3.2 "On-Chip Regulator and BOR".
	Updated the Connections for the On-Chip Regulator (see Figure 1-2).
1.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings and added Note 3.
	Added Thermal Packaging Characteristics for the 121-pin XBGA package (see Table 1-3).
	Updated the Operating Current (IDD) DC Characteristics (see Table 1-5).
	Updated the Idle Current (IIDLE) DC Characteristics (see Table 1-6).
	Updated the Power-Down Current (IPD) DC Characteristics (see Table 1-7).
	Removed Note 1 from the Program Flash Memory Wait State Characteristics (see Table 1-12).
	Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics, changing SP52 to SP35 between the MSb and Bit 14 on SDOx (see Figure 1-13).
1.0 "Packaging Information"	Added the 121-pin XBGA package marking information and package details.
"Product Identification System"	Added the definition for BG (121-lead 10x10x1.1 mm, XBGA).
	Added the definition for Speed.

TABLE B-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
4.0 "Memory Organization" (Continued)	Made the following bit name changes in the I2C1, I2C3, I2C4 and I2C5 Register Map (Table 4-11):
	 I2C3BRG SFR: I2C1BRG was changed to I2C3BRG I2C4BRG SFR: I2C1BRG was changed to I2C4BRG I2C5BRG SFR: I2C1BRG was changed to I2C5BRG I2C4TRN SFR: I2CT1DATA was changed to I2CT2ADATA I2C4RCV SFR: I2CR2DATA was changed to I2CR2ADATA I2C5TRN SFR: I2CT1DATA was changed to I2CT3ADATA I2C5RCV SFR: I2CR1DATA was changed to I2CR3ADATA
	Added the RTSMD bit and UEN<1:0> bits to the UART1A, UART1B, UART2A, UART2B, UART3A and UART3B Register Map (Table 4-13)
	Added the SIDL bit to the DMA Global Register Map (Table 4-17).
	Changed the CM bit to CMR in the System Control Register Map (Table 4-23).
	Added the following devices to the I2C2, SPI1, PORTA, PORTC, PORTD, PORTE, PORTF, PORTG, Change Notice and Pull-up Register Maps (Table 4-12, Table 4-14, Table 4-24, Table 4-27, Table 4-29, Table 4-31, Table 4-33, Table 4-35 and Table 4-36):
	 PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX664F064L PIC32MX664F128L PIC32MX764F128L
	Added the following devices to the PORTC, PORTD, PORTE, PORTF, PORTG, Change Notice and Pull-up Register Maps (Table 4-26, Table 4-28, Table 4-30, Table 4-32, Table 4-34 and Table 4-37):
	 PIC32MX534F064H PIC32MX564F064H PIC32MX564F128H PIC32MX664F064H PIC32MX664F128H PIC32MX764F128H
	Added the following devices to the CAN1 Register Map (Table 4-45):
	 PIC32MX534F064H PIC32MX564F064H PIC32MX564F128H PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX764F128L
	Added the following devices to the Ethernet Controller Register Map (Table 4-47):
	 PIC32MX664F064H PIC32MX664F128H PIC32MX664F064L PIC32MX664F128L
	• PIC32MX764F128L

Oscillator Configuration95	CiFLTCON4 (CAN Filter Control 4)
Output Compare185	CiFLTCON5 (CAN Filter Control 5)
P	CiFLTCON6 (CAN Filter Control 6)
	CiFLTCON7 (CAN Filter Control 7)
Packaging401	CiFSTAT (CAN FIFO Status)
Details	CilNT (CAN Interrupt)
Marking	CiRXFn (CAN Acceptance Filter 'n')272
Parallel Master Port (PMP)211	CiRXMn (CAN Acceptance Filter Mask 'n') 255
PIC32 Family USB Interface Diagram	CiRXOVF (CAN Receive FIFO Overflow Status) 254
PICkit 3 In-Circuit Debugger/Programmer349	CiTMR (CAN Timer)254
Pinout I/O Descriptions (table)26	CiTREC (CAN Transmit/Receive Error Count) 253
Power-on Reset (POR)	CiVEC (CAN Interrupt Code)252
and On-Chip Voltage Regulator343	CMSTAT (Comparator Control Register)326
Power-Saving Features331	CMxCON (Comparator 'x' Control)325
CPU Halted Methods331	CNCON (Change Notice Control)166
Operation	CVRCON (Comparator Voltage Reference Control) 329
with CPU Running331	DCHxCON (DMA Channel 'x' Control) 124
Prefetch Cache101	DCHxCPTR (DMA Channel 'x' Cell Pointer)131
Program Flash Memory	DCHxCSIZ (DMA Channel 'x' Cell-Size) 131
Wait State Characteristics363	DCHxDAT (DMA Channel 'x' Pattern Data)132
R	DCHxDPTR (Channel 'x' Destination Pointer) 130
	DCHxDSA (DMA Channel 'x' Destination
Real-Time Clock and Calendar (RTCC)221	Start Address)128
Register Maps55–283	DCHxDSIZ (DMA Channel 'x' Destination Size) 129
Registers	DCHxECON (DMA Channel 'x' Event Control) 125
AD1CHS (ADC Input Select)239	DCHxINT (DMA Channel 'x' Interrupt Control) 126
AD1CON1 (ADC Control 1)235	DCHxSPTR (DMA Channel 'x' Source Pointer) 130
AD1CON2 (ADC Control 2)237	DCHxSSA (DMA Channel 'x' Source Start Address) 128
AD1CON3 (ADC Control 3)238	DCHxSSIZ (DMA Channel 'x' Source Size) 129
AD1CSSL (ADC Input Scan Select)240	DCRCCON (DMA CRC Control)121
ALRMDATE (Alarm Date Value)230	DCRCDATA (DMA CRC Data)123
ALRMTIME (Alarm Time Value)229	DCRCXOR (DMA CRCXOR Enable) 123
BMXBOOTSZ (Boot Flash (IFM) Size)61	DDPCON (Debug Data Port Control)342
BMXCON (Bus Matrix Configuration)56	DEVCFG0 (Device Configuration Word 0
BMXDKPBA (Data RAM Kernel Program	DEVCFG1 (Device Configuration Word 1
Base Address)57	DEVCFG2 (Device Configuration Word 2
BMXDRMSZ (Data RAM Size)60	DEVCFG3 (Device Configuration Word 3341
BMXDUDBA (Data RAM User Data Base Address) 58	DEVID (Device and Revision ID)
BMXDUPBA (Data RAM User Program	DMAADDR (DMA Address)120
Base Address)59	DMACON (DMA Controller Control) 119
BMXPFMSZ (Program Flash (PFM) Size)61	DMASTAT (DMA Status)120
BMXPUPBA (Program Flash (PFM) User Program	EMAC1CFG1 (Ethernet Controller MAC Configuration 1)
Base Address)60	306
CHEACC (Cache Access)104	EMAC1CFG2 (Ethernet Controller MAC Configuration 2)
CHECON (Cache Control)103	307
CHEHIT (Cache Hit Statistics)109	EMAC1CLRT (Ethernet Controller MAC Collision Win-
CHELRU (Cache LRU)108	dow/Retry Limit)311
CHEMIS (Cache Miss Statistics)109	EMAC1IPGR (Ethernet Controller MAC Non-Back-to-
CHEMSK (Cache TAG Mask)106	Back Interpacket Gap)310
CHETAG (Cache TAG)105	EMAC1IPGT (Ethernet Controller MAC Back-to-Back In-
CHEW0 (Cache Word 0)106	terpacket Gap)309
CHEW1 (Cache Word 1)107	EMAC1MADR (Ethernet Controller MAC MII Manage-
CHEW2 (Cache Word 2)107	ment Address)
CHEW3 (Cache Word 3)108	EMAC1MAXF (Ethernet Controller MAC Maximum
CiCFG (CAN Baud Rate Configuration)248	Frame Length) 312
CiCON (CAN Module Control)246	EMAC1MCFG (Ethernet Controller MAC MII Manage-
CiFIFOBA (CAN Message Buffer Base Address) 273	ment Configuration)
CiFIFOCINn (CAN Module Message Index Register 'n')	EMAC1MCMD (Ethernet Controller MAC MII Manage-
278	ment Command)316
CiFIFOCONn (CAN FIFO Control Register 'n')274	EMAC1MIND (Ethernet Controller MAC MII Manage-
CiFIFOINTn (CAN FIFO Interrupt Register 'n') 276	ment Indicators)319
CiFIFOUAn (CAN FIFO User Address Register 'n')278	EMAC1MRDD (Ethernet Controller MAC MII Manage-
CiFLTCON0 (CAN Filter Control 0)256	ment Read Data)318
CiFLTCON1 (CAN Filter Control 1)258	EMAC1MWTD (Ethernet Controller MAC MII Manage-
CiFLTCON2 (CAN Filter Control 2)260	
CiELTCON3 (CAN Filter Control 3) 262	ment Write Data)318