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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx775f512h-80v-pt

TABLE 8: PIN NAMES FOR 100-PIN USB AND ETHERNET DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MX664F064L
 PIC32MX664F128L
 PIC32MX675F256L
 PIC32MX675F512L
 PIC32MX695F512L

100

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Pin #	Full Pin Name	Pin #	Full Pin Name
71	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	86	VDD
72	SDO1/OC1/INT0/RD0	87	ETXD1/PMD11/RF0
73	SOSCI/CN1/RC13	88	ETXD0/PMD10/RF1
74	SOSCO/T1CK/CN0/RC14	89	ETXERR/PMD9/RG1
75	Vss	90	PMD8/RG0
76	OC2/RD1	91	TRCLK/RA6
77	OC3/RD2	92	TRD3/RA7
78	OC4/RD3	93	PMD0/RE0
79	ETXD2/IC5/PMD12/RD12	94	PMD1/RE1
80	ETXD3/PMD13/CN19/RD13	95	TRD2/RG14
81	OC5/PMWR/CN13/RD4	96	TRD1/RG12
82	PMRD/CN14/RD5	97	TRD0/RG13
83	ETXEN/PMD14/CN15/RD6	98	PMD2/RE2
84	ETXCLK/PMD15/CN16/RD7	99	PMD3/RE3
85	VCAP/VDDCORE	100	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

NOTES:

REGISTER 14-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

bit 3	T32: 32-Bit Timer Mode Select bit ⁽²⁾ 1 = Odd numbered and even numbered timers form a 32-bit timer 0 = Odd numbered and even numbered timers form a separate 16-bit timer
bit 2	Unimplemented: Read as '0'
bit 1	TCS: Timer Clock Source Select bit ⁽³⁾ 1 = External clock from TxCK pin 0 = Internal peripheral clock
bit 0	Unimplemented: Read as '0'

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit is only available on even numbered timers (Timer2 and Timer4).
- 3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, and Timer5). All timer functions are set through the even numbered timers.
- 4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON ^(1,2)	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	—	SWDTPS<4:0>					WDTWINEN	WDTCLR

Legend:

y = Values set from Configuration bits on POR
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit^(1,2)

1 = Enables the WDT if it is not enabled by the device configuration
0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit

1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit

1 = Writing a '1' will clear the WDT
0 = Software cannot force this bit to a '0'

- Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
2: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

bit 2-0 **ICM<2:0>**: Input Capture Mode Select bits

- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode – every sixteenth rising edge
- 100 = Prescaled Capture Event mode – every fourth rising edge
- 011 = Simple Capture Event mode – every rising edge
- 010 = Simple Capture Event mode – every falling edge
- 001 = Edge Detect mode – every edge (rising and falling)
- 000 = Input Capture module is disabled

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 17-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON ⁽¹⁾	U-0 —	R/W-0 SIDL	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	U-0 —	U-0 —	R/W-0 OC32	R-0 OCFLT ⁽²⁾	R/W-0 OCTSEL	OCM<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Module On bit⁽¹⁾

1 = Output Compare module is enabled

0 = Output Compare module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue operation when CPU enters Idle mode

0 = Continue operation when CPU is in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit

1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source

0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit⁽²⁾

1 = PWM Fault condition has occurred (only cleared in hardware)

0 = PWM Fault condition has not occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit

1 = Timer3 is the clock source for this Output Compare module

0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits

111 = PWM mode on OCx; Fault pin enabled

110 = PWM mode on OCx; Fault pin disabled

101 = Initialize OCx pin low; generate continuous output pulses on OCx pin

100 = Initialize OCx pin low; generate single output pulse on OCx pin

011 = Compare event toggles OCx pin

010 = Initialize OCx pin high; compare event forces OCx pin low

001 = Initialize OCx pin low; compare event forces OCx pin high

000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only used when OCM<2:0> = 111. It is read as '0' in all other modes.

REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC ⁽³⁾	AMASK<3:0> ⁽²⁾			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0> ⁽²⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit^(1,2)

1 = Alarm is enabled

0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit⁽²⁾

1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF

0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽³⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.

When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit⁽³⁾

1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read.

The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain.

0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits⁽²⁾

1111 = Reserved

•
•
•

1010 = Reserved

1001 = Once a year (except when configured for February 29, once every four years)

1000 = Once a month

0111 = Once a week

0110 = Once a day

0101 = Every hour

0100 = Every 10 minutes

0011 = Every minute

0010 = Every 10 seconds

0001 = Every second

0000 = Every half-second

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is only reset on a Power-on Reset (POR).

REGISTER 24-11: CifLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)

bit 15 **FLTEN5**: Filter 17 Enable bit

- 1 = Filter is enabled
- 0 = Filter is disabled

bit 14-13 **MSEL5<1:0>**: Filter 5 Mask Select bits

- 11 = Acceptance Mask 3 selected
- 10 = Acceptance Mask 2 selected
- 01 = Acceptance Mask 1 selected
- 00 = Acceptance Mask 0 selected

bit 12-8 **FSEL5<4:0>**: FIFO Selection bits

- 11111 = Message matching filter is stored in FIFO buffer 31
- 11110 = Message matching filter is stored in FIFO buffer 30
-
-
-
- 00001 = Message matching filter is stored in FIFO buffer 1
- 00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4**: Filter 4 Enable bit

- 1 = Filter is enabled
- 0 = Filter is disabled

bit 6-5 **MSEL4<1:0>**: Filter 4 Mask Select bits

- 11 = Acceptance Mask 3 selected
- 10 = Acceptance Mask 2 selected
- 01 = Acceptance Mask 1 selected
- 00 = Acceptance Mask 0 selected

bit 4-0 **FSEL4<4:0>**: FIFO Selection bits

- 11111 = Message matching filter is stored in FIFO buffer 31
- 11110 = Message matching filter is stored in FIFO buffer 30
-
-
-
- 00001 = Message matching filter is stored in FIFO buffer 1
- 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 25-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 25/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	EXCESS DFR	BPNBOK OFF	NOBK OFF	—	—	LONGPRE	PUREPRE
7:0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	AUTO PAD ^(1,2)	VLAN PAD ^(1,2)	PAD ENABLE ^(1,3)	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **EXCESSDER:** Excess Defer bit

- 1 = The MAC will defer to carrier indefinitely as per the Standard
- 0 = The MAC will abort when the excessive deferral limit is reached

bit 13 **BPNBOKOFF:** Backpressure/No Backoff bit

- 1 = The MAC after incidentally causing a collision during backpressure will immediately retransmit without backoff reducing the chance of further collisions and ensuring transmit packets get sent
- 0 = The MAC will not remove the backoff

bit 12 **NOBKOFF:** No Backoff bit

- 1 = Following a collision, the MAC will immediately retransmit rather than using the Binary Exponential Backoff algorithm as specified in the Standard
- 0 = Following a collision, the MAC will use the Binary Exponential Backoff algorithm

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **LONGPRE:** Long Preamble Enforcement bit

- 1 = The MAC only allows receive packets which contain preamble fields less than 12 bytes in length
- 0 = The MAC allows any length preamble as per the Standard

bit 8 **PUREPRE:** Pure Preamble Enforcement bit

- 1 = The MAC will verify the content of the preamble to ensure it contains 0x55 and is error-free. A packet with errors in its preamble is discarded
- 0 = The MAC does not perform any preamble checking

bit 7 **AUTOPAD:** Automatic Detect Pad Enable bit^(1,2)

- 1 = The MAC will automatically detect the type of frame, either tagged or untagged, by comparing the two octets following the source address with 0x8100 (VLAN Protocol ID) and pad accordingly
- 0 = The MAC does not perform automatic detection

Note 1: Table 25-6 provides a description of the pad function based on the configuration of this register.

2: This bit is ignored if the PADENABLE bit is cleared.

3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

REGISTER 25-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	B2BIPKTGP<6:0>						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp			
Param. No.	Typical ⁽²⁾	Max.	Units	Conditions		
Power-Down Current (IPD) ⁽¹⁾ for PIC32MX575/675/695/775/795 Family Devices						
DC40	10	40	μA	-40°C	2.3V Base Power-Down Current (Note 6)	
DC40a	36	100		+25°C		
DC40b	400	720		+85°C		
DC40h	900	1800		+105°C		
DC40c	41	120		+25°C	3.3V Base Power-Down Current	
DC40d	22	80		-40°C	3.6V Base Power-Down Current (Note 6)	
DC40e	42	120		+25°C		
DC40g	315	400 ⁽⁵⁾		+70°C		
DC40f	410	800		+85°C		
DC40i	1000	2000		+105°C		
Module Differential Current for PIC32MX575/675/695/775/795 Family Devices						
DC41	—	10	μA	—	2.3V Watchdog Timer Current: ΔIWDT (Notes 3,6)	
DC41a	5	—			3.3V Watchdog Timer Current: ΔIWDT (Note 3)	
DC41b	—	20			3.6V Watchdog Timer Current: ΔIWDT (Note 3,6)	
DC42	—	40	μA	—	2.3V RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC (Notes 3,6)	
DC42a	23	—			3.3V RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC (Note 3)	
DC42b	—	50			3.6V RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC (Note 3,6)	
DC43	—	1300	μA	—	2.5V ADC: ΔIADC (Notes 3,4,6)	
DC43a	1100	—			3.3V ADC: ΔIADC (Notes 3,4)	
DC43b	—	1300			3.6V ADC: ΔIADC (Notes 3,4,6)	

Note 1: The test conditions for IPD current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0)
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to V_{SS}
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

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TABLE 32-18: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 2.3V TO 3.6V)

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	3.92	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes
OS51	FSYS	On-Chip VCO System Frequency	60	—	120	MHz	—
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	—
OS53	DCLK	CLKO Stability ⁽²⁾ (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 80 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{80}{20}}} = \frac{D_{CLK}}{2}$$

TABLE 32-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal FRC Accuracy @ 8.00 MHz⁽¹⁾ for PIC32MX575/675/695/775/795 Family Devices						
F20a	FRC	-2	—	+2	%	—
Internal FRC Accuracy @ 8.00 MHz⁽¹⁾ for PIC32MX534/564/664/764 Family Devices						
F20b	FRC	-0.9	—	+0.9	%	—

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

FIGURE 32-5: EXTERNAL RESET TIMING CHARACTERISTICS

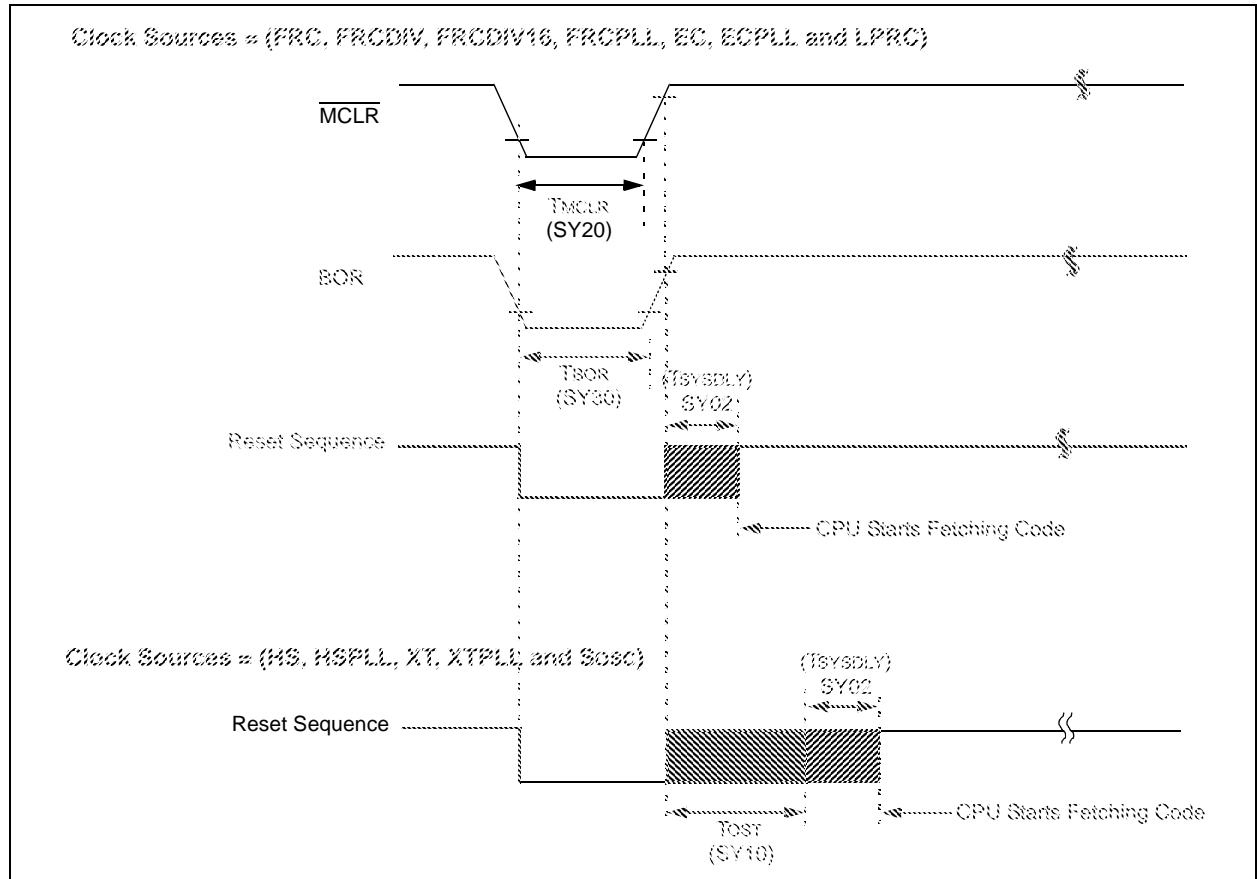


TABLE 32-22: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	-40°C to +85°C
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	—	1 μs + 8 SYSCLK cycles	—	—	-40°C to +85°C
SY20	TMCLR	MCLR Pulse Width (low)	—	2	—	μs	-40°C to +85°C
SY30	TBOR	BOR Pulse Width (low)	—	1	—	μs	-40°C to +85°C

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

TABLE 32-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Max.	Units	Conditions	
TB10	T _{TXH}	TxCK High Time	Synchronous, with prescaler	$[(12.5\text{ ns or }1\text{ TPB})/N]$ + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	T _{TXL}	TxCK Low Time	Synchronous, with prescaler	$[(12.5\text{ ns or }1\text{ TPB})/N]$ + 25 ns	—	ns	Must also meet parameter TB15	
TB15	T _{TXP}	TxCK Input Period	Synchronous, with prescaler	$[(\text{Greater of } [(25\text{ ns or }2\text{ TPB})/N] + 30\text{ ns})]$	—	ns	V _{DD} > 2.7V	
				$[(\text{Greater of } [(25\text{ ns or }2\text{ TPB})/N] + 50\text{ ns})]$	—	ns	V _{DD} < 2.7V	
TB20	T _{CKEXTMRL}	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPB	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

33.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 33-1: V_{OH} – 4x DRIVER PINS

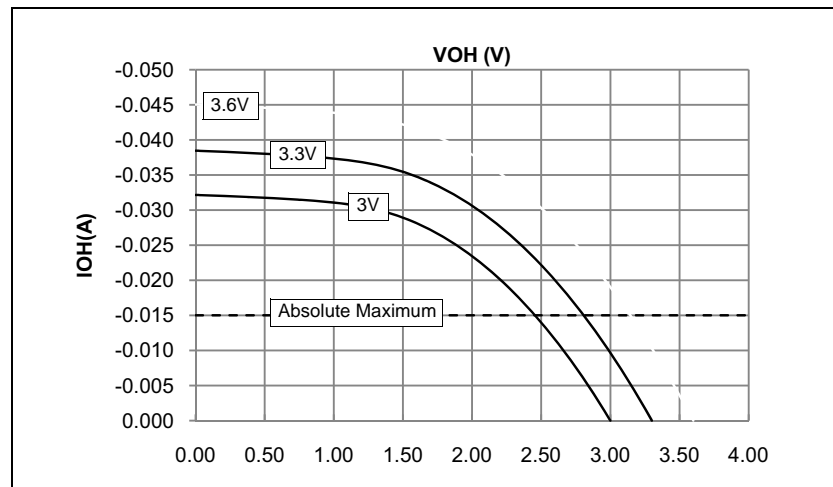


FIGURE 33-3: V_{OL} – 4x DRIVER PINS

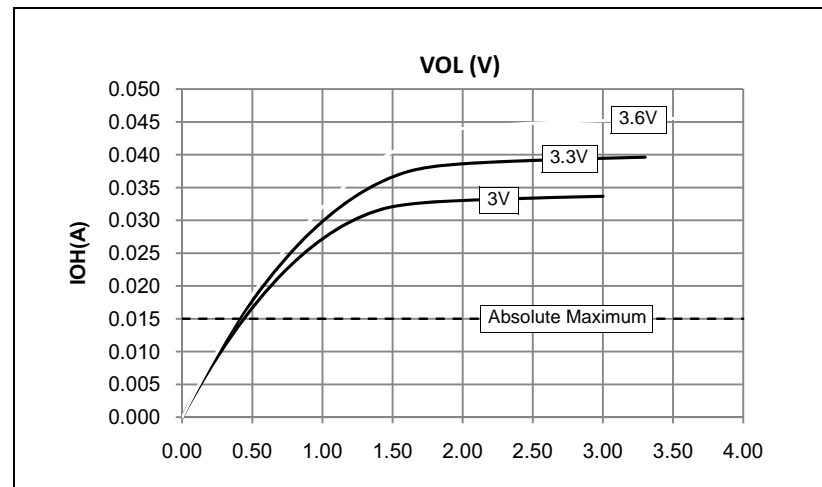


FIGURE 33-2: V_{OH} – 8x DRIVER PINS

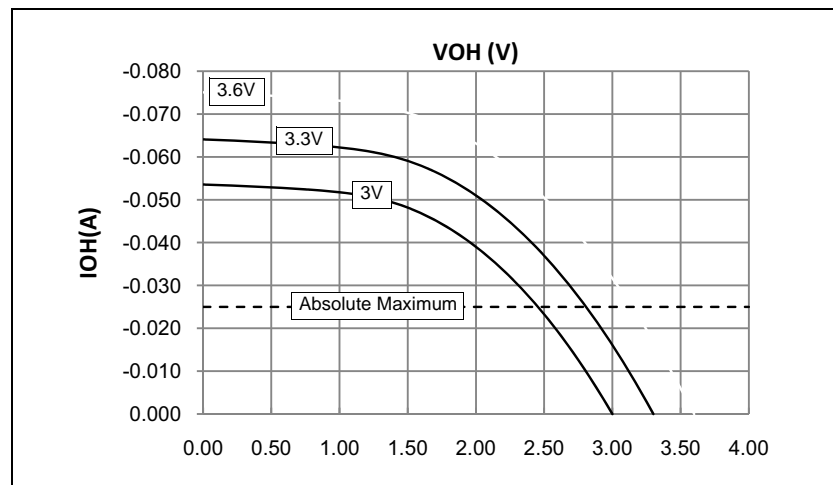
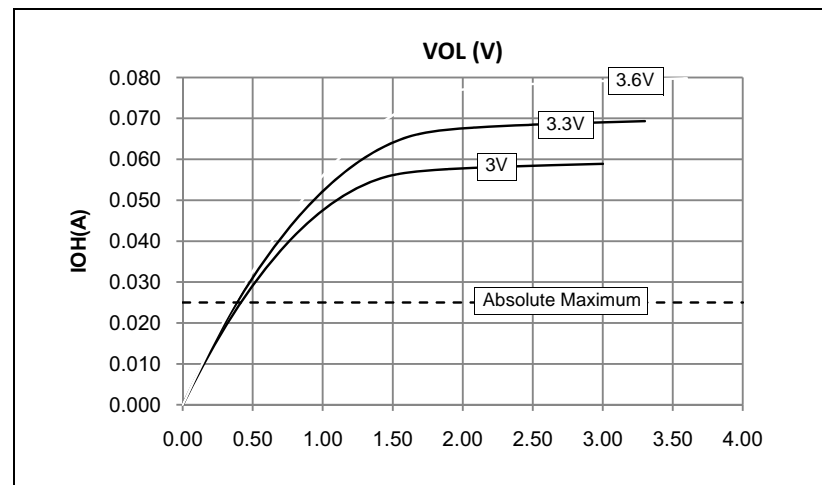


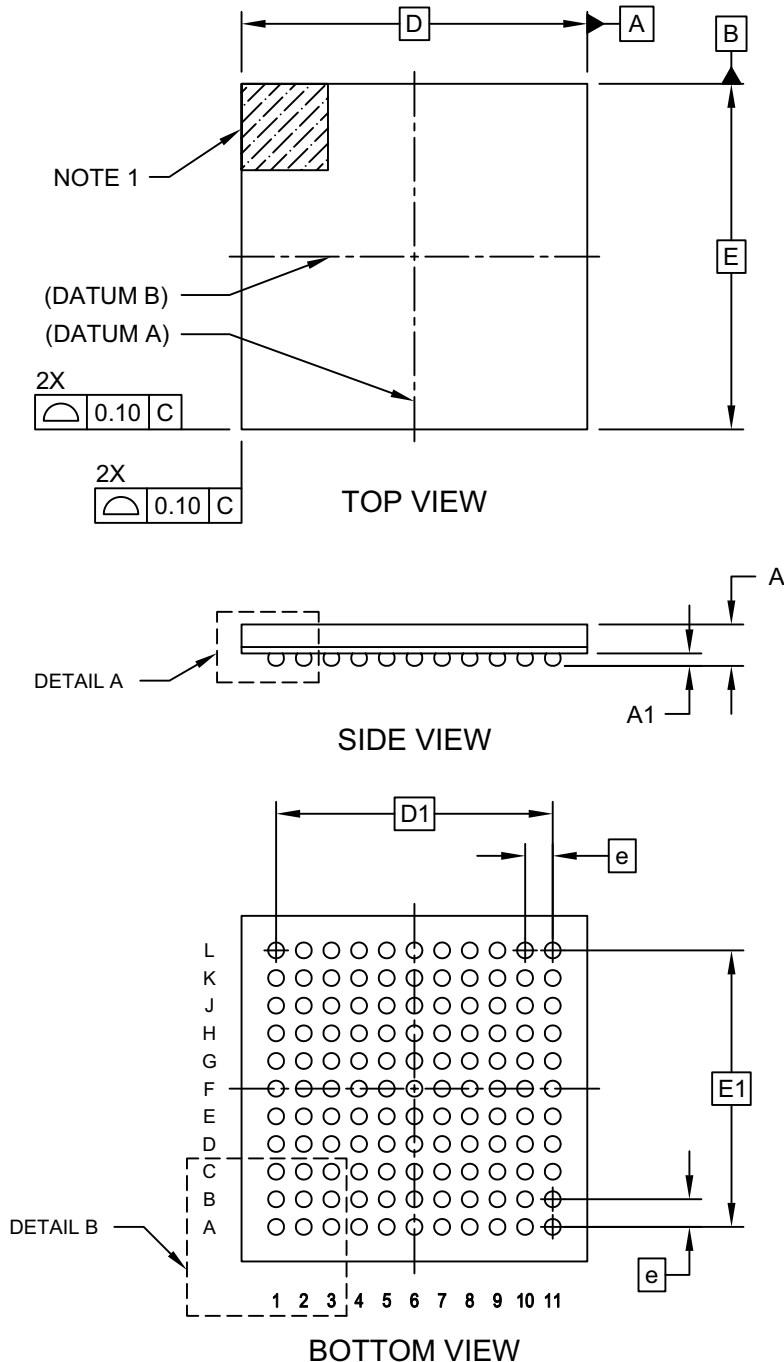
FIGURE 33-4: V_{OL} – 8x DRIVER PINS



PIC32MX5XX/6XX/7XX

121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

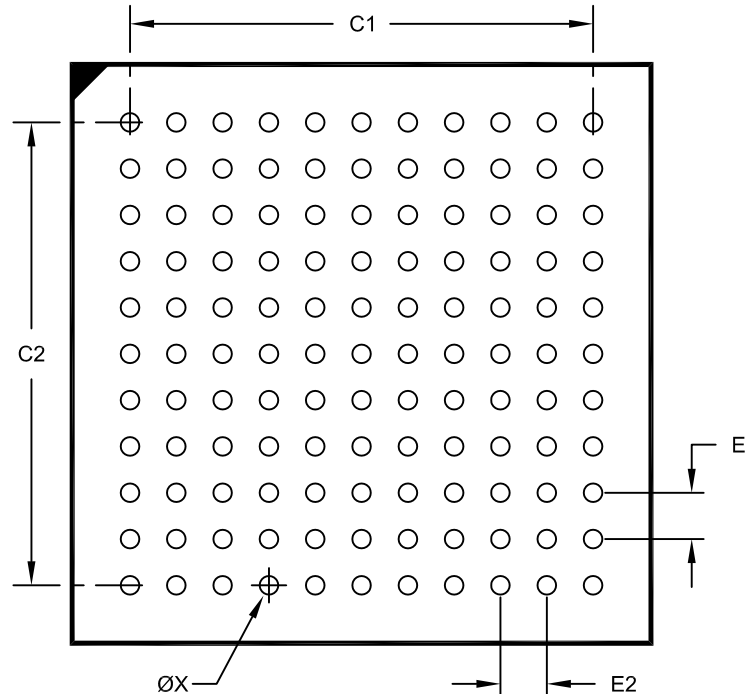


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121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E1	0.80 BSC		
Contact Pitch	E2	0.80 BSC		
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

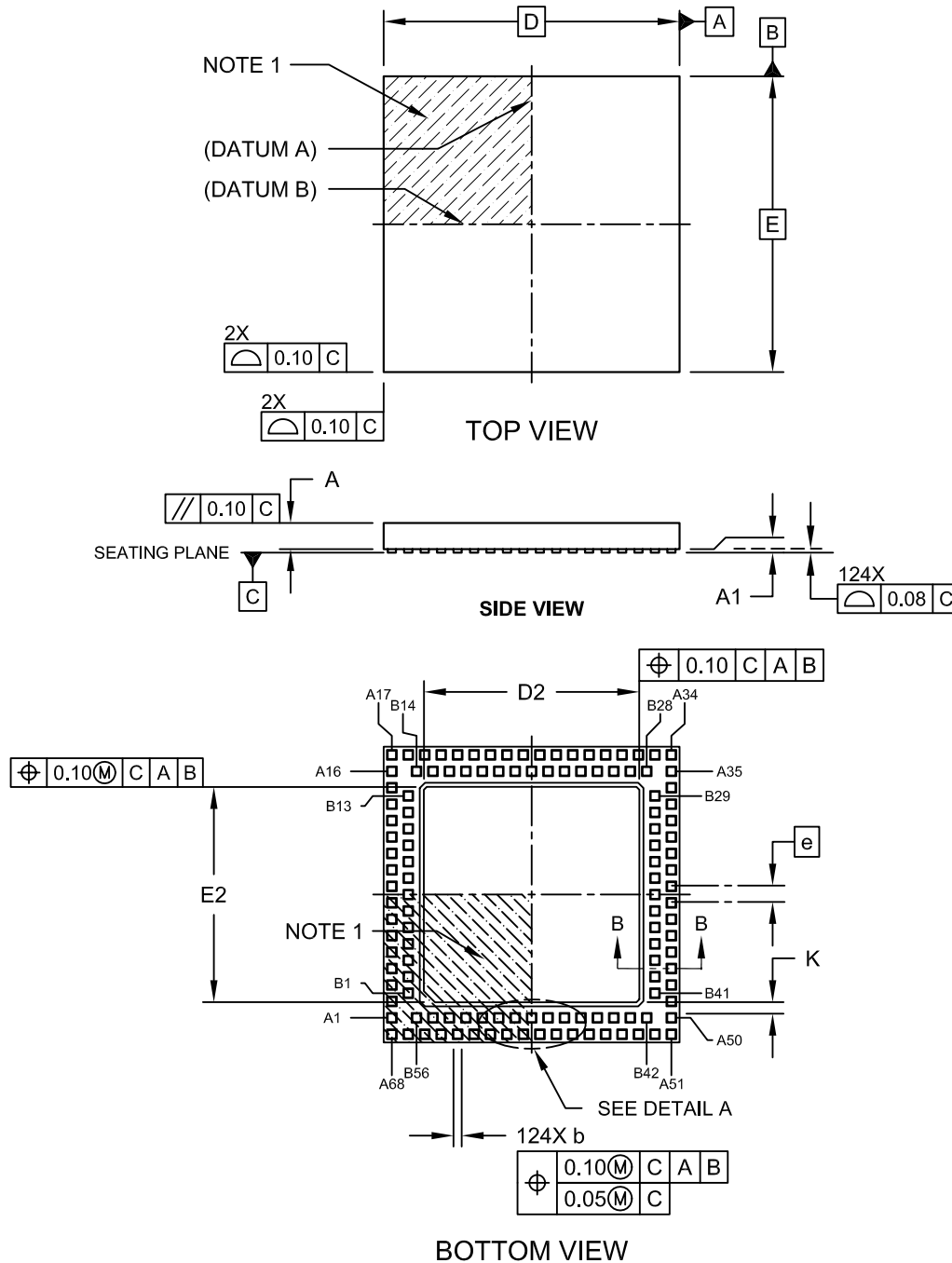
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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PIC32MX5XX/6XX/7XX

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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TABLE B-4: SECTION UPDATES (CONTINUED)

Section Name	Update Description
7.0 “Interrupt Controller”	<ul style="list-style-type: none"> Updated the following Interrupt Sources in Table 7-1: <ul style="list-style-type: none"> Changed IC2AM – I2C4 Master Event to: IC4M – I2C4 Master Event Changed IC3AM – I2C5 Master Event to: IC5M – I2C4 Master Event Changed U1E – UART1A Error to: U1E – UART1 Error Changed U4E – UART1B Error to: U4E – UART4 Error Changed U1RX – UART1A Receiver to: U1RX – UART1 Receiver Changed U4RX – UART1B Receiver to: U4RX – UART4 Receiver Changed U1TX – UART1A Transmitter to: U1TX – UART1 Transmitter Changed U4TX – UART1B Transmitter to: U4TX – UART4 Transmitter Changed U6E – UART2B Error to: U6E – UART6 Error Changed U6RX – UART2B Receiver to: U6RX – UART6 Receiver Changed U6TX – UART2B Transmitter to: U6TX – UART6 Transmitter Changed U5E – UART3B Error to: U5E – UART5 Error Changed U5RX – UART3B Receiver to: U5RX – UART5 Receiver Changed U5TX – UART3B Transmitter to: U5TX – UART5 Transmitter
1.0 “Oscillator Configuration”	Updated Figure 1-1
1.0 “Output Compare”	Updated Figure 1-1
1.0 “Ethernet Controller”	Added a note on using the Ethernet controller pins (see note above Table 1-3)
1.0 “Comparator Voltage Reference (CVREF)”	Updated the note in Figure 1-1
1.0 “Special Features”	Updated the bit description for bit 10 in Register 1-2 Added notes 1 and 2 to Register 1-4
1.0 “Electrical Characteristics”	Updated the Absolute Maximum Ratings: <ul style="list-style-type: none"> Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V - 0.3V to +3.6V was updated Voltage on VBUS with respect to VSS - 0.3V to +5.5V was added Updated the maximum value of DC16 as 2.1 in Table 1-4 Updated the Typical values for the following parameters: DC20b, DC20c, DC21c, DC22c and DC23c (see Table 1-5) Updated Table 1-11: <ul style="list-style-type: none"> Removed the following DC Characteristics: Programming temperature $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ (25°C recommended) Updated the Minimum value for the Parameter number D131 as 2.3 Removed the Conditions for the following Parameter numbers: D130, D131, D132, D135, D136 and D137 Updated the condition for the parameter number D130a and D132a Updated the Minimum, Typical and Maximum values for parameter D305 in Table 1-13 Added note 2 to Table 1-18 Updated the Minimum and Maximum values for parameter F20b (see Table 1-19) Updated the following figures: <ul style="list-style-type: none"> Figure 1-4 Figure 1-9 Figure 1-22 Figure 1-23
Appendix A: “Migrating from PIC32MX3XX/4XX to PIC32MX5XX/6XX/7XX Devices”	Removed the A.3 Pin Assignments sub-section.

PIC32MX5XX/6XX/7XX

TABLE B-7: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
32.0 “Electrical Characteristics”	Note 4 in the Operating Current specification was updated (see Table 32-5). Note 3 in the Idle Current specification was updated (see Table 32-6). Note 6 references in the Power-Down Current specification were updated (see Table 32-7). The Program Memory parameters, D135, D136, and D137, and Note 4 were updated (see Table 32-11). The Voltage Reference Specifications were updated (see Table 32-14). Parameter DO50 (Cosco) was added to the Capacitive Loading Requirements on Output Pins (see Table 32-16). The EJTAG Timing Characteristics were updated (see Figure 32-28). The maximum value for parameters ET13 and ET14 were updated in the Ethernet Module Specifications (see Table 32-35). Parameter PM7 (TDHOLD) was updated (see Table 32-40).
34.0 “Packaging Information”	Packaging diagrams were updated.
Product Identification System	The Speed and Program Memory Size were updated and Note 1 was added.