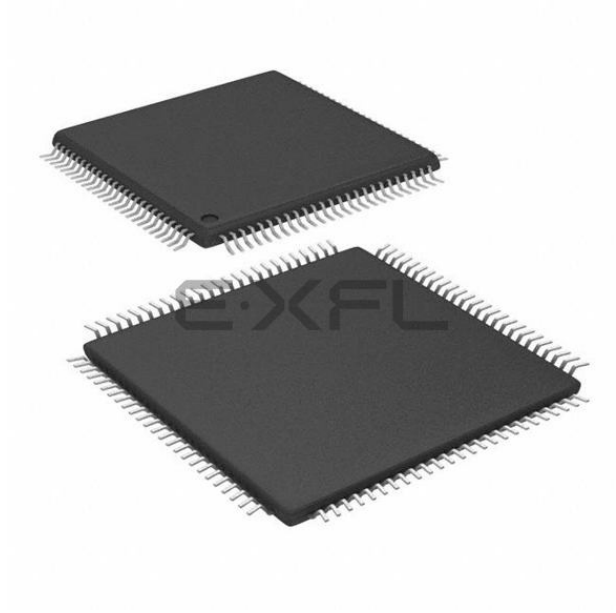
# Microchip Technology - PIC32MX775F512L-80I/PT Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx775f512l-80i-pt |

## Device Pin Tables

### TABLE 4: PIN NAMES FOR 64-PIN USB AND CAN DEVICES

**64-PIN QFN(2) AND TQFP (TOP VIEW)**

**PIC32MX534F064H**
**PIC32MX564F064H**
**PIC32MX564F128H**
**PIC32MX575F256H**
**PIC32MX575F512H**

64 1

**QFN(2)**

64 1

**TQFP**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | PMD5/RE5 | 33 | USBID/RF3 |
| 2 | PMD6/RE6 | 34 | VBUS |
| 3 | PMD7/RE7 | 35 | VUSB3V3 |
| 4 | SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | 36 | D-/RG3 |
| 5 | SDA4/SDI2/U3RX/PMA4/CN9/RG7 | 37 | D+/RG2 |
| 6 | SCL4/SDO2/U3TX/PMA3/CN10/RG8 | 38 | VDD |
| 7 | MCLR | 39 | OSC1/CLKI/RC12 |
| 8 | SS2/U6RX/U3CTS/PMA2/CN11/RG9 | 40 | OSC2/CLKO/RC15 |
| 9 | VSS | 41 | VSS |
| 10 | VDD | 42 | RTCC/IC1/INT1/RD8 |
| 11 | AN5/C1IN+/VBUSON/CN7/RB5 | 43 | SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 |
| 12 | AN4/C1IN-/CN6/RB4 | 44 | SCL1/IC3/PMCS2/PMA15/INT3/RD10 |
| 13 | AN3/C2IN+/CN5/RB3 | 45 | IC4/PMCS1/PMA14/INT4/RD11 |
| 14 | AN2/C2IN-/CN4/RB2 | 46 | OC1/INT0/RD0 |
| 15 | PGEC1/AN1/VREF-/CVREF-/CN3/RB1 | 47 | SOSCI/CN1/RC13 |
| 16 | PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0 | 48 | SOSCO/T1CK/CN0/RC14 |
| 17 | PGEC2/AN6/OCFA/RB6 | 49 | SCK3/U4TX/U1RTS/OC2/RD1 |
| 18 | PGED2/AN7/RB7 | 50 | SDA3/SDI3/U1RX/OC3/RD2 |
| 19 | AVDD | 51 | SCL3/SDO3/U1TX/OC4/RD3 |
| 20 | AVSS | 52 | OC5/IC5/PMWR/CN13/RD4 |
| 21 | AN8/SS4/U5RX/U2CTS/C1OUT/RB8 | 53 | PMRD/CN14/RD5 |
| 22 | AN9/C2OUT/PMA7/RB9 | 54 | CN15/RD6 |
| 23 | TMS/AN10/CVREFOUT/PMA13/RB10 | 55 | CN16/RD7 |
| 24 | TDO/AN11/PMA12/RB11 | 56 | VCAP |
| 25 | VSS | 57 | VDD |
| 26 | VDD | 58 | C1RX/RF0 |
| 27 | TCK/AN12/PMA11/RB12 | 59 | C1TX/RF1 |
| 28 | TDI/AN13/PMA10/RB13 | 60 | PMD0/RE0 |
| 29 | AN14/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14 | 61 | PMD1/RE1 |
| 30 | AN15/OCFB/PMALL/PMA0/CN12/RB15 | 62 | PMD2/RE2 |
| 31 | AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4 | 63 | PMD3/RE3 |
| 32 | AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5 | 64 | PMD4/RE4 |

**Note 1:** Shaded pins are 5V tolerant.
**2:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**TABLE 12: PIN NAMES FOR USB, ETHERNET, AND CAN DEVICES**

**121-PIN TFBGA (BOTTOM VIEW)** L11

L1 A11

**PIC32MX764F128L**
**PIC32MX775F256L**
**PIC32MX775F512L**
**PIC32MX795F512L**

**Note:** The TFBGA package skips from row "H" to row "J" and has no "I" row. A1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| A1 | PMD4/RE4 | E2 | T4CK/AC2RX(1)/RC3 |
| A2 | PMD3/RE3 | E3 | ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6 |
| A3 | TRD0/RG13 | E4 | T3CK/AC2TX(1)/RC2 |
| A4 | PMD0/RE0 | E5 | VDD |
| A5 | C2RX(1)/PMD8/RG0 | E6 | C2TX(1)/ETXERR/PMD9/RG1 |
| A6 | C1TX/ETXD0/PMD10/RF1 | E7 | VSS |
| A7 | VDD | E8 | AETXEN/SDA1/INT4/RA15 |
| A8 | VSS | E9 | RTCC/EMDIO/AEMDIO/IC1/RD8 |
| A9 | ETXD2/IC5/PMD12/RD12 | E10 | SS1/IC2/RD9 |
| A10 | OC3/RD2 | E11 | AETXCLK/SCL1/INT3/RA14 |
| A11 | OC2/RD1 | F1 | MCLR |
| B1 | No Connect (NC) | F2 | ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8 |
| B2 | AERXERR/RG15 | F3 | ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9 |
| B3 | PMD2/RE2 | F4 | ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7 |
| B4 | PMD1/RE1 | F5 | VSS |
| B5 | TRD3/RA7 | F6 | No Connect (NC) |
| B6 | C1RX/ETXD1/PMD11/RF0 | F7 | No Connect (NC) |
| B7 | VCAP | F8 | VDD |
| B8 | PMRD/CN14/RD5 | F9 | OSC1/CLKI/RC12 |
| B9 | OC4/RD3 | F10 | VSS |
| B10 | VSS | F11 | OSC2/CLKO/RC15 |
| B11 | SOSCO/T1CK/CN0/RC14 | G1 | AERXD0/INT1/RE8 |
| C1 | PMD6/RE6 | G2 | AERXD1/INT2/RE9 |
| C2 | VDD | G3 | TMS/RA0 |
| C3 | TRD1/RG12 | G4 | No Connect (NC) |
| C4 | TRD2/RG14 | G5 | VDD |
| C5 | TRCLK/RA6 | G6 | VSS |
| C6 | No Connect (NC) | G7 | VSS |
| C7 | ETXCLK/PMD15/CN16/RD7 | G8 | No Connect (NC) |
| C8 | OC5/PMWR/CN13/RD4 | G9 | TDO/RA5 |
| C9 | VDD | G10 | SDA2/RA3 |
| C10 | SOSCI/CN1/RC13 | G11 | TDI/RA4 |
| C11 | EMDC/AEMDC/IC4/PMCS1/PMA14/RD11 | H1 | AN5/C1IN+/VBUSON/CN7/RB5 |
| D1 | T2CK/RC1 | H2 | AN4/C1IN-/CN6/RB4 |
| D2 | PMD7/RE7 | H3 | VSS |
| D3 | PMD5/RE5 | H4 | VDD |
| D4 | VSS | H5 | No Connect (NC) |
| D5 | VSS | H6 | VDD |
| D6 | No Connect (NC) | H7 | No Connect (NC) |
| D7 | ETXEN/PMD14/CN15/RD6 | H8 | VBUS |
| D8 | ETXD3/PMD13/CN19/RD13 | H9 | VUSB3V3 |
| D9 | SDO1/OC1/INT0/RD0 | H10 | D+/RG2 |
| D10 | No Connect (NC) | H11 | SCL2/RA2 |
| D11 | SCK1/IC3/PMCS2/PMA15/RD10 | J1 | AN3/C2IN+/CN5/RB3 |
| E1 | T5CK/SDI1/RC4 | J2 | AN2/C2IN-/CN4/RB2 |

**Note 1:** This pin is not available on PIC32MX764F128L devices.
**2:** Shaded pins are 5V tolerant.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| RG0 | — | 90 | A5 | A61 | I/O | ST | PORTG is a bidirectional I/O port |
| RG1 | — | 89 | E6 | B50 | I/O | ST | |
| RG6 | 4 | 10 | E3 | A7 | I/O | ST | |
| RG7 | 5 | 11 | F4 | B6 | I/O | ST | |
| RG8 | 6 | 12 | F2 | A8 | I/O | ST | |
| RG9 | 8 | 14 | F3 | A9 | I/O | ST | |
| RG12 | — | 96 | C3 | A65 | I/O | ST | |
| RG13 | — | 97 | A3 | B55 | I/O | ST | |
| RG14 | — | 95 | C4 | B54 | I/O | ST | |
| RG15 | — | 1 | B2 | A2 | I/O | ST | |
| RG2 | 37 | 57 | H10 | B31 | I | ST | PORTG input pins |
| RG3 | 36 | 56 | J11 | A38 | I | ST | |
| T1CK | 48 | 74 | B11 | B40 | I | ST | Timer1 external clock input |
| T2CK | — | 6 | D1 | A5 | I | ST | Timer2 external clock input |
| T3CK | — | 7 | E4 | B4 | I | ST | Timer3 external clock input |
| T4CK | — | 8 | E2 | A6 | I | ST | Timer4 external clock input |
| T5CK | — | 9 | E1 | B5 | I | ST | Timer5 external clock input |
| $\overline{U1CTS}$ | 43 | 47 | L9 | B26 | I | ST | UART1 clear to send |
| $\overline{U1RTS}$ | 49 | 48 | K9 | A31 | O | — | UART1 ready to send |
| U1RX | 50 | 52 | K11 | A36 | I | ST | UART1 receive |
| U1TX | 51 | 53 | J10 | B29 | O | — | UART1 transmit |
| $\overline{U3CTS}$ | 8 | 14 | F3 | A9 | I | ST | UART3 clear to send |
| $\overline{U3RTS}$ | 4 | 10 | E3 | A7 | O | — | UART3 ready to send |
| U3RX | 5 | 11 | F4 | B6 | I | ST | UART3 receive |
| U3TX | 6 | 12 | F2 | A8 | O | — | UART3 transmit |
| $\overline{U2CTS}$ | 21 | 40 | K6 | A27 | I | ST | UART2 clear to send |
| $\overline{U2RTS}$ | 29 | 39 | L6 | B22 | O | — | UART2 ready to send |
| U2RX | 31 | 49 | L10 | B27 | I | ST | UART2 receive |
| U2TX | 32 | 50 | L11 | A32 | O | — | UART2 transmit |
| U4RX | 43 | 47 | L9 | B26 | I | ST | UART4 receive |
| U4TX | 49 | 48 | K9 | A31 | O | — | UART4 transmit |
| U6RX | 8 | 14 | F3 | A9 | I | ST | UART6 receive |
| U6TX | 4 | 10 | E3 | A7 | O | — | UART6 transmit |
| U5RX | 21 | 40 | K6 | A27 | I | ST | UART5 receive |
| U5TX | 29 | 39 | L6 | B22 | O | — | UART5 transmit |
| SCK1 | — | 70 | D11 | B38 | I/O | ST | Synchronous serial clock input/output for SPI1 |

**Legend:** CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer
Analog = Analog input
O = Output
P = Power
I = Input

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.

## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX5XX/6XX/7XX microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX5XX/6XX/7XX devices to execute from data memory.

Key features include:

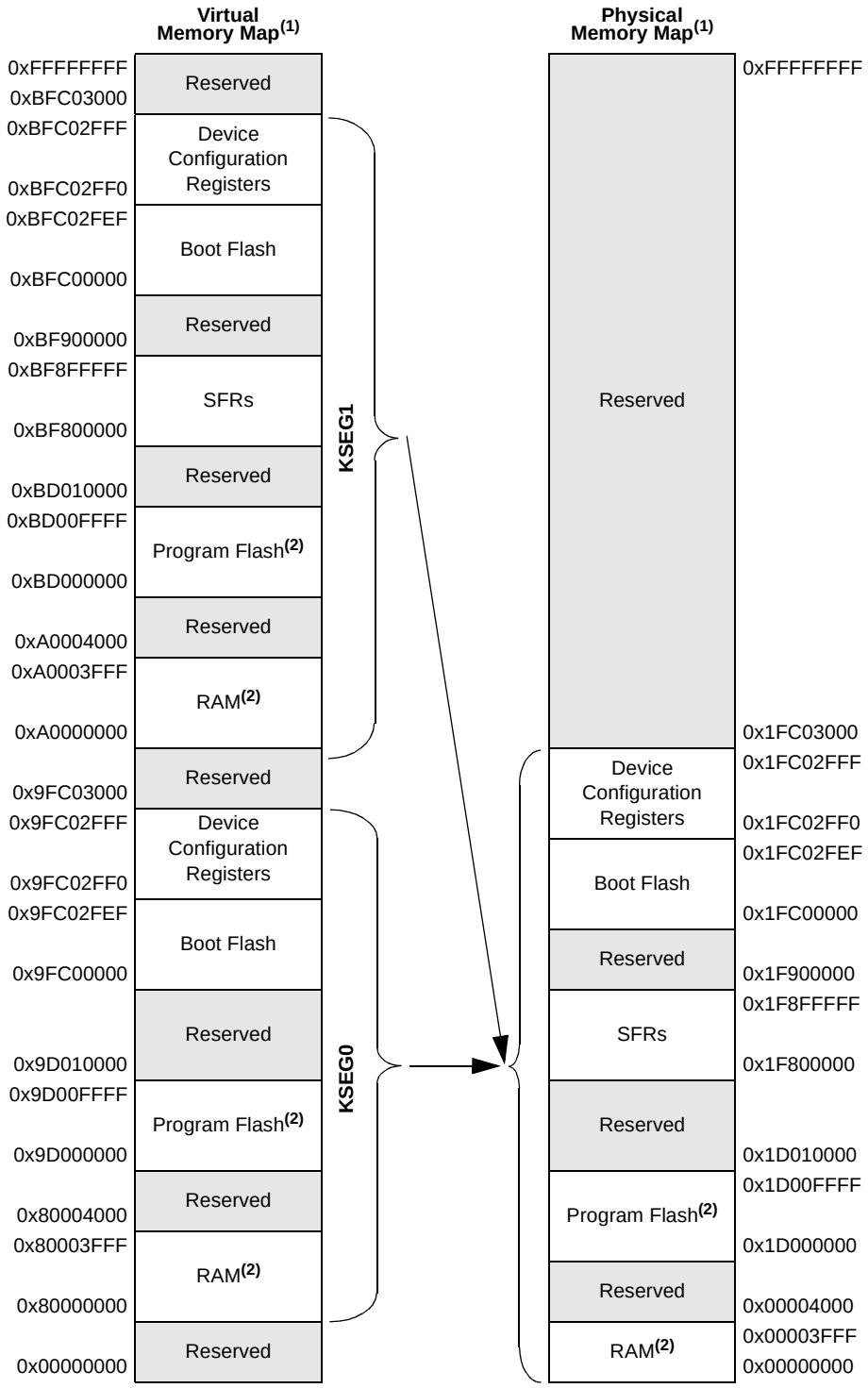
- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/ KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

### 4.1 Memory Layout

PIC32MX5XX/6XX/7XX microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX5XX/6XX/7XX devices are illustrated in Figure 4-1 through Figure 4-6. Table 4-1 provides memory map information for the Special Function Registers (SFRs).

**FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX534F064H AND PIC32MX534F064L DEVICES**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

**TABLE 11-1: USB REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 53A0 | U1EP10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53B0 | U1EP11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53C0 | U1EP12 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53D0 | U1EP13 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53E0 | U1EP14 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53F0 | U1EP15 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register does not have associated SET and INV registers.

**3:** This register does not have associated CLR, SET and INV registers.

**4:** Reset value for this bit is undefined.

**REGISTER 11-16: U1SOF: USB SOF THRESHOLD REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CNT<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:
01001010 = 64-byte packet
00101010 = 32-byte packet
00011010 = 16-byte packet
00010010 = 8-byte packet

**REGISTER 11-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| | BDTPTRL<15:9> | | | | | | | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'

**REGISTER 19-2: I2CxSTAT: $I^2C$ STATUS REGISTER (CONTINUED)**

bit 5 **D_A:** Data/Address bit (when operating as $I^2C$ slave)
This bit is cleared by hardware upon a device address match, and is set by hardware by reception of the slave byte.
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address

bit 4 **P:** Stop bit
This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected.
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

bit 3 **S:** Start bit
This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected.
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last

bit 2 **R_W:** Read/Write Information bit (when operating as $I^2C$ slave)
This bit is set or cleared by hardware after reception of an $I^2C$ device address byte.
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave

bit 1 **RBF:** Receive Buffer Full Status bit
This bit is set by hardware when the I2CxRCV register is written with a received byte, and is cleared by hardware when software reads I2CxRCV.
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty

bit 0 **TBF:** Transmit Buffer Full Status bit
This bit is set by hardware when software writes to the I2CxTRN register, and is cleared by hardware upon completion of data transmission.
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty

**REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | S/HC-0 | R/W-1 | R/W-0 | R/W-0 |
| | — | — | — | — | ABAT | REQOP<2:0> | | |
| 23:16 | R-1 | R-0 | R-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | OPMOD<2:0> | | | CANCAP | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | R-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDLE | — | CANBUSY | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | DNCNT<4:0> | | | | |

| Legend: | HC = Hardware Clear | S = Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as '0'

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as '0'

**Note 1:** If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

**REGISTER 24-9: CiRXMn: CAN ACCEPTANCE FILTER MASK 'n' REGISTER (n = 0, 1, 2 OR 3)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SID<10:3> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | SID<2:0> | | | — | MIDE | — | EID<17:16> | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EID<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EID<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Include the SIDx bit in filter comparison
0 = The SIDx bit is a 'don't care' in filter operation

bit 20 **Unimplemented:** Read as '0'

bit 19 **MIDE:** Identifier Receive Mode bit
1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Include the EIDx bit in filter comparison
0 = The EIDx bit is a 'don't care' in filter operation

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

**REGISTER 25-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | TXBUSE | RXBUSE | — | — | — | EWMARK | FWMARK |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXDONE | PKTPEND | RXACT | — | TXDONE | TXABORT | RXBUFNA | RXOVFLW |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSE:** Transmit BVCI Bus Error Interrupt bit

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the TX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 13 **RXBUSE:** Receive BVCI Bus Error Interrupt bit

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the RX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARK:** Empty Watermark Interrupt bit

1 = Empty Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a '0' or a '1' has no effect.

bit 8 **FWMARK:** Full Watermark Interrupt bit

1 = Full Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 7 **RXDONE:** Receive Done Interrupt bit

1 = RX packet was successfully received
0 = No interrupt pending

This bit is set whenever an RX packet is successfully received. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

**Note:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

**REGISTER 25-36: EMAC1MIND: ETHERNET CONTROLLER MAC MII MANAGEMENT INDICATORS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | LINKFAIL | NOTVALID | SCAN | MIIMBUSY |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **LINKFAIL:** Link Fail bit

When '1' is returned - indicates link fail has occurred. This bit reflects the value last read from the PHY status register.

bit 2 **NOTVALID:** MII Management Read Data Not Valid bit

When '1' is returned - indicates an MII management read cycle has not completed and the Read Data is not yet valid.

bit 1 **SCAN:** MII Management Scanning bit

When '1' is returned - indicates a scan operation (continuous MII Management Read cycles) is in progress.

bit 0 **MIIMBUSY:** MII Management Busy bit

When '1' is returned - indicates MII Management module is currently performing an MII Management Read or Write cycle.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**REGISTER 25-38: EMAC1SA1: ETHERNET CONTROLLER MAC STATION ADDRESS 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR4<7:0> | | | | | | | |
| 7:0 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR3<7:0> | | | | | | | |

| **Legend:** | | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR4<7:0>:** Station Address Octet 4 bits
These bits hold the fourth transmitted octet of the station address.

bit 7-0 **STNADDR3<7:0>:** Station Address Octet 3 bits
These bits hold the third transmitted octet of the station address.

**Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**2:** This register is loaded at reset from the factory preprogrammed station address.

**TABLE 32-18: PLL CLOCK TIMING SPECIFICATIONS ($V_{DD}$ = 2.3V TO 3.6V)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 3.92 | — | 5 | MHz | ECPLL, HSPLL, XTPLL, FRCPLL modes |
| OS51 | FSYS | On-Chip VCO System Frequency | 60 | — | 120 | MHz | — |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | — | — | 2 | ms | — |
| OS53 | DCLK | CLKO Stability(2) (Period Jitter or Cumulative) | -0.25 | — | +0.25 | % | Measured over 100 ms period |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 80 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

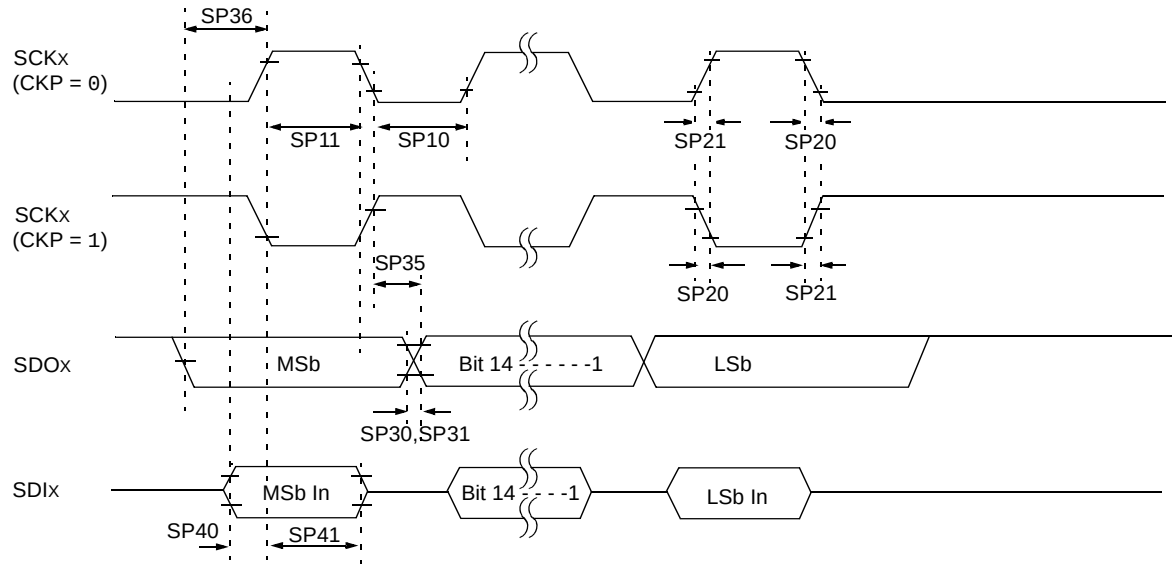
$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{80}{20}}} = \frac{D_{CLK}}{2}$$

**TABLE 32-19: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Internal FRC Accuracy @ 8.00 MHz(1) for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| F20a | FRC | -2 | — | +2 | % | — |
| **Internal FRC Accuracy @ 8.00 MHz(1) for PIC32MX534/564/664/764 Family Devices** | | | | | | |
| F20b | FRC | -0.9 | — | +0.9 | % | — |

**Note 1:** Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

**FIGURE 32-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time(3) | Tsck/2 | — | — | ns | — |
| SP11 | TscH | SCKx Output High Time(3) | Tsck/2 | — | — | ns | — |
| SP20 | TscF | SCKx Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 15 | — | — | ns | — |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 32-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | μs | PBCLK must operate at a minimum of 800 kHz |
| | | | 400 kHz mode | 1.3 | — | μs | PBCLK must operate at a minimum of 3.2 MHz |
| | | | 1 MHz mode(1) | 0.5 | — | μs | — |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | μs | PBCLK must operate at a minimum of 800 kHz |
| | | | 400 kHz mode | 0.6 | — | μs | PBCLK must operate at a minimum of 3.2 MHz |
| | | | 1 MHz mode(1) | 0.5 | — | μs | — |
| IS20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 100 | ns | |
| IS21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 300 | ns | |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | — |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(1) | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | — |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| | | | 1 MHz mode(1) | 0 | 0.3 | μs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4700 | — | ns | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 250 | — | ns | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4000 | — | ns | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 250 | — | ns | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 600 | — | ns | |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 250 | | ns | |
| IS40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | 0 | 3500 | ns | — |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode(1) | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | μs | The amount of time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | μs | |
| | | | 1 MHz mode(1) | 0.5 | — | μs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | — |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (only for 1 MHz mode).

### Revision E (July 2010)

Minor corrections were incorporated throughout the document.

### Revision F (December 2010)

The revision includes the following global update:

VCAP/VDDCORE has been changed to: VCAP/VCORE

Other major changes are referenced by their respective chapter/section in Table B-4:

**TABLE B-4: SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers** | Removed the following Analog Feature: FV tolerant input pins (digital pins only)<br>Updated the term LIN 1.2 support as LIN support for the peripheral feature: Six UART modules with: RS-232, RS-485, and LIN support |
| **1.0 "Device Overview"** | Updated the value of 64-pin QFN/TQFP pin number for the following pin names: PMA0, PMA1 and ECRSDV |
| **4.0 "Memory Organization"** | The following register map tables were updated:<br>• Table 4-2:<br>- Changed bits 24/8 to I2C5BIF in IFS1<br>- Changed bits 24/8-24/10 to SRIPL<2:0> in INTSTAT<br>- Changed bits 25/9/-24/8 to U5IS<1:0> in IPC12<br>- Added note 2<br>• Table 4-3 through Table 4-7:<br>- Changed bits 24/8-24/10 to SRIPL<2:0> in INTSTAT<br>- Changed bits 25/9-24/8 to U5IS<1:0> in IPC12<br>• Table 4-3:<br>- Changed bits 24/8 to I2C5BIF in IFS1<br>- Added note 2<br>• Table 4-4:<br>- Changed bits 24/8 to I2C5BIF in IFS1<br>- Changed bits 24/8 to I2C5BIE in IEC1<br>- Added note 2 references<br>• Table 4-5:<br>- Changed bits 24/8 to I2C5BIF in IFS1<br>- Changed bits 24/8 to I2C5BIE in IEC1<br>- Added note 2 references<br>• Table 4-6:<br>- Changed bit 24/8 to I2C5BIF in IFS1<br>- Updated the bit value of bit 24/8 as I2C5BIE for the IEC1 register.<br>- Added note 2<br>• Table 4-7:<br>- Changed bit 25/9 to I2C5SIF in IFS1<br>- Changed bit 24/8 as I2C5BIF in IFS1<br>- Changed bit 25/9 as I2C5SIE in IEC1<br>- Changed bit 24/8 as I2C5BIE in IEC1<br>- Added note 2 references<br>• Added note 2 to Table 4-8<br>• Updated the All Resets values for the following registers in Table 4-11: I2C3CON, I2C4CON, I2C5CON and I2C1CON.<br>• Updated the All Resets values for the I2C2CON register in Table 4-12 |

## Revision J (September 2016)

This revision includes typographical and formatting updates throughout the data sheet text. In addition, all SFR Register maps were moved from the Memory chapter to their respective peripheral chapters.

All other major updates are referenced by their respective section in Table B-7.

**TABLE B-7: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet"** | Updated Communication Interfaces for LIN support to 2.1.<br>Updated Qualification and Class B Support to AEC-Q100 REVH. |
| **2.0 "Guidelines for Getting Started with 32-bit MCUs"** | The Recommended Minimum Connection diagram was updated (see Figure 2-1).<br>The Example of $\overline{\text{MCLR}}$ Pin Connections diagram was updated (see Figure 2-2).<br>**2.11 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations"** was added. |
| **4.0 "Memory Organization"** | The SFR Memory Map was added (see Table 4-1). |
| **7.0 "Interrupt Controller"** | The UART interrupt sources were updated in the Interrupt IRQ, Vector, and Bit location table (see Table 7-1). |
| **8.0 "Oscillator Configuration"** | Updated the bit value definitions for the TUN<5:0> bits in the OCSTUN register (see Register 8-2). |
| **15.0 "Watchdog Timer (WDT)"** | The content in this chapter was relocated from the Special Features chapter to its own chapter. |
| **18.0 "Serial Peripheral Interface (SPI)"** | The register map tables were combined (see Table 18-1). |
| **19.0 "Inter-Integrated Circuit ($I^2C$)"** | The register map tables were combined (see Table 19-1).<br>The PMADDR register was updated (see Register 21-3). |
| **21.0 "Parallel Master Port (PMP)"** | The bit value definitions for the ADRMUX<1:0> and CSF<1:0> bits in the PMCON register were updated (see Register 21-1). |
| **29.0 "Special Features"** | Removed the duplicate bit value definition for '010' in the DEVCFG2 register (see Register 29-3).<br>Note 1 was added to the Programming, Debugging, and Trace Ports block diagram (see Figure 29-2).<br>The DDPCON register was relocated (see Register 29-6).<br>The Device ID, Revision, and Configuration Summary was updated (see Table 29-2). |

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ISBN: 978-1-5224-0958-8