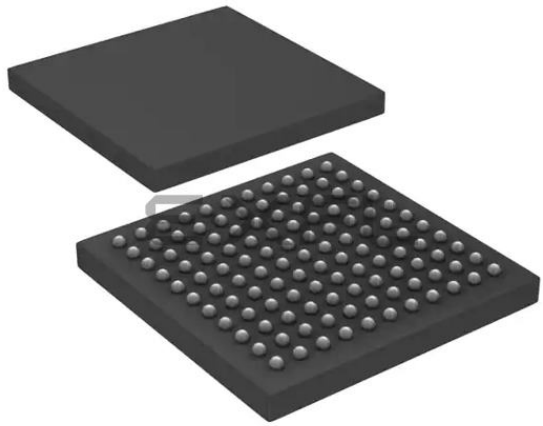
Microchip Technology - PIC32MX795F512L-80I/BG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx795f512l-80i-bg

Device Pin Tables

TABLE 4: PIN NAMES FOR 64-PIN USB AND CAN DEVICES

64-PIN QFN(2) AND TQFP (TOP VIEW)

PIC32MX534F064H
PIC32MX564F064H
PIC32MX564F128H
PIC32MX575F256H
PIC32MX575F512H

64 1

QFN(2)

64 1

TQFP

Pin #	Full Pin Name	Pin #	Full Pin Name
1	PMD5/RE5	33	USBID/RF3
2	PMD6/RE6	34	VBUS
3	PMD7/RE7	35	VUSB3V3
4	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	36	D-/RG3
5	SDA4/SDI2/U3RX/PMA4/CN9/RG7	37	D+/RG2
6	SCL4/SDO2/U3TX/PMA3/CN10/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	SS2/U6RX/U3CTS/PMA2/CN11/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RTCC/IC1/INT1/RD8
11	AN5/C1IN+/VBUSON/CN7/RB5	43	SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9
12	AN4/C1IN-/CN6/RB4	44	SCL1/IC3/PMCS2/PMA15/INT3/RD10
13	AN3/C2IN+/CN5/RB3	45	IC4/PMCS1/PMA14/INT4/RD11
14	AN2/C2IN-/CN4/RB2	46	OC1/INT0/RD0
15	PGEC1/AN1/VREF-/CVREF-/CN3/RB1	47	SOSCI/CN1/RC13
16	PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0	48	SOSCO/T1CK/CN0/RC14
17	PGEC2/AN6/OCFA/RB6	49	SCK3/U4TX/U1RTS/OC2/RD1
18	PGED2/AN7/RB7	50	SDA3/SDI3/U1RX/OC3/RD2
19	AVDD	51	SCL3/SDO3/U1TX/OC4/RD3
20	AVSS	52	OC5/IC5/PMWR/CN13/RD4
21	AN8/SS4/U5RX/U2CTS/C1OUT/RB8	53	PMRD/CN14/RD5
22	AN9/C2OUT/PMA7/RB9	54	CN15/RD6
23	TMS/AN10/CVREFOUT/PMA13/RB10	55	CN16/RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	C1RX/RF0
27	TCK/AN12/PMA11/RB12	59	C1TX/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14	61	PMD1/RE1
30	AN15/OCFB/PMALL/PMA0/CN12/RB15	62	PMD2/RE2
31	AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4	63	PMD3/RE3
32	AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5	64	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.
2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 6: PIN NAMES FOR 64-PIN USB, ETHERNET, AND CAN DEVICES

64-PIN QFN(3) AND TQFP (TOP VIEW)

PIC32MX764F128H
PIC32MX775F256H
PIC32MX775F512H
PIC32MX795F512H

64 1

QFN(3) 64 1 **TQFP**

Pin #	Full Pin Name	Pin #	Full Pin Name
1	ETXEN/PMD5/RE5	33	USBID/RF3
2	ETXD0/PMD6/RE6	34	VBUS
3	ETXD1/PMD7/RE7	35	VUSB3V3
4	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	36	D-/RG3
5	SDA4/SDI2/U3RX/PMA4/CN9/RG7	37	D+/RG2
6	SCL4/SDO2/U3TX/PMA3/CN10/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	SS2/U6RX/U3CTS/PMA2/CN11/RG9	40	OSC2/CLKO/RC15
9	VSS	41	Vss
10	VDD	42	RTCC/AERXD1/ETXD3/IC1/INT1/RD8
11	AN5/C1IN+/VBUSON/CN7/RB5	43	AERXD0/ETXD2/SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9
12	AN4/C1IN-/CN6/RB4	44	ECOL/AECRSDV/SCL1/IC3/PMCS2/PMA15/INT3/RD10
13	AN3/C2IN+/CN5/RB3	45	ECRS/AEREFCLK/IC4/PMCS1/PMA14/INT4/RD11
14	AN2/C2IN-/CN4/RB2	46	OC1/INT0/RD0
15	PGEC1/AN1/VREF-/CVREF-/CN3/RB1	47	SOSCI/CN1/RC13
16	PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0	48	SOSCO/T1CK/CN0/RC14
17	PGEC2/AN6/OCFA/RB6	49	EMDIO/AEMDIO/SCK3/U4TX/U1RTS/OC2/RD1
18	PGED2/AN7/RB7	50	SDA3/SDI3/U1RX/OC3/RD2
19	AVDD	51	SCL3/SDO3/U1TX/OC4/RD3
20	AVSS	52	OC5/IC5/PMWR/CN13/RD4
21	AN8/C2TX(2)/SS4/U5RX/U2CTS/C1OUT/RB8	53	PMRD/CN14/RD5
22	AN9/C2OUT/PMA7/RB9	54	AETXEN/ETXERR/CN15/RD6
23	TMS/AN10/CVREFOUT/PMA13/RB10	55	ETXCLK/AERXERR/CN16/RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	C1RX/AETXD1/ERXD3/RF0
27	TCK/AN12/PMA11/RB12	59	C1TX/AETXD0/ERXD2/RF1
28	TDI/AN13/PMA10/RB13	60	ERXD1/PMD0/RE0
29	AN14/C2RX(2)/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14	61	ERXD0/PMD1/RE1
30	AN15/EMDC/AEMDC/OCFB/PMALL/PMA0/CN12/RB15	62	ERXDV/ECRSDV/PMD2/RE2
31	AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4	63	ERXCLK/EREFCLKPMD3/RE3
32	AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5	64	ERXERR/PMD4/RE4

Note 1: Shaded pins are 5V tolerant.
2: This pin is not available on PIC32MX765F128H devices.
3: The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 7: PIN NAMES FOR 100-PIN USB AND CAN DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MX534F064L
PIC32MX564F064L
PIC32MX564F128L
PIC32MX575F512L
PIC32MX575F256L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RG15	36	VSS
2	VDD	37	VDD
3	PMD5/RE5	38	TCK/RA1
4	PMD6/RE6	39	AC1TX/SCK4/U5TX/U2RTS/RF13
5	PMD7/RE7	40	AC1RX/SS4/U5RX/U2CTS/RF12
6	T2CK/RC1	41	AN12/PMA11/RB12
7	T3CK/RC2	42	AN13/PMA10/RB13
8	T4CK/RC3	43	AN14/PMALH/PMA1/RB14
9	T5CK/SDI1/RC4	44	AN15/OCFB/PMALL/PMA0/CN12/RB15
10	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	45	VSS
11	SDA4/SDI2/U3RX/PMA4/CN9/RG7	46	VDD
12	SCL4/SDO2/U3TX/PMA3/CN10/RG8	47	SS3/U4RX/U1CTS/CN20/RD14
13	MCLR	48	SCK3/U4TX/U1RTS/CN21/RD15
14	SS2/U6RX/U3CTS/PMA2/CN11/RG9	49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
15	VSS	50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
16	VDD	51	USBID/RF3
17	TMS/RA0	52	SDA3/SDI3/U1RX/RF2
18	INT1/RE8	53	SCL3/SDO3/U1TX/RF8
19	INT2/RE9	54	VBUS
20	AN5/C1IN+/VBUSON/CN7/RB5	55	VUSB3V3
21	AN4/C1IN-/CN6/RB4	56	D-/RG3
22	AN3/C2IN+/CN5/RB3	57	D+/RG2
23	AN2/C2IN-/CN4/RB2	58	SCL2/RA2
24	PGEC1/AN1/CN3/RB1	59	SDA2/RA3
25	PGED1/AN0/CN2/RB0	60	TDI/RA4
26	PGEC2/AN6/OCFA/RB6	61	TDO/RA5
27	PGED2/AN7/RB7	62	VDD
28	VREF-/CVREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	SCL1/INT3/RA14
32	AN8/C1OUT/RB8	67	SDA1/INT4/RA15
33	AN9/C2OUT/RB9	68	RTCC/IC1/RD8
34	AN10/CVREFOUT/PMA13/RB10	69	SS1/IC2/RD9
35	AN11/PMA12/RB11	70	SCK1/IC3/PMCS2/PMA15/RD10

Note 1: Shaded pins are 5V tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
SDI1	—	9	E1	B5	I	ST	SPI1 data in
SDO1	—	72	D9	B39	O	—	SPI1 data out
$\overline{SS1}$	—	69	E10	A45	I/O	ST	SPI1 slave synchronization or frame pulse I/O
SCK3	49	48	K9	A31	I/O	ST	Synchronous serial clock input/output for SPI3
SDI3	50	52	K11	A36	I	ST	SPI3 data in
SDO3	51	53	J10	B29	O	—	SPI3 data out
$\overline{SS3}$	43	47	L9	B26	I/O	ST	SPI3 slave synchronization or frame pulse I/O
SCK2	4	10	E3	A7	I/O	ST	Synchronous serial clock input/output for SPI2
SDI2	5	11	F4	B6	I	ST	SPI2 data in
SDO2	6	12	F2	A8	O	—	SPI2 data out
$\overline{SS2}$	8	14	F3	A9	I/O	ST	SPI2 slave synchronization or frame pulse I/O
SCK4	29	39	L6	B22	I/O	ST	Synchronous serial clock input/output for SPI4
SDI4	31	49	L10	B27	I	ST	SPI4 data in
SDO4	32	50	L11	A32	O	—	SPI4 data out
$\overline{SS4}$	21	40	K6	A27	I/O	ST	SPI4 slave synchronization or frame pulse I/O
SCL1	44	66	E11	B36	I/O	ST	Synchronous serial clock input/output for I2C1
SDA1	43	67	E8	A44	I/O	ST	Synchronous serial data input/output for I2C1
SCL3	51	53	J10	B29	I/O	ST	Synchronous serial clock input/output for I2C3
SDA3	50	52	K11	A36	I/O	ST	Synchronous serial data input/output for I2C3
SCL2	—	58	H11	A39	I/O	ST	Synchronous serial clock input/output for I2C2
SDA2	—	59	G10	B32	I/O	ST	Synchronous serial data input/output for I2C2
SCL4	6	12	F2	A8	I/O	ST	Synchronous serial clock input/output for I2C4
SDA4	5	11	F4	B6	I/O	ST	Synchronous serial data input/output for I2C4
SCL5	32	50	L11	A32	I/O	ST	Synchronous serial clock input/output for I2C5
SDA5	31	49	L10	B27	I/O	ST	Synchronous serial data input/output for I2C5

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

2: See **25.0 "Ethernet Controller"** for more information.

NOTES:

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS	R-0, HS	R-0, HSC	U-0	U-0	U-0
	WR	WREN	WRERR(1)	LVDERR(1)	LVDSTAT(1)	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	NVMOP<3:0>			

Legend:	U = Unimplemented bit, read as '0'		HSC = Set and Cleared by hardware
R = Readable bit	W = Writable bit	HS = Set by hardware	HC = Cleared by hardware
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit
This bit is writable when WREN = 1 and the unlock sequence is followed.
1 = Initiate a Flash operation. Hardware clears this bit when the operation completes
0 = Flash operation complete or inactive

bit 14 **WREN:** Write Enable bit
1 = Enable writes to WR bit and enables LVD circuit
0 = Disable writes to WR bit and disables LVD circuit

Note: This is the only bit in this register that is reset by a device Reset.

bit 13 **WRERR:** Write Error bit(1)
This bit is read-only and is automatically set by hardware.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit (LVD circuit must be enabled)(1)
This bit is read-only and is automatically set by hardware.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **LVDSTAT:** Low-Voltage Detect Status bit (LVD circuit must be enabled)(1)
This bit is read-only and is automatically set, and cleared, by hardware.
1 = Low-voltage event is active
0 = Low-voltage event is not active

bit 10-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits
These bits are writable when WREN = 0.
1111 = Reserved
•
•
•
0111 = Reserved
0110 = No operation
0101 = Program Flash (PFM) erase operation: erases PFM if all pages are not write-protected
0100 = Page erase operation: erases page selected by NVMADDR if it is not write-protected
0011 = Row program operation: programs row selected by NVMADDR if it is not write-protected
0010 = No operation
0001 = Word program operation: programs word selected by NVMADDR if it is not write-protected
0000 = No operation

Note 1: This bit is cleared by setting NVMOP == 0000b, and initiating a Flash operation (i.e., WR).

7.1 Control Registers

TABLE 7-2: INTERRUPT REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H AND PIC32MX575F512H DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	IC3EIF	IC2EIF	IC1EIF	—	—	CAN1IF	USBIF	FCEIF	DMA7IF(2)	DMA6IF(2)	DMA5IF(2)	DMA4IF(2)	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	—	—	—	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	IC3EIE	IC2EIE	IC1EIE	—	—	CAN1IE	USBIE	FCEIE	DMA7IE(2)	DMA6IE(2)	DMA5IE(2)	DMA4IE(2)	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	—	—	—	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: These bits are not available on PIC32MX534/564/664/764 devices.

3: This register does not have associated CLR, SET, and INV registers.

9.2 Control Registers

TABLE 9-1: PREFETCH REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	CHECON(1,2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHECOH	0000
		15:0	—	—	—	—	—	—	DCSZ<1:0>		—	—	PREFEN<1:0>		—	PFMWS<2:0>			0007
4010	CHEACC(1)	31:16	CHEWEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CHEIDX<3:0>				0000
4020	CHETAG(1)	31:16	LTAGBOOT	—	—	—	—	—	—	—	LTAG<23:16>								00xx
		15:0	LTAG<15:4>												LVALID	LLOCK	LTYPE	—	xxx2
4030	CHEMSK(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LMASK<15:5>											—	—	—	—	—	0000
4040	CHEW0	31:16	CHEW0<31:0>																xxxx
		15:0																	xxxx
4050	CHEW1	31:16	CHEW1<31:0>																xxxx
		15:0																	xxxx
4060	CHEW2	31:16	CHEW2<31:0>																xxxx
		15:0																	xxxx
4070	CHEW3	31:16	CHEW3<31:0>																xxxx
		15:0																	xxxx
4080	CHELRU	31:16	—	—	—	—	—	—	—	CHELRU<24:16>									0000
		15:0	CHELRU<15:0>																0000
4090	CHEHIT	31:16	CHEHIT<31:0>																xxxx
		15:0																	xxxx
40A0	CHEMIS	31:16	CHEMIS<31:0>																xxxx
		15:0																	xxxx
40C0	CHEPFABT	31:16	CHEPFABT<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: Reset value is dependent on DEVCFGx configuration.

REGISTER 10-5: DCRCDATA: DMA CRC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return '0' on any read.

REGISTER 10-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
0 = No interrupt is pending

REGISTER 11-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE(1)	URSTIE(2) / DETACHIE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
- 1 = STALL interrupt is enabled
- 0 = STALL interrupt is disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit
- 1 = ATTACH interrupt is enabled
- 0 = ATTACH interrupt is disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit
- 1 = RESUME interrupt is enabled
- 0 = RESUME interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
- 1 = Idle interrupt is enabled
- 0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
- 1 = TRNIF interrupt is enabled
- 0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
- 1 = SOFIF interrupt is enabled
- 0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
- 1 = USB Error interrupt is enabled
- 0 = USB Error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
- 1 = URSTIF interrupt is enabled
- 0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit(3)
- 1 = DATTCHIF interrupt is enabled
- 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.
2: Device mode.
3: Host mode.

12.1 Parallel I/O (PIO) Ports

All port pins have three registers (TRIS, LAT and PORT) that are directly associated with their operation.

TRIS is a Data Direction or Tri-State Control register that determines whether a digital pin is an input or an output. Setting a TRISx register bit = 1, configures the corresponding I/O pin as an input; setting a TRISx register bit = 0, configures the corresponding I/O pin as an output. All port I/O pins are defined as inputs after a device Reset. Certain I/O pins are shared with analog peripherals and default to analog inputs after a device Reset.

PORT is a register used to read the current state of the signal applied to the port I/O pins. Writing to a PORTx register performs a write to the port's latch, LATx register, latching the data to the port's I/O pins.

LAT is a register used to write data to the port I/O pins. The LATx Latch register holds the data written to either the LATx or PORTx registers. Reading the LATx Latch register reads the last value written to the corresponding PORT or Latch register.

Not all port I/O pins are implemented on some devices, therefore, the corresponding PORTx, LATx and TRISx register bits will read as zeros.

12.1.1 CLR, SET AND INV REGISTERS

Every I/O module register has a corresponding Clear (CLR), Set (SET) and Invert (INV) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

Note:	Using a PORTxINV register to toggle a bit is recommended because the operation is performed in hardware atomically, using fewer instructions, as compared to the traditional read-modify-write method, as follows: `PORTC ^ = 0x0001;`

12.1.2 DIGITAL INPUTS

Pins are configured as digital inputs by setting the corresponding TRIS register bits = 1. When configured as inputs, they are either TTL buffers or Schmitt Triggers. Several digital pins share functionality with analog inputs and default to the analog inputs at POR. Setting the corresponding bit in the AD1PCFG register = 1 enables the pin as a digital pin.

The maximum input voltage allowed on the input pins is the same as the maximum V_{IH} specification. Refer to **Section 32.0 "Electrical Characteristics"** for V_{IH} specification details.

Note:	Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

12.1.3 ANALOG INPUTS

Certain pins can be configured as analog inputs used by the ADC and comparator modules. Setting the corresponding bits in the AD1PCFG register = 0 enables the pin as an analog input pin and must have the corresponding TRIS bit set = 1 (input). If the TRIS bit is cleared = 0 (output), the digital output level (V_{OH} or V_{OL}) will be converted. Any time a port I/O pin is configured as analog, its digital input is disabled and the corresponding PORTx register bit will read '0'. The AD1PCFG register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

12.1.4 DIGITAL OUTPUTS

Pins are configured as digital outputs by setting the corresponding TRIS register bits = 0. When configured as digital outputs, these pins are CMOS drivers or can be configured as open-drain outputs by setting the corresponding bits in the Open-Drain Configuration (ODCx) register.

The open-drain feature allows generation of outputs higher than V_{DD} (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

See the **"Device Pin Tables"** section for the available pins and their functionality.

12.1.5 ANALOG OUTPUTS

Certain pins can be configured as analog outputs, such as the CV_{REF} output voltage used by the comparator module. Configuring the comparator reference module to provide this output will present the analog output voltage on the pin, independent of the TRIS register setting for the corresponding pin.

12.1.6 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports (CNx) allows devices to generate interrupt requests in response to change-of-state on selected pin.

Each CNx pin also has a weak pull-up, which acts as a current source connected to the pin. The pull-ups are enabled by setting the corresponding bit in the CNPUE register.

TABLE 19-1: I2C1THROUGH I2C5 REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5230	I2C5MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5240	I2C5BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5250	I2C5TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
5260	I2C5RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000
5300	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5310	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5320	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
5330	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5340	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5350	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
5360	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000
5400	I2C2CON(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5410	I2C2STAT(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5420	I2C2ADD(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
5430	I2C2MSK(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5440	I2C2BRG(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5450	I2C2TRN(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
5460	I2C2RCV(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This register is not available on 64-pin devices.

REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(2)

11111111 = Alarm will trigger 256 times

•

•

•

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note:	This register is only reset on a Power-on Reset (POR).

23.1 Control Registers

TABLE 23-1: ADC REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	AD1CON1(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE	0000
9010	AD1CON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000
9020	AD1CON3(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>								0000
9040	AD1CHS(1)	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9060	AD1PCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
9050	AD1CSSL(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16	ADC Result Word 0 (ADC1BUF0<31:0>)																0000
		15:0																	0000
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)																0000
		15:0																	0000
9090	ADC1BUF2	31:16	ADC Result Word 2 (ADC1BUF2<31:0>)																0000
		15:0																	0000
90A0	ADC1BUF3	31:16	ADC Result Word 3 (ADC1BUF3<31:0>)																0000
		15:0																	0000
90B0	ADC1BUF4	31:16	ADC Result Word 4 (ADC1BUF4<31:0>)																0000
		15:0																	0000
90C0	ADC1BUF5	31:16	ADC Result Word 5 (ADC1BUF5<31:0>)																0000
		15:0																	0000
90D0	ADC1BUF6	31:16	ADC Result Word 6 (ADC1BUF6<31:0>)																0000
		15:0																	0000
90E0	ADC1BUF7	31:16	ADC Result Word 7 (ADC1BUF7<31:0>)																0000
		15:0																	0000
90F0	ADC1BUF8	31:16	ADC Result Word 8 (ADC1BUF8<31:0>)																0000
		15:0																	0000
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)																0000
		15:0																	0000
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 24-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6 (CONTINUED)

bit 15 **FLTEN25:** Filter 25 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL25<1:0>:** Filter 25 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL25<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN24:** Filter 24 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL24<1:0>:** Filter 24 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL24<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

28.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This section describes power-saving features for the PIC32MX5XX/6XX/7XX family of devices. These devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

28.1 Power-Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the Peripheral Bus Clock (PBCLK) and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- SOSC Run mode: the CPU is clocked from the SOSC clock source.

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

28.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- **POSC Idle mode:** the system clock is derived from the POSC. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- **FRC Idle mode:** the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- **SOSC Idle mode:** the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- **LPRC Idle mode:** the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- **Sleep mode:** the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

28.3 Power-Saving Operation

Peripherals and the CPU can be halted or disabled to further reduce power consumption.

28.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See **Section 28.3.3 "Peripheral Bus Scaling Method"** for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit, if enabled, remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

30.0 INSTRUCTION SET

The PIC32MX5XX/6XX/7XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core Extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

NOTES:

Revision D (May 2010)

The revision includes the following updates, as described in Table B-3:

TABLE B-3: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"	Updated the initial Flash memory range to 64K. Updated the initial SRAM memory range to 16K. Added the following devices (see Table 1, Table 2, Table 3 and the Pin Diagrams): • PIC32MX534F064H • PIC32MX564F064H • PIC32MX664F064H • PIC32MX564F128H • PIC32MX664F128H • PIC32MX764F128H • PIC32MX534F064L • PIC32MX564F064L • PIC32MX664F064L • PIC32MX564F128L • PIC32MX664F128L • PIC32MX764F128L
4.0 "Memory Organization"	Added new Memory Maps (Figure 4-1, Figure 4-2 and Figure 4-3). The bit named I2CSIF was changed to I2C1SIF and the bit named I2CBIF was changed to I2C1BIF in the Interrupt Register Map tables (Table 4-2, Table 4-3, Table 4-4, Table 4-5, Table 4-6 and Table 4-7) Added the following devices to the Interrupt Register Map (Table 4-2): • PIC32MX534F064H • PIC32MX564F064H • PIC32MX564F128H Added the following devices to the Interrupt Register Map (Table 4-3): • PIC32MX664F064H • PIC32MX664F128H Added the following device to the Interrupt Register Map (Table 4-4): • PIC32MX764F128H Added the following devices to the Interrupt Register Map (Table 4-5): • PIC32MX534F064L • PIC32MX564F064L • PIC32MX564F128L Added the following devices to the Interrupt Register Map (Table 4-6): • PIC32MX664F064L • PIC32MX664F128L Added the following device to the Interrupt Register Map (Table 4-7): • PIC32MX764F128L