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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	M68000
Number of Cores/Bus Width	1 Core, 8/16-Bit
Speed	20MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	132-BQFP Bumpered
Supplier Device Package	132-PQFP (24.13x24.13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68302ceh20c

Table 2-3. M68000 Instruction Type Variations

Instruction Type	Variation	Description
ADD	ADD ADDA ADDQ ADDI ADDX	Add Add Address Add Quick Add Immediate Add with Extend
AND	AND ANDI ANDI to CCR ANDI to SR	Logical AND And Immediate And Immediate to Condition Codes And Immediate to Status Registers
CMP	CMP CMPA CMPM CMPI	Compare Compare Addresses Compare Memory Compare Immediate
EOR	EOR EORI EORI to CCR EORI to SR	Exclusive OR Exclusive OR Immediate Exclusive OR Immediate to Condition Codes Exclusive OR Immediate to Status Register
MOVE	MOVE MOVEA MOVEM MOVEP MOVEQ MOVE from SR MOVE to SR MOVE to CCR MOVE USP	Move Source to Destination Move Address Move Multiple Register Move Peripheral Data Move Quick Move from Status Register Move to Status Register Move to Condition Codes Move User Stack Pointer
NEG	NEG NEGX	Negate Negate with Extend
OR	OR ORI ORI to CCR ORI to SR	Logical OR OR Immediate OR Immediate to Condition Codes OR Immediate to Status Register
SUB	SUB SUBA SUBI SUBQ SUBX	Subtract Subtract Address Subtract Immediate Subtract Quick Subtract with Extend

2.3 ADDRESS SPACES

The M68000 microprocessor operates in one of two privilege states: user or supervisor. The privilege state determines which operations are legal, which operations are used by the external memory management device to control and translate accesses, and which operations are used to choose between the SSP and the USP in instruction references. The M68000 address spaces are shown in Table 2-4.

In the M68000 Family, the address spaces are indicated by function code pins. On the M68000, three function code pins are output from the device on every bus cycle of every executed instruction. This provides the purpose of each bus cycle to external logic.

Table 2-5. M68000 Exception Vector Assignment

11	44	02C	SD	Line 1111 Emulator
12[1]	48	030	SD	(Unassigned, Reserved)
13[1]	52	034	SD	(Unassigned, Reserved)
14[1]	56	038	SD	(Unassigned, Reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16–23[1]	64	040	SD	(Unassigned, Reserved)
	92	05C	SD	
24	96	060	SD	Spurious Interrupt[3]
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32–47	128	080	SD	TRAP Instruction Vectors[4]
	188	0BC	SD	
48–63[1]	192	0C0	SD	(Unassigned, Reserved)
	255	0FC	SD	
64–255	256	100	SD	User Interrupt Vectors
	1020	3FC	SD	

NOTES:

1. Vector numbers 12–14, 16–23, and 48–63 are reserved for future enhancements by Motorola (with vectors 60–63 being used by the M68302 (see 2.7 MC68302 IMP Configuration and Control)). No user peripheral devices should be assigned these numbers.
2. Unlike the other vectors which only require two words, reset vector (0) requires four words and is located in the supervisor program space.
3. The spurious interrupt vector is taken when there is a bus error indication during interrupt processing.
4. TRAP # n uses vector number 32 + n.

2.4.2 Exception Stacking Order

Exception processing saves the most volatile portion of the current processor context on top of the supervisor stack. This context is organized in a format called the exception stack frame. The amount and type of information saved on the stack is determined by the type of exception. The reset exception causes the M68000 to halt current execution and to read a new SSP and PC as shown in Table 2-5. A bus error or address error causes the M68000 to store the information shown in Figure 2-3. The interrupts, traps, illegal instructions, and trace stack frames are shown in Figure 2-4.

External Device Termination

If desired, a transfer may be terminated by the device even before the BCR is decremented to zero. If $\overline{\text{DONE}}$ is asserted one setup time prior to the S5 falling edge (i.e., before or with $\overline{\text{DTACK}}$) during a device access, then the channel operation will be terminated following the operand transfer (see the DNS bit in the CSR). STR is cleared, and an interrupt is generated if INTN is set. The BCR is also decremented, and the SAPR and/or DAPR are incremented in the normal fashion. The use of DONE is not limited to external request generation only; it may also be used to externally terminate an internally generated IDMA transfer sequence.

Error Termination

When a fatal error occurs during an IDMA bus cycle, a bus error is used to abort the cycle and terminate the channel operation. STR is cleared, either BED or BES is set, and an error interrupt is generated if INTE is set.

3.1.5 IDMA Programming

Once the channel has been initialized with all parameters required for a transfer operation, it is started by setting the start operation (STR) bit in the CMR. After the channel has been started, any register that describes the current operation may be read but not modified (SAPR/DAPR, FCR, or BCR).

Once STR has been set, the channel is active and either accepts operand transfer requests in external mode or generates requests automatically in internal mode. When the first valid external request is recognized, the IDMA arbitrates for the bus. The $\overline{\text{DREQ}}$ input is ignored until STR is set.

STR is cleared automatically when the BCR reaches zero and the channel transfer is either terminated by $\overline{\text{DONE}}$ or the IDMA cycle is terminated by a bus error.

Channel transfer operation may be suspended at any time by clearing STR. In response, any operand transfer in progress will be completed, and the bus will be released. No further bus cycles will be started while STR remains negated. During this time, the M68000 core may access IDMA internal registers to determine channel status or to alter operation. When STR is set again, if a transfer request is pending, the IDMA will arbitrate for the bus and continue normal operation.

Interrupt handling for the IDMA is configured globally through the interrupt pending register (IPR), the IMR, and the interrupt in-service register (ISR). Within the CMR in the IDMA, two bits are used to either mask or enable the presence of an interrupt reported in the CSR of the IDMA. One bit is used for masking normal termination; the other bit is used for masking error termination. When these interrupt mask bits in the CMR (INTN and INTE) are cleared and the IDMA status changes, status bits are set in the CSR but not in the IPR. When either INTN or INTE is set and the corresponding event occurs, the appropriate bit is set in the IPR, and, if this bit is not masked, the interrupt controller will interrupt the M68000 core.

Table 3-5. Encoding the Interrupt Vector

Priority Level	5-Bit Vector	Interrupt Source
7 (Highest)	10111	External Device
6	10110	External Device
5	None	External Device
4	01111	General-Purpose Interrupt 3 (PB11)
4	01110	General-Purpose Interrupt 2 (PB10)
4	01101	SCC1
4	01100	SDMA Channels Bus Error
4	01011	IDMA Channel
4	01010	SCC2
4	01001	Timer 1
4	01000	SCC3
4	00111	General-Purpose Interrupt 1 (PB9)
4	00110	Timer 2
4	00101	SCP
4	00100	Timer 3
4	00011	SMC1
4	00010	SMC2
4	00001	General-Purpose Interrupt 0 (PB8)
4	00000	Error
3	None	External Device
2	None	External Device
1 (Lowest)	10001	External Device

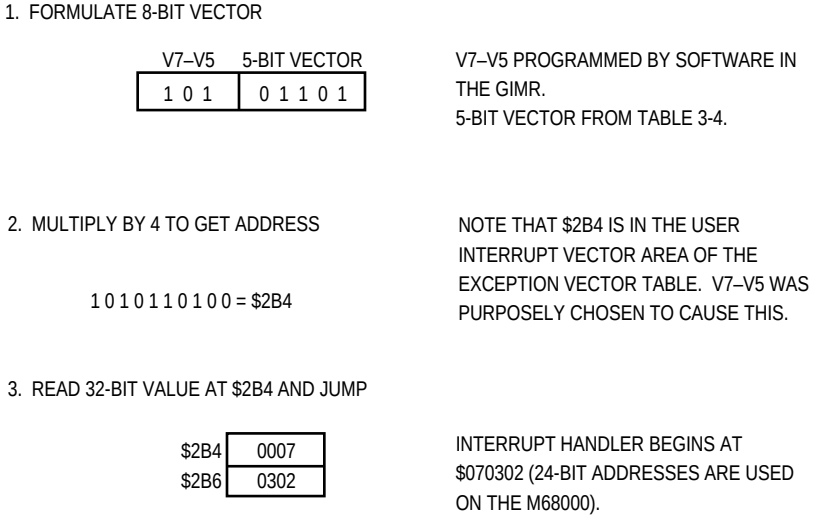

Figure 3-4. SCC1 Vector Calculation Example

Port A Control Register(PACNT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA

0 = I/O 1 = Peripheral

Port A Data Direction Register(PADDR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA

0 = Input 1 = Output

Port A Data Register(PADAT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA

Port B Control Register(PBCNT)

15	8	7	6	5	4	3	2	1	0
RESERVED		CB	CB	CB	CB	CB	CB	CB	CB

0 = I/O 1 = Peripheral

Port B Data Direction Register(PBDDR)

15	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB

0 = Input 1 = Output

Port B Data Register(PBDAT)

15	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PB	PB	PB	PB	PB	PB	PB	PB	PB	PB	PB	PB

Figure 3-6. Parallel I/O Port Registers

3.4 DUAL-PORT RAM

The CP has 1152 bytes of static RAM configured as a dual-port memory. The dual-port RAM can be accessed by the CP main controller or by one of three bus masters: the M68000 core, the IDMA, or an external master. The M68000 core and the IDMA access the RAM synchro-

At the end of the STOP instruction, a major change to the IMP occurs. The M68000 core immediately goes into a standby state in which it executes no instructions. In this state, the clock internally sent to the M68000 core is internally divided, saving power. The amount of this divide ratio is configured by the user. At the same time, however, the rest of the IMP continues to operate at the normal system frequency (i.e., the frequency on the EXTAL pin). All peripherals continue to operate normally during this time. Also, during low-power modes, all IMP external signals continue to function normally and at full speed.

In all modes, any of the 16 possible internal interrupt request (INRQ) sources can cause the IMP to leave a low-power mode. Masked interrupt sources will never cause a lower power mode to be exited. If it is desired to have an external signal cause the IMP to exit a low-power mode, it must be routed to one of the PB11–PB8 port pins with interrupt capability, so that an INRQ interrupt can be generated.

There are three low-power modes: low power, lowest power, and lowest power with external clock. Low-power mode allows execution to resume immediately upon recognition of the interrupt, with no loss of any IMP state information. Lowest power mode requires execution to resume with an internal M68000 reset. The M68000 state is lost, but the rest of the IMP peripheral states are completely retained. The lowest power mode with external clock offers the absolute minimum power consumption with the IMP, but requires external hardware.

3.8.7.2.1 Low-Power Mode

This mode is possible if the user-selected low-power frequency applied to the M68000 core remains above the operating limits specified in Section 6 Electrical Characteristics (e.g., 8 MHz). In this mode, LPREC is set to zero. Once an INRQ interrupt becomes pending, the system control block switches the M68000 core back to full frequency and power, and begins handling the interrupt in the usual manner. No M68000 core or peripheral status is lost in this mode. Note: The CLKO signal will remain at the same frequency that is on the EXTAL input.

The following list gives a step-by-step example of how to use the low-power mode. For this example, an interrupt from either timer 1 or timer 2 causes the IMP to exit the low-power mode. This example also assumes an initial operating frequency of 16.67 MHz for the IMP.

1. Set the lower byte of the SCR (location $F7) to $20. This sets the LPEN bit and sets the clock divider to a value of 2 (divide by 2).
2. Disable all interrupts except TIMER1 and TIMER2 in the IMR.
3. Turn off any unneeded peripherals, such as the SCCs, by clearing the ENR and ENT bits. Also turn off any unneeded baud rate generators by setting the EXTC bits in the SCON registers. This procedure can save as much as 4 mA per SCC at 16.67 MHz. (EXTC is cleared by default on power-on reset.)
4. Execute the STOP instruction. The low-power mode is now entered.
5. When a timer 1 or 2 interrupt occurs, the M68000 resumes execution with the timer 1 or 2 interrupt handler. After the RTE instruction, execution continues with the instruction following the STOP instruction in step 4 above. All IMP state information is retained.

4.4.1 IDL Interface

The IDL interface is a full-duplex ISDN interface used to interconnect a physical layer device (such as the Motorola ISDN S/T transceiver MC145474) to the integrated multiprotocol processor (IMP). Data on five channels (B1, B2, D, A, and M) is transferred in a 20-bit frame every 125 µs, providing 160-kbps full-duplex bandwidth. The IMP is an IDL slave device that is clocked by the IDL bus master (physical layer device). The IMP provides direct connections to the MC145474. Refer to Figure 4-6 for the IDL bus signals.

The IMP supports 10-bit IDL as shown in Figure 4-6; it does not support 8-bit IDL.

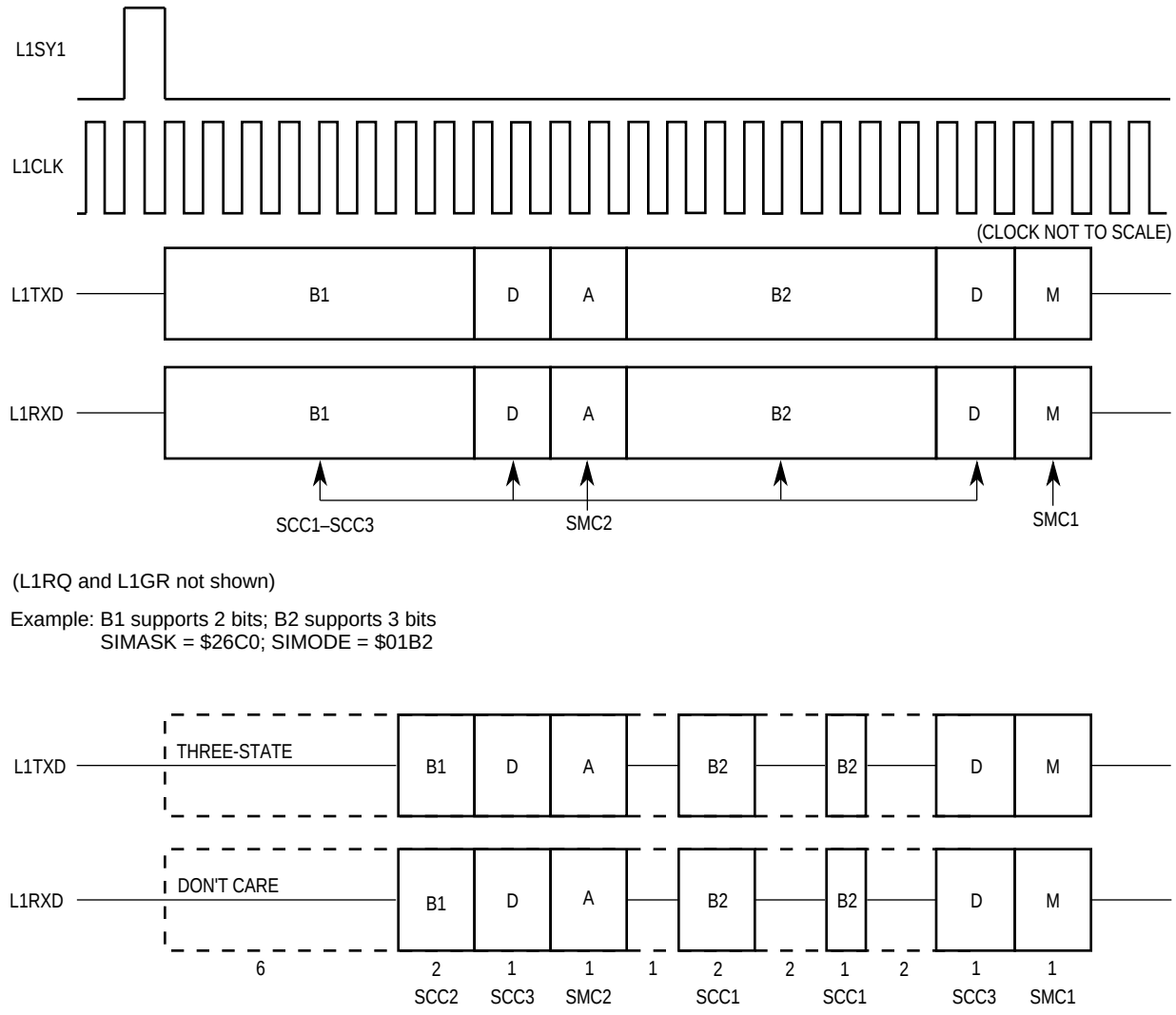

Figure 4-6. IDL Bus Signals

An application of the IDL interface is to build a basic rate ISDN terminal adaptor (see Figure 4-7). In such an application, the IDL interface is used to connect the 2B + D channels between the IMP, CODEC, and S/T transceiver. One of the IMP SCCs would be configured to HDLC mode to handle the D channel; another IMP SCC would be used to rate adapt the

The monitor channel is used to transfer data between layer-1 devices and the control unit (i.e., the M68000 core). The command/indication channel is used to control activation/deactivation procedures or for the switching of test loops by the control unit.

The IMP supports all five channels of the GCI channel 0. The following table shows where each channel can be routed. The two B channels can be concatenated and routed to the same SCC channel.

GCI Channel 0	Serial Controllers
D	SCC1, SCC2, SCC3
B1	SCC1, SCC2, SCC3
B2	SCC1, SCC2, SCC3
M	SMC1
C/I	SMC2

The GCI interface supports the CCITT I.460 recommendation for data rate adaptation. The GCI interface can access each bit of the B channel as an 8-kbps channel. The mask register (SIMASK) for the B channels specifies which bits are supported by the GCI interface. The receiver will receive only the bits that are enabled by SIMASK; the transmitter will transmit only the bits that are enabled by SIMASK and will not drive the L1TXD pin otherwise (L1TXD in GCI mode is an open-drain output).

The IMP supports contention detection on the D channel. When the IMP has data to transmit on the D channel, it checks bit 4 of the SCIT C/I channel 2. The physical layer device monitors the physical layer bus for activity on the D channel and indicates with this bit that the channel is free. If a collision is detected on the D channel, the physical layer device sets bit 4 of C/I channel 2 to logic high. The IMP then aborts its transmission and retransmits the frame when this bit is asserted again. This procedure is handled automatically for the first two buffers of a frame. The L1GR line may also be used for access to the S interface D channel. This signal is checked by the IMP, and the physical layer device should indicate that the S interface D channel is free by asserting L1GR.

In the deactivated state, the clock pulse is disabled, and the data line is a logic one. The layer-1 device activates the IMP by enabling the clock pulses and by an indication in the channel 0 C/I channel. The IMP will then report to the M68000 core by a maskable interrupt that a valid indication is in the SMC2 receive buffer descriptor.

When the M68000 core activates the line, it sets SETZ in the serial interface mode (SIMODE) register, causing the data output from L1TXD to become a logic zero. Code 0 (command timing TIM) will be transmitted on channel 0 C/I channel to the layer-1 device until the SETZ is reset. The physical layer device will resume transmitting the clock pulses and will give an indication in the channel 0 C/I channel. The M68000 core should reset SETZ to enable data output.

4.4.3 PCM Highway Mode

In PCM highway mode, one, two, or all three SCCs can be multiplexed together to support various time-division multiplexed interfaces. PCM highway supports the standard T1 and CEPT interfaces as well as user-defined interfaces. In this mode, the NMSI1 pins have new names and functions (see Table 4-2).

NMSI mode. The SIMODE register is a memory-mapped read-write register cleared by reset.

15	14	13	12	11	10	9	8
SETZ	SYNC/SCIT	SDIAG1	SDIAG0	SDC2	SDC1	B2RB	B2RA

7	6	5	4	3	2	1	0
B1RB	B1RA	DRB	DRA	MSC3	MSC2	MS1	MS0

SETZ—Set L1TXD to zero (valid only for the GCI interface)

0 = Normal operation
1 = L1TXD output set to a logic zero (used in GCI activation, refer to 4.4.2 GCI Interface)

SYNC/SCIT—SYNC Mode/SCIT Select Support

SYNC is valid only in PCM mode.

0 = One pulse wide prior to the 8-bit data
1 = N pulses wide and envelopes the N-bit data

The SCIT (Special Circuit Interface T) interface mode is valid only in GCI mode.

0 = SCIT support disabled
1 = SCIT D-channel collision enabled. Bit 4 of channel 2 C/I used by the IMP for receiving indication on the availability of the S interface D channel.

SDIAG1–SDIAG0—Serial Interface Diagnostic Mode (NMSI1 Pins Only)

00 = Normal operation
01 = Automatic echo
The channel automatically retransmits the received data on a bit-by-bit basis. The receiver operates normally, but the transmitter can only retransmit received data. In this mode, L1GR is ignored.
10 = Internal loopback
The transmitter output (L1TXD) is internally connected to the receiver input (L1RXD). The receiver and the transmitter operate normally. Transmitted data appears on the L1TXD pin, and any external data received on L1RXD pin is ignored. In this mode, L1RQ is asserted normally, and L1GR is ignored.
11 = Loopback control
In this mode, the transmitter output (TXD1/L1TXD) is internally connected to the receiver input (RXD1/L1RXD). The TXD1/L1TXD, TXD2, TXD3, $\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$, and $\overline{\text{RTS3}}$ pins will be high, but L1TXD will be three-stated in IDL and PCM modes. This mode may be used to accomplish multiplex mode loopback testing without affecting the multiplexed layer 1 interface. It also prevents an SCC's individual loopback (configured in the SCM) from affecting the pins of its associated NMSI interface.

character of 9 to 13 consecutive ones (if UM1–UM0 = 00) or by the address bit of the next message (if UM0 = 1).

When the receiver is in sleep mode and a break sequence is received, the receiver will increment the BRKEC counter and generate the BRK interrupt (if enabled).

4.5.11.11 UART Error-Handling Procedure

The UART controller reports character reception and transmission error conditions through the channel BDs, the error counters, and the UART event register (SCCE). The modem interface lines can also be monitored directly by the SCC status register.

Transmission Error

Clear to Send Lost During Character Transmission. When this error occurs and the channel is not programmed to control this line with software, the channel terminates buffer transmission, closes the buffer, sets the CTS lost (CT) bit in the BD, and generates the TX interrupt (if enabled). The channel will resume transmission after the reception of the RESTART TRANSMIT command.

Reception Errors

1. Overrun Error. The UART controller maintains an internal three-byte FIFO for receiving data. The CP begins programming the SDMA channel (if the data buffer is in external memory) when the first byte is received into the FIFO. When a receiver FIFO overrun occurs, the channel writes the received character into the internal FIFO over the previously received character (the previous character and its status bits are lost). Then the channel writes the received character to the buffer, closes the buffer, sets overrun (OV) in the BD, and generates the RX interrupt (if enabled). In automatic multidrop mode, the receiver enters hunt mode immediately.
2. Carrier Detect Lost During Character Reception. When this error occurs and the channel is not programmed to control this line with software, the channel terminates character reception, closes the buffer, sets the carrier detect lost (CD) bit in the BD, and generates the RX interrupt (if enabled). This error's priority is the highest; the last character in the buffer is lost and other errors are not checked. In automatic multidrop mode, the receiver enters hunt mode immediately.
3. Framing Error. Framing error is reported by the UART controller when no stop bit is detected in a received data string. When this error occurs, the channel writes the received character to the buffer, closes the buffer, sets framing error (FR) in the BD, and generates the RX interrupt (if enabled). The channel also increments the framing error counter (FRMEC). When this error occurs, parity is not checked for this character. In automatic multidrop mode, the receiver enters hunt mode immediately.
4. Parity Error. When the parity error occurs, the channel writes the received character to the buffer, closes the buffer, sets parity error (PR) in the BD, and generates the RX interrupt (if enabled). The channel also increments the parity error counter (PAREC). In automatic multidrop mode, the receiver enters hunt mode immediately.
5. Noise Error. Noise error is detected by the UART controller when the three samples taken on every bit are not identical. When this error occurs, the channel writes the received character to the buffer and proceeds normally but increments the noise error

CD—Carrier Detect Lost

The carrier detect signal was negated during message reception.

Data Length

Data length contains the number of octets written by the CP into this BD's data buffer. It is written by the CP once as the BD is closed.

NOTE

The actual amount of memory allocated for this buffer should be greater than or equal to the contents of maximum receive buffer length register (MRBLR).

Rx Buffer Pointer

The receive buffer pointer, which always points to the first location of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.11.15 UART Transmit Buffer Descriptor (Tx BD)

Data is presented to the CP for transmission on an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The CP confirms transmission (or indicates error conditions) through the BDs to inform the M68000 core that the buffers have been serviced. The Tx BD shown in Figure 4-22.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	CR	A	P	—	—	—	—	—	—	—	—	CT
OFFSET + 2	DATA LENGTH															
OFFSET + 4 OFFSET +6	TX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															

Figure 4-22. UART Transmit Buffer Descriptor

The first word of the Tx BD contains status and control bits. The following bits are prepared by the user before transmission and set by the CP after the buffer has been transmitted.

R—Ready

0 = This buffer is not currently ready for transmission. The user is free to manipulate the BD (or its associated buffer). The CP clears this bit after the buffer has been transmitted or after an error condition has been encountered.

1 = The data buffer, which has been prepared for transmission by the user, has not been transmitted or is currently transmitting. No fields of this BD may be written by the user once this bit is set.

CR—Rx CRC Error

This frame contains a CRC error.

OV—Overrun

A receiver overrun occurred during frame reception.

CD—Carrier Detect Lost

The carrier detect signal was negated during frame reception. This bit is valid only when working in NMSI mode.

Data Length

The data length is the number of octets written to this BD's data buffer by the HDLC controller. It is written by the CP once as the BD is closed.

When this BD is the last BD in the frame (L = 1), the data length contains the total number of frame octets (including any previous linked receive data buffers and two or four bytes for the CRC) in the frame. This behavior is useful for determining the total number of octets received, even if MFLR was exceeded.

NOTE

The actual amount of memory allocated for this buffer should be even and greater than or equal to the contents of maximum receive buffer length register (MRBLR).

Rx Buffer Pointer

The receive buffer pointer, which always points to the first location of the associated data buffer, may reside in either internal or external memory.

NOTE

The Rx buffer pointer must be even, and the upper 8 bits must of the pointer must be zero for the function codes to operate correctly.

4.5.12.11 HDLC Transmit Buffer Descriptor (Tx BD)

Data is presented to the HDLC controller for transmission on an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The HDLC controller confirms transmission (or indicates error conditions) using the BDs to inform the M68000 core that the buffers have been serviced. The Tx BD is shown in Figure 4-28.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	L	TC	—	—	—	—	—	—	—	—	UN	CT
OFFSET + 2	DATA LENGTHTX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET + 4																
OFFSET + 6																

Figure 4-28. HDLC Transmit Buffer Descriptor

by the M68000 core before setting the STR bit so that received replies may be easily recognized by the software.

4.7 SERIAL MANAGEMENT CONTROLLERS (SMCS)

The SMC key features are as follows:

- Two Modes of Operation:
  - —IDL—SMC1 supports the maintenance channel and SMC2 supports the auxiliary channel
  - —GCI (IOM-2)—SMC1 supports the monitor channel and SMC2 supports the C/I channel
- Full-Duplex Operation
- Local Loopback Capability for Testing

4.7.1 Overview

The SMCs are two synchronous, full-duplex serial management control (SMC) ports. The SMC ports may be configured to operate in either Motorola interchip digital link (IDL) or general circuit interface (GCI) modes. GCI is also known as ISDN oriented modular 2 (IOM-2). See 4.4 Serial Channels Physical Interface for the details of configuring the IDL and GCI interfaces. The SMC ports are not used when the physical serial interface is configured for PCM highway or NMSI modes.

4.7.1.1 Using IDL with the SMCs

In this mode, SMC1 transfers the maintenance (M) bits of the IDL to and from the internal RAM, and SMC2 transfers the auxiliary (A) bits to and from the internal RAM. The CP generates a maskable interrupt upon reception/transmission of eight bits. The SMC1 and SMC2 receivers can be programmed to work in hunt-on-zero mode, in which the receiver will search the line signals for a zero bit. When it is found, the receiver will transfer data to the internal RAM.

4.7.1.2 Using GCI with the SMCs

In this mode, SMC1 controls the GCI monitor channel.

SMC1 Transmission

The monitor channel is used to transfer commands to the layer-1 component. The M68000 core writes the data byte into the SMC1 Tx BD. SMC1 will transmit the data on the monitor channel.

The SMC1 channel transmitter can be programmed to work in one of two modes:

Transparent Mode

In this mode, SMC1 transmits the monitor channel data and the A and E control bits transparently into the channel. When the M68000 core has not written new data to the buffer, the SMC1 transmitter will retransmit the previous monitor channel data and the A and E control bits.

Table 5-1. Signal Definitions

Chip Select	CS3–CS0	4
Testing	$\overline{FRZ}$ (2 Spare)	3
V_{DD}		8
GND		13

All pins except EXTAL, CLKO, and the layer 1 interface pins in IDL mode support TTL levels. EXTAL, when used as an input clock, needs a CMOS level. CLKO supplies a CMOS level output. The IDL interface is specified as a CMOS electrical interface.

All outputs (except CLKO and the GCI pins) drive 130 pF. CLKO is designed to drive 50 pF. The GCI output pins drive 150 pF.

5.2 POWER PINS

The IMP has 21 power supply pins. Careful attention has been paid to reducing IMP noise, potential crosstalk, and RF radiation from the output drivers. Inputs may be +5 V when V_{DD} is 0 V without damaging the device.

- V_{DD} (8)—There are 8 power pins.
- GND (13)—There are 13 ground pins.

NOTE

The Input High Voltage and Input Low Voltage for EXTAL and the values for power are specified in the DC Electrical Characteristics.A valid clock signal oscillates between a low voltage of between V_{SS}-0.3 and .6 volts and a high voltage of between 4.0 and V_{DD} volts. This EXTAL signal must be present within 20 mS after V_{DD} reaches its minimum specified level of 4.5 volts.

6.4 POWER DISSIPATION

Characteristic	Symbol	Typ	Max	Unit
Power Dissipation at 25 MHz- Rev C.8µ (see Notes 1 & 2)	PD	85	130	mA
Power Dissipation at 25 MHz -Rev C.65µ (see Notes 1 & 2)	PD	65	90	mA
Power Dissipation at 20 MHz-Rev C.8µ (see Notes 1 & 2)	PD	65	100	mA
Power Dissipation at 20 MHz-Rev C.65µ (see Notes 1 & 2)	PD	50	80	mA
Power Dissipation at 16.67 MHz-Rev C.8µ (see Notes 1 & 2)	PD	54	85	mA
Power Dissipation at 16.67 MHz-Rev C.65µ (see Notes 1 & 2)	PD	44	70	mA
Power Dissipation at 4 MHz-Rev C.8µ (see Notes 1,2 & 3)	PD	40	-	mA
Power Dissipation at 4 MHz-Rev C.65µ (see Notes 1, 2 & 3)	PD	27	-	mA
Power Dissipation at 3.3V 20 MHz-Rev C.65µ (see Note 2)	PD	30	60	mA
Power Dissipation at 3.3V 16.67 MHz-Rev C.65µ (see Note 2)	PD	25	50	mA

NOTES:
1. Values measured with maximum loading of 130 pF on all output pins. Typical means 5.0 V at 25°C. Maximum means guaranteed maximum over maximum temperature (85°C) and voltage (5.5 V).
2. The IMP is tested with the M68000 core executing, all three baud rate generators enabled and clocking at a rate of 64 kHz, and the two general-purpose timers running with a prescaler of 256. Power measurements are not significantly impacted by baud rate generators or timers until their clocking frequency becomes a much more sizable fraction of the system frequency than in these test conditions.
3. The M68000 core will not operate at 4 MHz. This is only for low power mode.

C.3 CENTRONICS[1] RECEPTION CONTROLLER

With this package, SCC2 is turned into an interface that can receive Centronics data. This package, for example, could be used in a laser printer design requiring a Centronics interface option. The package uses SCC2 (its pins and registers) in addition to PA12, PA13 or PA11, PA14, and PA15.

The main features are as follows:

- Flexible Message-Oriented Data Structure
- Flexible Control Character Comparison
- Controls the $\overline{\text{BUSY}}$ and $\overline{\text{ACK}}$ Signals
- Three Timing Relationships Possible between $\overline{\text{BUSY}}$ and $\overline{\text{ACK}}$
- Supports the SET_BUSY and CLEAR_BUSY Commands
- Programmable Duration (in clock cycles) of the $\overline{\text{ACK}}$ Signal
- Receive Buffer May Be Closed upon a Programmable Silence Period

C.4 PROFIBUS CONTROLLER

Process field bus (PROFIBUS) is a UART-based master-slave protocol that specifies data rates starting at 9.6 kbps. The PROFIBUS microcode running on the IMP RISC controller assists the M68000 core in handling some of the time-critical PROFIBUS link layer functions, leaving more of the M68000 core available for the application software.

The main PROFIBUS controller features are as follows:

- Automatic Frame Synchronization by Searching for the Start Delimiter
- Frame Preceding IDLE Sequence Generation/Checking
- Flexible Frame-Oriented Data Buffers
- Separate Interrupts for Frames and Buffers (Receive and Transmit)
- Maintenance of Six 16-Bit Error Counters
- Two Address Comparison Registers with Mask
- Frame Error, Noise Error, Parity Error Detection
- Detection of IDLE in the Middle of a Frame
- Check Sum Generation/Checking
- End Delimiter (ED) Generation/Checking
- Three Commands

C.5 AUTOBAUD SUPPORT PACKAGE

The package allows a UART to automatically detect the baud rate of a serial stream and adjust to it. This is useful in modem applications that must support an autobaud capability. It is

1. Centronics is a trademark of Centronics.

method works because the parallel I/O lines default as inputs to the MC68302 and can therefore all be pulled high initially. After the slave BARs are programmed, the parallel I/O lines on the master should be reconfigured as inputs; otherwise, a contention could occur on A23 when a slave's DMA is accessing the bus.

This method is the easiest because it requires no external glue. It costs one parallel I/O line per slave on the master MC68302 and reduces the address space of each slave from 16 MB to 8 MB, neither of which should be a problem in most systems. If A23 is really needed on the slaves, it can be regained, but extra logic is required.

D.7.4 Dealing with Interrupts

The following example is the easiest method for dealing with interrupts from the slaves. It assumes that any other external interrupt sources are sent directly to the master MC68302 without using the interrupt controllers on the slaves.

1. The internal interrupts cause the slaves to force out level 4 on their $\overline{IOUT2}$-$\overline{IOUT0}$ pins. (AVEC, RMC, and CS0 are not available on the slaves.)
2. IOUT2 from the slave is connected to the master PB8, PB9, PB10, or PB11 pin if the master is in normal interrupt mode, or to $\overline{IRQ1}$ or $\overline{IRQ6}$ if it is in dedicated interrupt mode. Thus, in normal mode the slave interrupts will arrive at level 4, and in dedicated mode they will arrive at either level 1 or 6.
3. The best method of operation is for the slaves not to generate the vector during the interrupt acknowledge cycle. The master MC68302 can generate it and then read the IPR of the slave to determine the actual source of the interrupt.

NOTE

Why not use the vector generation enable (VGE) bit in each slave MC68302 to allow the slaves to generate different vectors for each of their internal peripherals? This could be done; however, the slaves must be tricked into responding to an unique interrupt level (or else multiple vectors could collide on the bus simultaneously). The external decoding and address buffer logic required to do this slows down the interface timing (and adds expense). Rather, the VGE bit is intended for applications where a single MC68302 is a slave to another processor such as the MC68020.

To use the interrupt controller on a slave MC68302 (in either normal or dedicated mode) to handle interrupt levels 1, 6, or 7 from an external peripheral, connect the slave's $\overline{IOUT2}$-$\overline{IOUT0}$ pins directly to the master's $\overline{IPL2}$-$\overline{IPL0}$ pins. The master MC68302 will supply the vector for levels 1, 6, and 7, and level 4 of the slave will be interpreted as an error vector (00000). Upon branching to this vector, the master MC68302 software should then check the slave's IPR to identify the source.

D.7.5 Arbitration

If only one slave is present, no arbiter is required because the $\overline{BR}$ as an output on the slave can be sent directly to the $\overline{BR}$ input on the master. Figure D-20 shows a dual master-slave system using this arbitration scheme. Note that the $\overline{BCLR}$ pin from the slave MC68302 can be used to give the 12 SDMA channels in the system priority over the two IDMA channels in the system. $\overline{BCLR}$ is asserted whenever an SDMA channel wants the bus, and, will tem-

There is nothing to synchronize on the receive side. As soon as the ENR bit is set, the first time slot for this SCC will begin the reception process. As with the NMSI mode, a word is not written to the buffer until the 9th clock after the serial clock that clocked in the last bit of this word (see D.8.7 Gating Clocks in NMSI Mode). Recall that clocks can only be counted *during* time slots.

D.8.9 PCM Mode Final Thoughts

Since all synchronous protocols work with PCM mode, it is possible to use the regular BISYNC mode to send syncs in the data stream, as described earlier.

When using totally transparent mode with PCM, both the NTSYN and EXSYN bits should normally be set. The DIAG1-DIAG0 bits can be set for either normal mode or software operation with no difference in behavior.

PCM mode does affect the SCCS register. In the SCCS register, the $\overline{CD}$ and $\overline{CTS}$ bits are always zero when the ENR and ENT bits, respectively, are set. The ID bit is not valid in transparent mode, regardless of the physical interface chosen.

Care should always be taken to avoid glitches or ringing on the L1CLK line. If a glitched or ringing L1CLK line causes an extra clock to be inserted during a time slot, there is no way to resynchronize the byte alignment in envelope mode until the ENT synchronization algorithm described previously is followed. This potential problem does lead to one slight advantage of the one-clock-prior method over the envelope sync. With the one-clock-prior method, it is more likely that the glitched clock will only misalign the transfer/reception of a single byte of data, rather than the whole data stream. (However, this cannot be guaranteed—predicting device behavior out-of-spec is extremely difficult.)

D.8.10 Using Transparent Mode with IDL and GCI

Transparent mode can be freely used with the ISDN physical interfaces. Using transparent mode with the ISDN interfaces is especially useful in the B-channels, since the D channel LAPD protocol is typically supported with the SCC in HDLC mode. Transparent data may be sent and received over the 64-kbps B1 channel, the 64-kbps B2 channel, a combined B1-B2 channel with a 128-kbps bandwidth, or subportions of either the B1 or B2 channel or both. (The desired subportions are defined in the SIMASK register.)

With the ISDN interfaces, as with the other types of interfaces, if the SCC is not transmitting data, it will transmit $FFs. If the NTSYN and the EXSYN bits are set in the SCM, data will be byte-aligned within the B1 or B2 channels. Thus, it will only be transmitted once the SCC transmit FIFO is filled and the *beginning* of the B1 or B2 channel occurs.

A special case occurs when the B1 and B2 channels are combined into a single 128-kbps channel. In this case, although data will only appear on byte boundaries, the transmit buffer's data could begin in either the B1 or B2 channels, depending on the timing involved. If this is a problem, the following rule may be observed. If the ENT bit is set at a consistent time during the GCI/IDL frame and if ready bit of the Tx BD is set at a consistent time relative to the GCI/IDL frame (preferably before the ENT bit is set), a consistent starting point of byte alignment (either B1 or B2) can be obtained. If data is then transmitted in a continuous

Bits 7, 6, 2—Reserved for future use

BR—Break Received

0 = No break sequence was detected during reception into this buffer.
1 = A break sequence was detected during reception into this buffer.

FR—Framing Error

0 = No framing error was detected.
1 = A framing error was detected during reception of the last data byte in this buffer.

PR—Parity Error

0 = No parity error was detected.
1 = A character with a parity error was received and is located in the last byte of this buffer.

OV—Overrun

0 = No receiver overrun occurred.
1 = A receiver overrun condition occurred during buffer reception.

CD—Carrier Detect Lost (valid only in NMSI mode)

0 = No CD lost was detected.
1 = CD was negated during buffer reception.

E.2.1.4.2 Receive Buffer Data Length. This 16-bit value is written by the IMP to indicate the number of octets received into the data buffer.

E.2.1.4.3 Receive Buffer Pointer. This 32-bit value is written by the user to indicate the address where the data is to be stored.

E.2.1.5 TRANSMIT BUFFER DESCRIPTORS. Each SCC has eight transmit buffer descriptors. Each buffer descriptor consists of four words as shown below. Reserved bits in registers should be written as zeros.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	CR	A	P	—	—	—	—	—	—	—	—	CT
OFFSET +2	DATA LENGTH															
OFFSET +4	TX BUFFER POINTER															
OFFSET +6																

E.2.1.5.1 Transmit BD Control/Status Word. To initialize the buffer, the user should write bits 15-9 and clear bit 0. The IMP clears bit 15 when the buffer is transmitted or closed due to an error and sets bit 0 depending on which error occurred.

R—Ready

0 = This data buffer is not currently ready for transmission.
1 = This data buffer has been prepared by the user for transmission but has not yet been fully transmitted. Must be set by the user to enable transmission of the buffer.