Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	M68000
Number of Cores/Bus Width	1 Core, 8/16-Bit
Speed	20MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	132-BQFP Bumpered
Supplier Device Package	132-PQFP (24.13x24.13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68302eh20c

1. Calculate what the mask should be. For a 1 Megabyte block, the address lines A0 through A19 are used to address bytes within the block, so they need to be masked out.
2. Write $3E00 to OR2 (DTACK=1 for 1 wait state, M23-M20 = 1 to use these bits in the comparison, M19-M13 = 0 to mask these address bits, MRW = 0 to enable the chip select for both read and write, and CFC = 0 to mask off function code comparison).
3. Write $0401 to BR2 (FC2-FC0 = 0 don't care, A23-A13 = base address, RW = 0 don't care, and EN =1 to enable the chip select.

NOTE

The mask bits in the OR are used to mask the individual address bits, so in the previous example, if bit 12 (M23) was changed to a zero, then CS2 would assert for a 1 Megabyte block beginning at $200000 and a 1 Megabyte block at $A00000.

3.7 ON-CHIP CLOCK GENERATOR

The IMP has an on-chip clock generator that supplies clocks to both the internal M68000 core and peripherals and to an external pin. The clock circuitry uses three dedicated pins: EXTAL, XTAL, and CLKO.

The external clock/crystal (EXTAL) input provides two clock generation options. EXTAL may be used to interface the internal generator to an external crystal (see Figure 3-10). Typical circuit parameters are C1 = C2 = 25 pF and R = 700 kΩ using a parallel resonant crystal. Typical crystal parameters are Co < 10 pF and Rx = 50 Ω. The equivalent load capacitance (C_L) of this circuit is 20 pF, calculated as (C1 + C_{in})/2, where C1 = C2 = 25 pF and C_{in} = 15 pF maximum on the EXTAL pin.

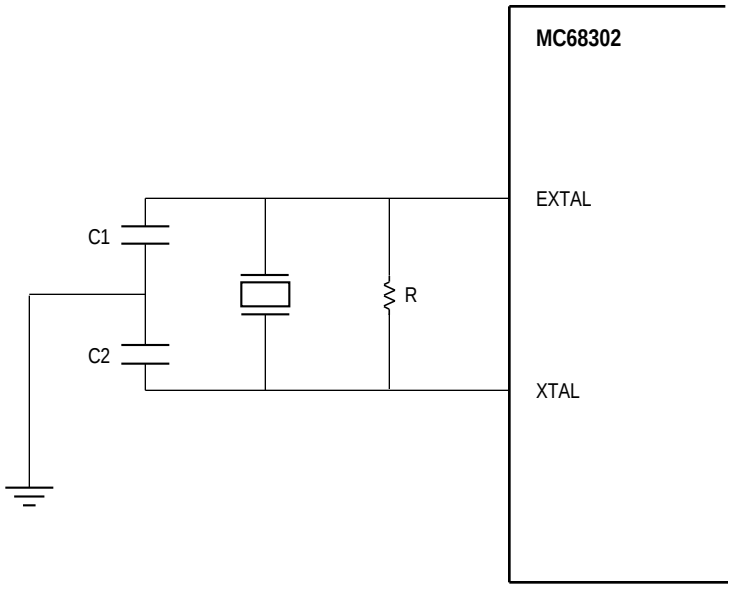


Figure 3-10. Using an External Crystal

Table 3-10. Bus Arbitration Priority Table

$\overline{\text{BCLR}}$ Ignored BCLM = 0	$\overline{\text{BCLR}}$ Used BCLM = 0	$\overline{\text{BCLR}}$ Ignored BCLM = 1	$\overline{\text{BCLR}}$ Used BCLM = 1
$\overline{\text{BR}}$ Pin SDMA IDMA M68000 Interrupts M68000	SDMA IDMA BR Pin M68000 Interrupts M68000	$\overline{\text{BR}}$ Pin SDMA M68000 Interrupts IDMA[4] M68000	SDMA M68000 Interrupts IDMA[4] BR Pin M68000

NOTES:
1. The SDMA on a given IMP always has a higher priority than the IDMA on that IMP.
2. This table assumes the M68000 core is not in disable CPU mode. In disable CPU mode, the SDMA and IDMA make requests to the M68000 bus when they wish to become bus masters.
3. "BCLR Used" means that the BCLR pin is used externally to force the external bus master off the bus, even though its priority is still the highest in the system from the standpoint of the IMP bus arbiter.
4. The bus arbitration priority for IDMA in the two rightmost columns of the table applies only to the case when the IDMA request is internally generated; for the cases of external request, the bus arbitration priority of IDMA is right below that of SDMA.

The IMP bus arbiter also supports an M68000 core low-interrupt latency option. When the M68000 core processor has an unmasked interrupt request, it asserts an internal interrupt pending signal (IPEND). The bus arbiter uses this signal according to BCLM in the SCR to assert external ($\overline{\text{BCLR}}$) and internal bus-clear (IBCLR) signals. These bus-clear signals allow the M68000 core to eliminate long latencies potentially associated with an external bus master or the IDMA, respectively.

The external $\overline{\text{BCLR}}$ is asserted whenever 1) one of the SDMA channels requests the bus when the IDMA is not the bus master or 2) the M68000 core has an unmasked pending interrupt request, provided BCLM in the SCR is set. In this case, $\overline{\text{BCLR}}$ will be asserted until the interrupt priority active (IPA) bit in the SCR is cleared. To implement this feature, $\overline{\text{BCLR}}$ would be used to force external devices to release bus ownership.

IBCLR to the IDMA is asserted whenever 1) an external bus master requests the bus ($\overline{\text{BR}}$ asserted); 2) the M68000 core has an unmasked pending interrupt request, provided BCLM in the SCR is set and the IDMA request is internally generated, and in this case, BCLR will be asserted until IPA is cleared (Note that $\overline{\text{BCLR}}$ could be used to negate $\overline{\text{DREQ}}$ when the IDMA is in external request mode); 3) the M68000 CPU is disabled, and BCLR is asserted.

The IBCLR signal causes the IDMA to release bus ownership at the end of the current operand transfer. IBCLR is not routed to the SDMA channels since they always release bus ownership after one operand transfer.

RMC is issued by the M68000 core and can be used by the internal bus arbiter to delay issuance of BG during read-modify-write cycles. This is controlled by the RMCST bit in the SCR. Otherwise, the MC68000/MC68008 core may be forced off the bus after any bus cycle.

3.8.5.2 External Bus Arbitration

An external bus master may gain ownership of the M68000 bus by asserting the bus request ($\overline{\text{BR}}$) pin. After gaining ownership, it may access the IMP registers or RAM or any system memory address. Chip selects and system control functions, such as the hardware watchdog, continue to operate.

OPCODE—Command Opcode

These bits are set by the M68000 core to define the specific SCC command. The precise meaning of each command below depends on the protocol chosen.

00 = STOP TRANSMIT Command
01 = RESTART TRANSMIT Command
10 = ENTER HUNT MODE Command
11 = RESET RECEIVER BCS CALCULATION (used only in BISYNC mode)

The detailed command description for the UART protocol is presented in 4.5.11 UART Controller.

The detailed command description for the HDLC protocol is presented in 4.5.12 HDLC Controller.

The detailed command description for the BISYNC protocol is presented in 4.5.13 BISYNC Controller.

The detailed command description for the DDCMP protocol is presented in 4.5.14 DDCMP Controller.

The detailed command description for the V.110 protocol is presented in 4.5.15 V.110 Controller.

The detailed command description for the transparent protocol is presented in 4.5.16 Transparent Controller.

1 = When GCI is set in conjunction with the opcode bits, the two GCI commands (ABORT REQUEST and TIMEOUT) are generated. The accompanying CH. NUM. should be 10, and FLG should be set.

OPCODE—Command Opcode (GCI Mode Only)

These bits are set by the M68000 core to define the specific GCI command. See 4.7 Serial Management Controllers (SMCs) for more details.

00 = TRANSMIT ABORT REQUEST; the GCI receiver sends an abort request on the E bit.
01 = TIMEOUT Command
10 = Reserved
11 = Reserved

Bit 3—Reserved bit; should be set to zero.

CH. NUM.—Channel Number

These bits are set by the M68000 core to define the specific SCC channel that the command is to operate upon.

00 = SCC1
01 = SCC2
10 = SCC3
11 = Reserved

4.4.1 IDL Interface

The IDL interface is a full-duplex ISDN interface used to interconnect a physical layer device (such as the Motorola ISDN S/T transceiver MC145474) to the integrated multiprotocol processor (IMP). Data on five channels (B1, B2, D, A, and M) is transferred in a 20-bit frame every 125 µs, providing 160-kbps full-duplex bandwidth. The IMP is an IDL slave device that is clocked by the IDL bus master (physical layer device). The IMP provides direct connections to the MC145474. Refer to Figure 4-6 for the IDL bus signals.

The IMP supports 10-bit IDL as shown in Figure 4-6; it does not support 8-bit IDL.

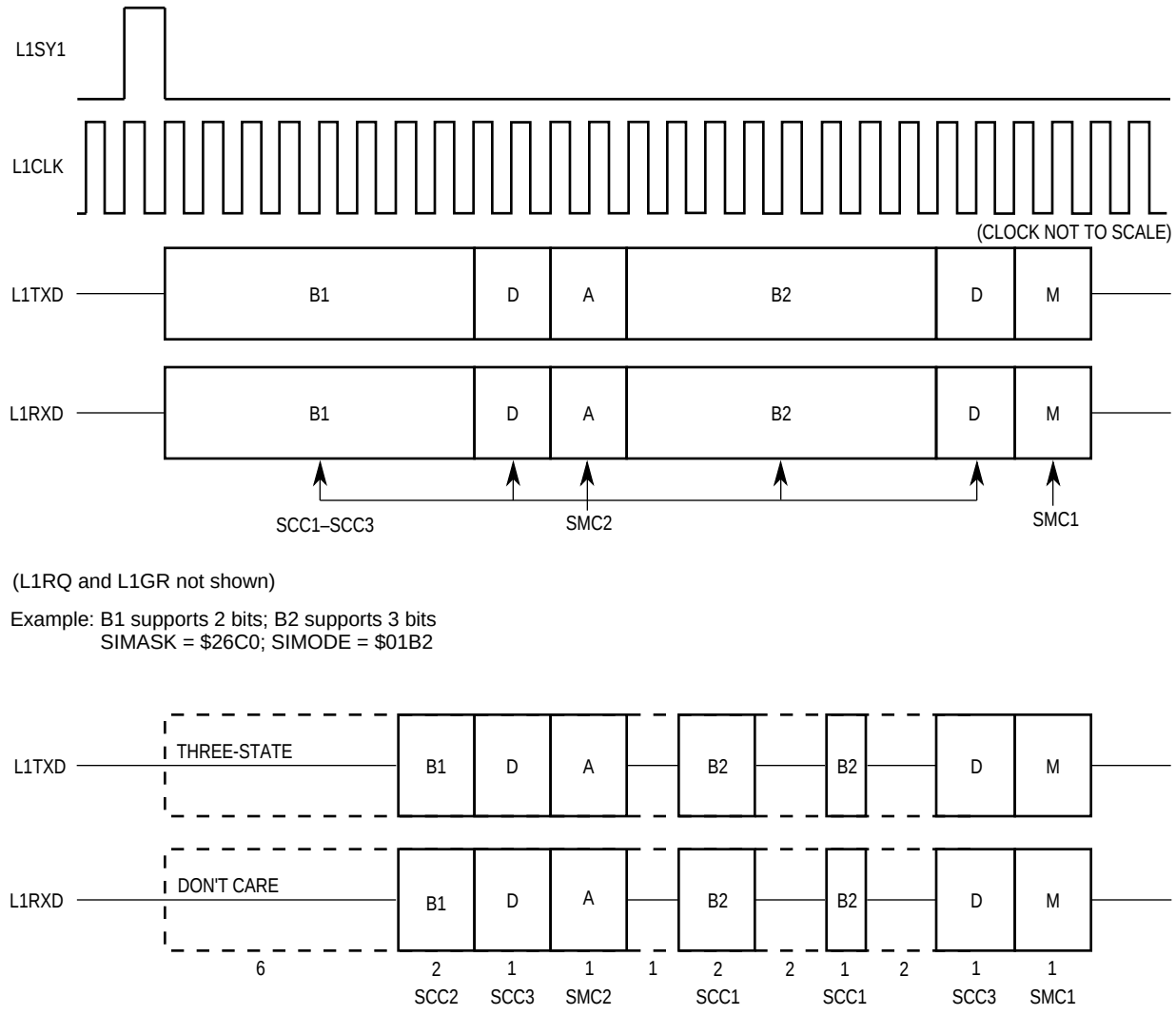


Figure 4-6. IDL Bus Signals

An application of the IDL interface is to build a basic rate ISDN terminal adaptor (see Figure 4-7). In such an application, the IDL interface is used to connect the 2B + D channels between the IMP, CODEC, and S/T transceiver. One of the IMP SCCs would be configured to HDLC mode to handle the D channel; another IMP SCC would be used to rate adapt the

4.5.11.6 UART Address Recognition

In multidrop systems, more than two stations may be present on a network, with each having a specific address. Figure 4-18 shows two examples of such a configuration. Frames comprised of many characters may be broadcast, with the first character acting as a destination address. To achieve this, the UART frame is extended by one bit, called the address bit, to distinguish between an address character and the normal data characters. The UART can be configured to operate in a multidrop environment in which two modes are supported:

Automatic Multidrop Mode—The IMP automatically checks the incoming address character and accepts the data following it only if the address matches one of two 8-bit preset values. In this mode, UM1–UM0 = 11 in the UART mode register.

Nonautomatic Multidrop Mode—The IMP receives all characters. An address character is always written to a new buffer (it may be followed by data characters in the same buffer). In this mode, UM1–UM0 = 01 in the UART mode register.

Each UART controller has two 8-bit address registers (UADDR1 and UADDR2) for address recognition. In the automatic mode, the incoming address is checked against the lower order byte of the UART address registers. Upon an address match, the address match (M) bit in the BD is set/cleared to indicate which address character was matched. The data following it is written to the same data buffer.

NOTE

For 7-bit characters, the eighth bit (bit 7) in UADDR1 and UADDR2 should be zero.

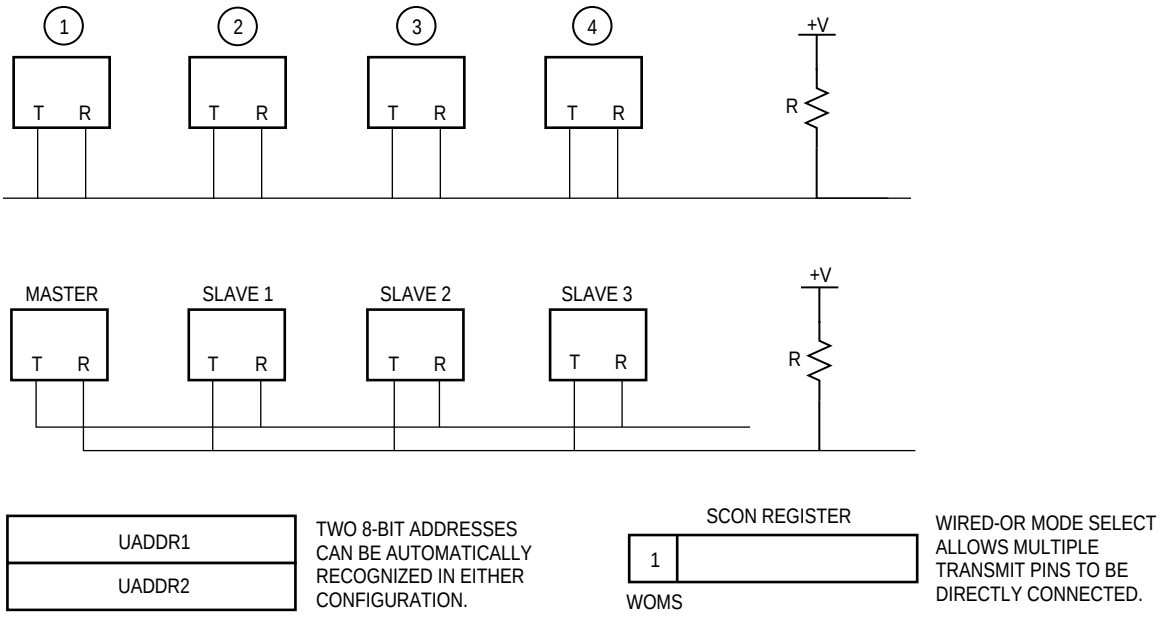


Figure 4-18. Two Configurations of UART Multidrop Operation

4.5.11.7 UART Control Characters and Flow Control

The UART has the capability to recognize special control characters. These characters may be used when the UART functions in a message-oriented environment. Up to eight control characters may be defined by the user in the control characters table. Each of these characters may be either stored (written to the receive buffer, after which the current buffer is closed and a new receive buffer taken) or rejected. If rejected, the character is written to the received control character register (RCCR) in internal RAM, and a maskable interrupt is generated. This method is useful for notifying the user of the arrival of control characters (e.g., XOFF) that are not part of the received messages.

The UART uses a table of 16-bit entries to support control-character recognition. Each entry consists of the control character, an end-of-table bit, and a reject character bit. The control characters table is shown in Figure 4-19.

NOTE

To disable all functions of the control characters and flow control table, initialize CHARACTER1 to $8000 and CHARACTER8 to $0000.

RCCR—Received Control Character Register

Upon a control character match for which the reject bit is set, the UART will write the control character into the RCCR and generate a maskable interrupt. The M68000 core must process the interrupt and read the RCCR before a second control character arrives. Failure to do so will result in the UART overwriting the first control character.

	15	14	13	12	11	10	9	8	7 … 0
OFFSET + 0									RCCR
OFFSET + 2	E	R							CHARACTER1
OFFSET + 4	E	R							CHARACTER2
OFFSET + 6	E	R							CHARACTER3
•									
•									
•									
OFFSET + 10	E	R	REA	I	CT	0	0	A	CHARACTER8

Figure 4-19. UART Control Characters Table

CHARACTER7–CHARACTER1—Control Character Value

These fields define control characters that should be compared to the incoming character. For 7-bit characters, the eighth bit (bit 7) should be zero.

BRK—Break Character Received

A break character was received.

CCR—Control Character Received

A control character was received (with reject (R) character = 1) and stored in the receive control character register (RCCR).

BSY—Busy Condition

A character was received and discarded due to lack of buffers. The receiver automatically enters hunt mode immediately if in the multidrop mode. The latest that an Rx BD can be made empty (have its empty bit set) and still avoid the busy condition is the middle of the stop bit of the first character to be stored in that buffer.

TX—Tx Buffer

A buffer has been transmitted over the UART channel. If CR = 1 in the Tx BD, this bit is set no sooner than when the last data bit of the last character in the buffer begins to be transmitted. If CR = 0, this bit is set after the last character was written to the transmit FIFO.

RX—Rx Buffer

A buffer has been received over the UART channel. This event occurs no sooner than the middle of the first stop bit of the character that causes the buffer to be closed.

4.5.11.17 UART MASK Register

The SCC mask register (SCCM) is referred to as the UART mask register when the SCC is operating as a UART. It is an 8-bit read-write register with the same bit formats as the UART event register. If a bit in the UART mask register is a one, the corresponding interrupt in the event register will be enabled. If the bit is zero, the corresponding interrupt in the event register will be masked. This register is cleared upon reset.

4.5.11.18 S-Records Programming Example

In the following paragraphs, an example of a downloading application is given that utilizes an SCC channel as a UART controller. The application performs downloads and uploads of S records between a host computer and an intelligent peripheral through a serial asynchronous line.

The S records are strings of ASCII characters that begin with `S' and end in an end-of-line character. This characteristic will be used to impose a message structure on the communication between the devices. Note that each device may also transmit XON and XOFF characters for flow control, which do not form part of the program being uploaded or downloaded.

The UART mode register should be set as required, with the freeze (FRZ) bit cleared and the enable transmitter/receiver (ENT, ENR) bits set. Receive buffers should be linked to the receive buffer table with the interrupt (I) bit set. For simplicity, assume that the line is not multidrop (no addresses are transmitted) and that each S record will fit into a single data buffer.

CR—Rx CRC Error

This frame contains a CRC error.

OV—Overrun

A receiver overrun occurred during frame reception.

CD—Carrier Detect Lost

The carrier detect signal was negated during frame reception. This bit is valid only when working in NMSI mode.

Data Length

The data length is the number of octets written to this BD's data buffer by the HDLC controller. It is written by the CP once as the BD is closed.

When this BD is the last BD in the frame (L = 1), the data length contains the total number of frame octets (including any previous linked receive data buffers and two or four bytes for the CRC) in the frame. This behavior is useful for determining the total number of octets received, even if MFLR was exceeded.

NOTE

The actual amount of memory allocated for this buffer should be even and greater than or equal to the contents of maximum receive buffer length register (MRBLR).

Rx Buffer Pointer

The receive buffer pointer, which always points to the first location of the associated data buffer, may reside in either internal or external memory.

NOTE

The Rx buffer pointer must be even, and the upper 8 bits must of the pointer must be zero for the function codes to operate correctly.

4.5.12.11 HDLC Transmit Buffer Descriptor (Tx BD)

Data is presented to the HDLC controller for transmission on an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The HDLC controller confirms transmission (or indicates error conditions) using the BDs to inform the M68000 core that the buffers have been serviced. The Tx BD is shown in Figure 4-28.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	L	TC	—	—	—	—	—	—	—	—	UN	CT
OFFSET + 2	DATA LENGTHTX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET + 4																
OFFSET + 6																

Figure 4-28. HDLC Transmit Buffer Descriptor

DSOH—DDCMP SOH Register

The 8-bit DSOH register is used to synchronize data messages by the DDCMP controller. When the DDCMP controller is not in hunt mode (byte synchronization is now established), it searches for the SOH character to start processing data messages. The DDCMP controller transfers the header and the data fields of the message to the buffer, checks the header and data CRCs, counts the data field up to the value contained in the header byte count field, and compares the header address field against the user-defined addresses. The DSOH register is a memory-mapped read-write register.

DENQ—DDCMP ENQ Register

The 8-bit DENQ register is used to synchronize control messages by the DDCMP controller. When the DDCMP controller is not in hunt mode (byte synchronization is established), it searches for the ENQ character to start processing control messages. The DDCMP controller transfers the message to the buffer, checks the CRC, and compares the message address field against the user-defined addresses. The DENQ register is a memory-mapped read-write register.

DDLE—DDCMP DLE Register

The 8-bit DDLE register is used to synchronize maintenance messages by the DDCMP controller. When the DDCMP controller is not in hunt mode (byte synchronization is established), it searches for the DLE character to start processing the maintenance messages. The DDCMP controller transfers the header and the data fields of the message to the buffer, checks the header and data CRCs, counts the data field up to the value contained in the header byte count field, and compares the header address field against the user-defined addresses. The DDLE register is a memory-mapped read-write register.

4.5.14.7 DDCMP Address Recognition.

Each DDCMP controller has five 16-bit registers to support address recognition: one mask register and four address registers (DMASK, DADDR1, DADDR2, DADDR3, and DADDR4). The DDCMP controller reads the message address from the receiver, masks it with the user-defined DMASK bits, and then checks the result against the four address register values. A one in DMASK indicates a bit position where a comparison should take place; a zero masks the comparison. For 8-bit address comparison, the high byte of DMASK should be zero.

4.5.14.8 DDCMP Error-Handling Procedure

The DDCMP controller reports message reception and transmission errors using the channel BDs, the error counters, and the DDCMP event register. The modem interface lines can also be directly monitored with the SCC status register.

Transmission errors:

1. Transmitter Underrun. When this error occurs, the channel terminates buffer transmission, closes the buffer, sets the underrun (UN) bit in the BD, and generates the transmit error (TXE) interrupt (if enabled). The channel will resume transmission after the reception of the RESTART TRANSMIT command. The FIFO size is three bytes.

following message reception. Bit 15 determines whether the M68000 core or the CP may currently access the BD.

E—Empty

0 = The data buffer associated with this BD has been filled with received data, or data reception has been aborted due to an error condition. The M6800 core is free to examine or write to any fields of the BD.

1 = The data buffer associated with this BD is empty. This bit signifies that the BD and its associated buffer are available to the DDCMP controller. The M68000 core should not write to any fields of this BD after it sets this bit. Note that the empty bit will remain set while the DDCMP controller is currently filling the buffer with received data.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.

1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Rx BD table.

1 = This is the last BD in the Rx BD table. After this buffer has been used, the DDCMP controller places incoming data into the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been closed.

1 = The RBD or RBK bits in the DDCMP event register will be set when this buffer has been closed by the DDCMP controller, which can cause interrupts.

The following status bits are written by the DDCMP controller after it has finished receiving data in the associated data buffer.

L—Last in Message

0 = The buffer is not the last in a message.

1 = The buffer is the last in a message.

H—Header in Buffer

0 = The buffer does not contain a message header.

1 = The buffer contains a message header.

NOTE

To correctly identify buffers containing headers, the buffer size should be eight or more bytes in length so that the header will fit in a single buffer.

Rx Buffer Pointer

This pointer contains the address of the associated data buffer and may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.14.11 DDCMP Transmit Buffer Descriptor (Tx BD)

Data is presented to the CP for transmission over an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The CP confirms transmission (or indicates error conditions) using the BDs to inform the M68000 core that the buffers have been serviced. The Tx BD is shown in Figure 4-37.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	L	TC	OL	—	—	—	—	—	—	—	UN	CT
OFFSET + 2	DATA LENGTH															
OFFSET + 4	TX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-37. DDCMP Transmit Buffer Descriptor

The first word contains status and control bits. Bits 15–9 are prepared by the user before transmission. Bits 1–0 are set by the DDCMP controller after the buffer has been transmitted. Bit 15 is set by the user when the buffer and BD have been prepared and is cleared by the DDCMP controller when the message is transmitted.

R—Ready

0 = This buffer is not currently ready for transmission. The user is free to manipulate this BD (or its associated buffer). The DDCMP controller clears this bit after the buffer has been completely transmitted (or after an error condition is encountered).
1 = The data buffer has been prepared for transmission by the user (but not yet transmitted). No fields of this BD may be written by the user once this bit is set.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Tx BD table.
1 = This is the last BD in the Tx BD table. After this buffer has been used, the DDCMP controller will transmit data from the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

4.5.15.1 Bit Rate Adaption of Synchronous Data Signaling Rates up to 19.2 kbps

The V.110 synchronous bit rate adaption block diagram within the terminal adaptor is shown in Figure 4-38.

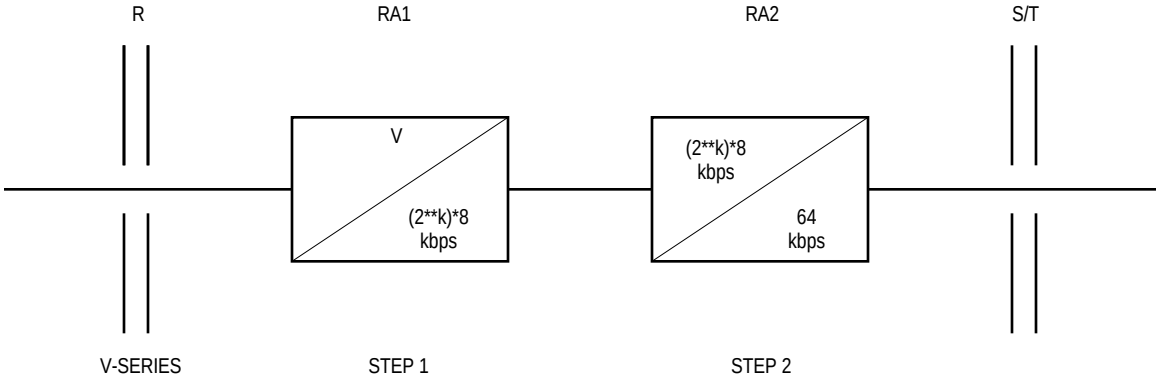


Figure 4-38. Two-Step Synchronous Bit Rate Adaption

This function may be implemented with two SCCs, one of which is configured for V.110 operation. Step 1 (RA1) rate adaption can be achieved using one SCC channel programmed to promiscuous (totally transparent) mode (see 4.5.13 BISYNC Controller). This SCC will transfer the data between the R interface and IMP memory. The M68000 core must be programmed to format the data in memory according to the V.110 protocol to create the V.110 80-bit frame. Another SCC is used to transfer the data between IMP memory and the S/T interface. This SCC should be programmed for V.110 operation, which provides the conversion of the data rate to 64 kbps. Data may be transmitted and received on 1, 2, or 4 bits of an ISDN B channel as programmed in the SIMASK register.

NOTE

V.110 contains a requirement (under further study) for control information on the R interface (i.e., RTS, CTS, CD, DTR, and DSR), conveyed by the S bits in the V.110 frame, not to have a different transmission delay than the user data conveyed by the D8–D1 bits. This very time-critical aspect of the standard is not supported by the IMP. In this case, provision would need to be made by the user to guarantee correct sampling times for this information to correspond with the user data. The IMP, however, can detect changes in these signals and issue appropriate interrupts to the M68000 core, allowing the function to be fully implemented in a slightly longer time period.

4.5.15.2 Rate Adaption of 48- and 56-kbps User Rates to 64 kbps

This function may again be implemented with two SCCs; however, in this case, the SCC connected to the B channel is programmed to promiscuous (totally transparent) mode rather than for V.110 operation (see 4.5.9 SCC Transparent Mode). The M68000 core will need to format the framing pattern in the 48-kbps conversion case. For the 56-kbps rate conversion, however, the B channel mask (SIMASK) in the serial channel physical interface can be used.

by the M68000 core before setting the STR bit so that received replies may be easily recognized by the software.

4.7 SERIAL MANAGEMENT CONTROLLERS (SMCS)

The SMC key features are as follows:

- Two Modes of Operation:
  - —IDL—SMC1 supports the maintenance channel and SMC2 supports the auxiliary channel
  - —GCI (IOM-2)—SMC1 supports the monitor channel and SMC2 supports the C/I channel
- Full-Duplex Operation
- Local Loopback Capability for Testing

4.7.1 Overview

The SMCs are two synchronous, full-duplex serial management control (SMC) ports. The SMC ports may be configured to operate in either Motorola interchip digital link (IDL) or general circuit interface (GCI) modes. GCI is also known as ISDN oriented modular 2 (IOM-2). See 4.4 Serial Channels Physical Interface for the details of configuring the IDL and GCI interfaces. The SMC ports are not used when the physical serial interface is configured for PCM highway or NMSI modes.

4.7.1.1 Using IDL with the SMCs

In this mode, SMC1 transfers the maintenance (M) bits of the IDL to and from the internal RAM, and SMC2 transfers the auxiliary (A) bits to and from the internal RAM. The CP generates a maskable interrupt upon reception/transmission of eight bits. The SMC1 and SMC2 receivers can be programmed to work in hunt-on-zero mode, in which the receiver will search the line signals for a zero bit. When it is found, the receiver will transfer data to the internal RAM.

4.7.1.2 Using GCI with the SMCs

In this mode, SMC1 controls the GCI monitor channel.

SMC1 Transmission

The monitor channel is used to transfer commands to the layer-1 component. The M68000 core writes the data byte into the SMC1 Tx BD. SMC1 will transmit the data on the monitor channel.

The SMC1 channel transmitter can be programmed to work in one of two modes:

Transparent Mode

In this mode, SMC1 transmits the monitor channel data and the A and E control bits transparently into the channel. When the M68000 core has not written new data to the buffer, the SMC1 transmitter will retransmit the previous monitor channel data and the A and E control bits.

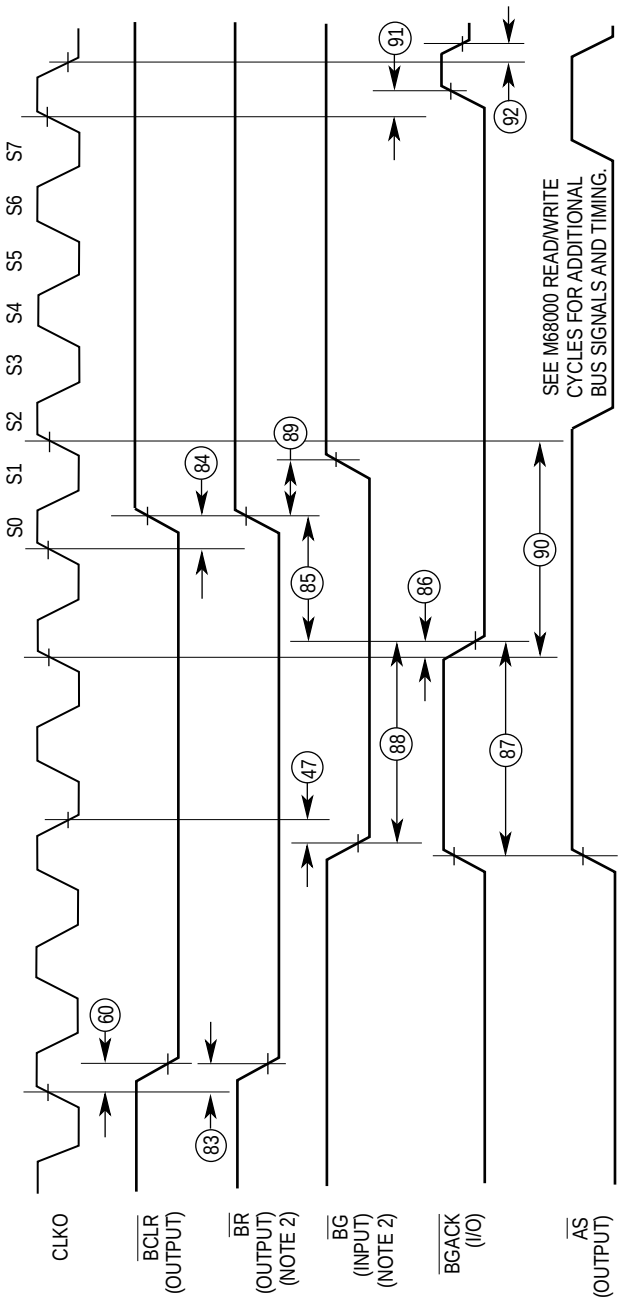


Figure 6-7. DMA Timing Diagram (SDMA)

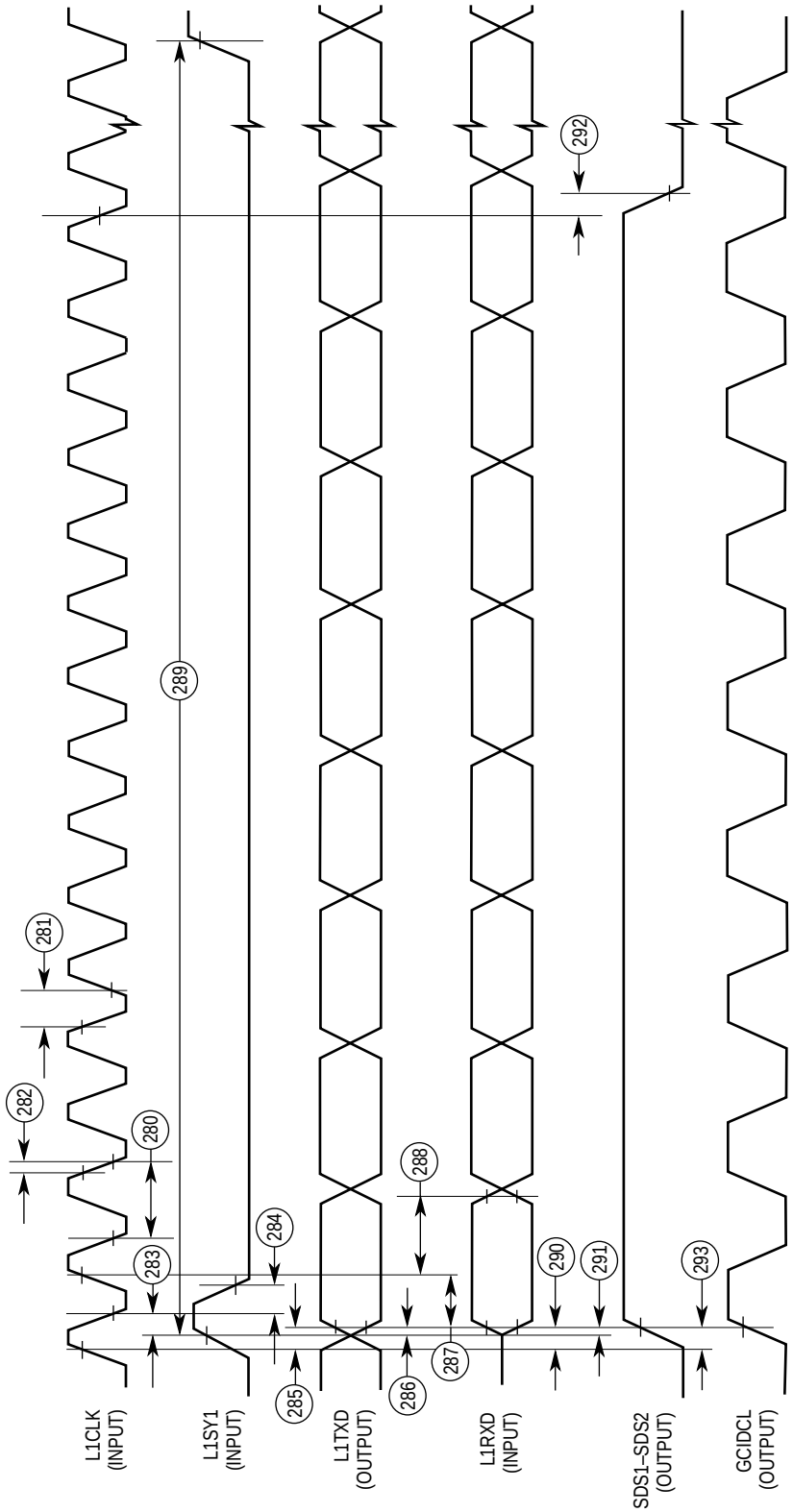


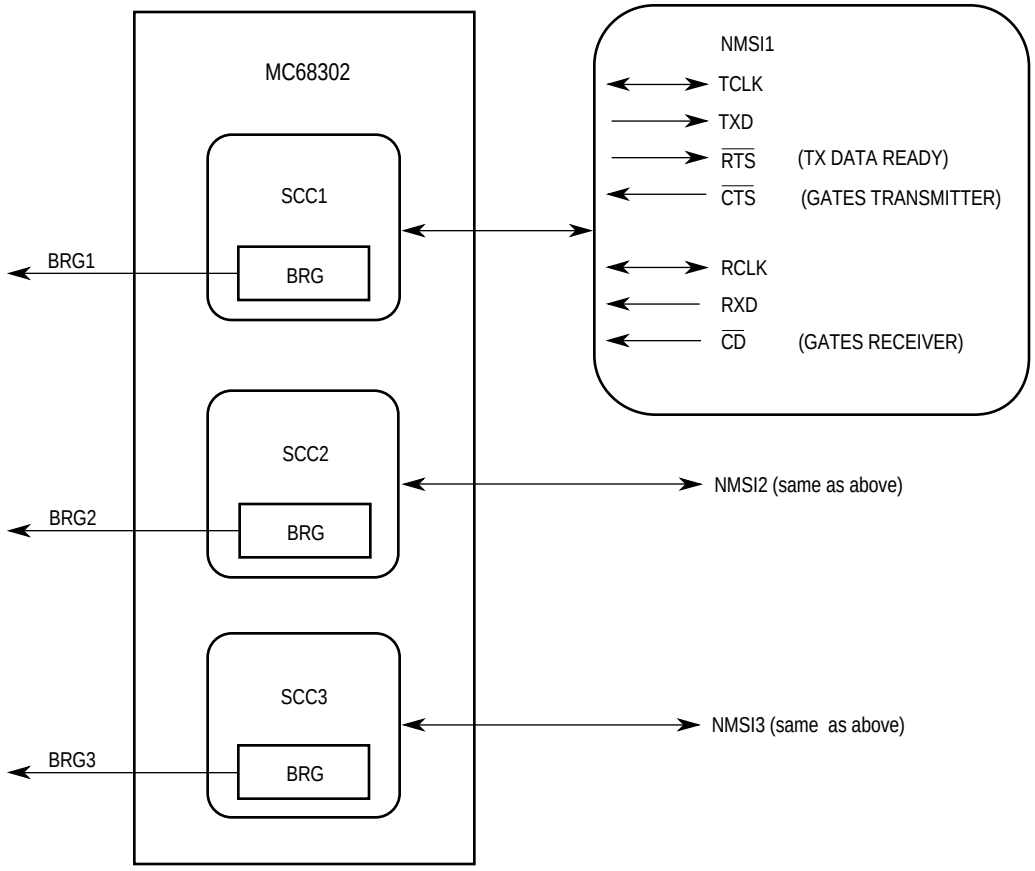
Figure 6-21. GCI Timing Diagram

```
IMR         EQU       BASE +  $816      ;Interrupt Mask Register
ISR         EQU       BASE +  $818      ;In-Service Register
SIMODE      EQU       BASE +  $8B4      ;Serial Interface Mode Register
SCON1       EQU       BASE +  $882      ;SCC1 Configuration Register
SCM1        EQU       BASE +  $884      ;SCC1 Mode Register
SCCE1       EQU       BASE +  $888      ;SCC1 Event Register
SCCM 1      EQU       BASE +  $88A      ;SCC1 Mask Register
EN_SCC      EQU       $0C               ;ENR and ENT bits in SCM

***SCC1 Parameter Table ***
ST_BD       EQU       0                 ;Status and Control in BD
SS_BD       EQU       1                 ;Status in BD
LN_BD       EQU       2                 ;Data Length in BD
PT_BD       EQU       4                 ;Buffer pointer in BD
SZ_BD       EQU       $08               ;Size of BD = 8 bytes
FCR_1       EQU       BASE+$0480        ;RFCR and TFCR for SCC1
MRBLR_1     EQU       BASE+$0482        ;Max Rx Buffer Length
RXBD_01     EQU       BASE+$0400        ;RX BD 0 in SCC1
TXBD_01     EQU       BASE+$0440        ;TX BD 0 in SCC1
READY       EQU       $07               ;Ready bit in the 1st byte of TX BD
EMPTY       EQU       $07               ;Empty bit in the 1st byte of RX BD
WRAP        EQU       $05               ;Wrap bit in the 1st byte of BD
* The following values are application dependent for this example
RXBF_01     EQU       $030000           ;Address of the first RX buffer
TXBF_01     EQU       $030080           ;Address of the first TX buffer
BD_CNT      EQU       $08               ;Number of BDs used
SZ_BF       EQU       $10               ;Size of buffer =16 bytes
N_DATA      EQU       6                 ;Number of data to be sent in a buffer
* SCC1 HDLC Parameters
CMSKL_1     EQU       BASE+$04A0        ;CRC Mask Low
CMSKH_1     EQU       BASE+$04A2        ;CRC Mask High
DISFC_1     EQU       BASE+$04A8        ;Discard Frame Counter
CRCEC_1     EQU       BASE+$04AA        ;CRC Error Counter
ABTSC_1     EQU       BASE+$04AC        ;Abort Sequence Counter
NMARC _ 1   EQU       BASE+$04AE        ;Nonmatching Address Receive Counter
RETRC_1     EQU       BASE+$04B0        ;Frame Retransmission Counter
MFLR_1      EQU       BASE+$04B2        ;Max Frame Length Register
HMASK 1     EQU       BASE+$04B6        ;User-Defined Frame Address Mask

********************** Typical M68302 Initialization Code********************
* Register Initialized values in ADS board before execution
* USP = 00080000 ISP = 000040000 (Stack pointer not used)
            ORG       INIT              ;PC = 00030300
            MOVE.W    #$2700,SR         ;SR = 2700, mask off interrupts
* Set Base Address = $700000
* Now all 68302 on-chip peripherals begin at address $700xxx
            MOVE.W    #$0700,BAR        ;BAR = 0700
* Set System Control Register
            MOVE.L    #0,SCR            ;Nothing special for this example
***Setups for interrupt ***
            MOVE.W    #$0A0,GIMR        ;Normal mode, v7–v5 = 5
            MOVE.W    #0,IMR            ;Mask off all for now
            MOVE.W    #$FFFF,IPR        ;Clear IPR

*** Set up Serial Interface Connection ***
```



NMSI — Nonmultiplexed serial interface (also called the modem I/F).

Figure D-21. NMSI Pin Definitions

The other three physical interfaces, PCM highway, IDL, and GCI, are called multiplexed interfaces since they allow data from one, two, or all three SCCs to be time multiplexed together on the same pins. If a multiplexed interface is chosen, the first SCC to use that interface must be SCC1, since the three multiplexed modes share pins with SCC1 (see Figure D-22). After choosing a multiplexed mode, you can decide independently whether SCC2 and SCC3 should be part of the multiplexed interface or whether they should have their own set of NMSI pins.

If you are working in ISDN, transparent mode can be quite useful in sending and receiving transparent data over the 2B + D interface. IDL and GCI allow the SCCs to transmit and receive data on the two 64 kbps B channels and on the one 16 kbps D channel in basic rate ISDN. If you are not interfacing to a 2B + D ISDN environment, you can probably rule out using IDL and GCI.

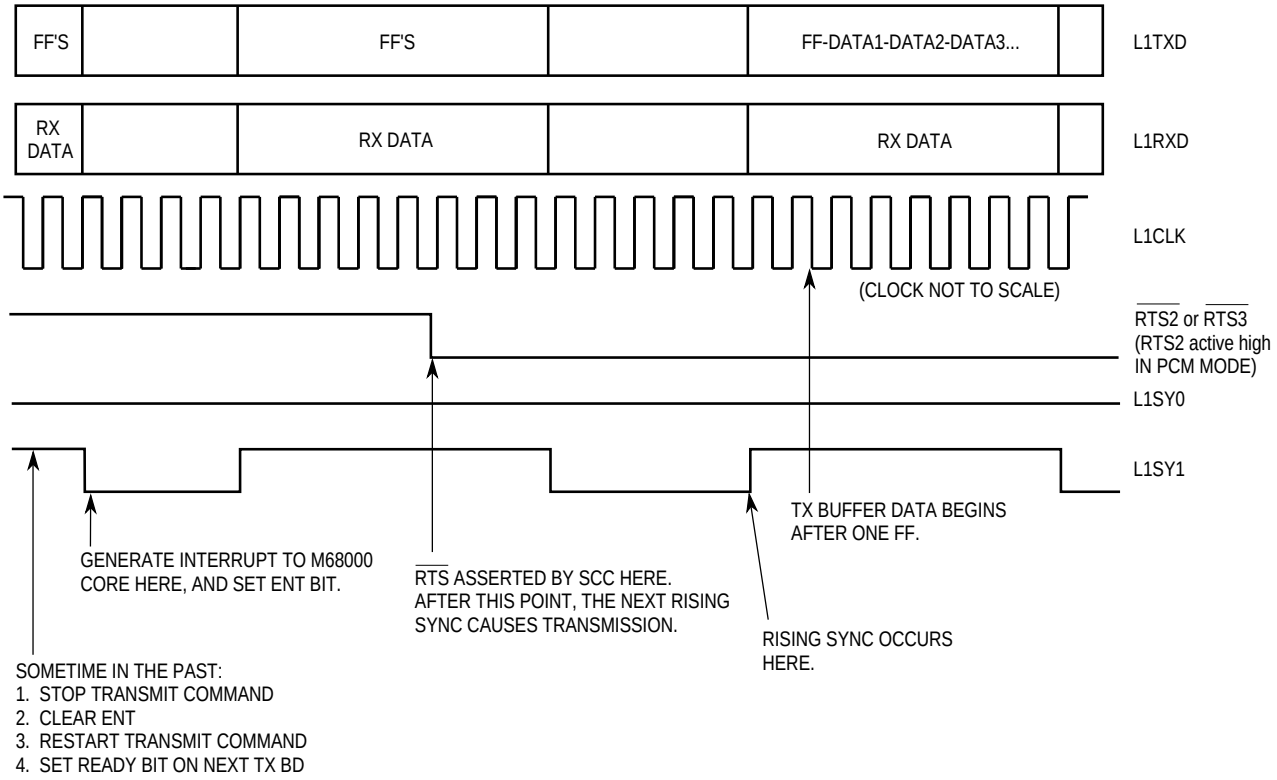


Figure D-30. PCM Transmission Timing Technique

A synchronized setting of the ENT bit causes the transmit FIFO to be filled in a fixed time if the following two conditions are true: 1) the SDMA is the highest priority bus master in the system (i.e., there is no external bus master during this period) and 2) the SCC needed for the transmission is the only SCC currently being used. Both of these factors become negligible if the serial clock rate is much slower than the system clock rate (e.g., a 1 to 50 ratio). (A slow serial clock rate means that deviations are much less than a serial bit time and have no effect on transmission delay.)

The preceding example showed ENT being set before the time slot. If there are more than 36 serial clocks following the setting of the ENT bit, it is possible to set the ENT bit during the time slot and see the same behavior. The assertion of the $\overline{\text{RTS}}$ signal can be used to verify that a sufficient number of clocks occurred after the setting of ENT.

In the transparent operation, assertion of $\overline{\text{RTS1}}$ is slightly different from that of $\overline{\text{RTS2}}$ and $\overline{\text{RTS3}}$. The description of $\overline{\text{RTS}}$ in Table D-4, the text on D-73, Figure D-29, and the text on D-74 is correct for $\overline{\text{RTS2}}$ and $\overline{\text{RTS3}}$, but not exactly correct for $\overline{\text{RTS1}}$. $\overline{\text{RTS1}}$ has the opposite polarity in PCM mode. $\overline{\text{RTS1}}$ goes low when SIMODE is programmed as the PCM mode, and then goes high when the SCC is about ready to transmit.

If the time slots are not long enough to guarantee transmission after the second time slot, then the synchronized setting of the ENT bit should at least guarantee a fixed delay to the start of data. In this case, there will be additional time slots with $FF data until the data1 byte is transmitted.

CR—Rx CRC Error

0 = This frame does not contain a CRC error.
1 = This frame contains a CRC error.

OV—Overrun

0 = No receiver overrun occurred.
1 = A receiver overrun condition occurred during frame reception.

CD—Carrier Detect Lost (valid only in NMSI mode)

0 = No CD lost was detected.
1 = CD was negated during frame reception.

E.1.1.4.2 Receive Buffer Data Length. This 16-bit value is written by the IMP to indicate the number of data bytes received into the data buffer.

E.1.1.4.3 Receive Buffer Pointer. This 32-bit value is written by the user to indicate the address where the data is to be stored.

E.1.1.5 TRANSMIT BUFFER DESCRIPTORS. Each SCC has eight transmit buffer descriptors. Each buffer descriptor consists of four words as shown below. Reserved bits in registers should be written as zeros.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	L	TC	—	—	—	—	—	—	—	—	UN	CT
OFFSET +2	DATA LENGTH															
OFFSET +4	TX BUFFER POINTER															
OFFSET +6																

E.1.1.5.1 Transmit BD Control/Status Word. To initialize the buffer, the user should write bits 15-10 and bits 1-0. The IMP clears bit 15 when the buffer is transmitted or closed due to an error and sets bits 1-0 depending on which error occurred.

R—Ready

0 = This data buffer is not currently ready for transmission.
1 = This data buffer has been prepared by the user for transmission but has not yet been fully transmitted. Must be set by the user to enable transmission of the buffer.

X—External Buffer

0 = The data buffer associated with this BD is in internal dual-port RAM.
1 = The data buffer associated with this BD is in external memory.

W—Wrap (final BD in table)

0 = This is not the last BD in the transmit BD table.
1 = This is the last BD in the transmit BD table.