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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	62
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8346mfve

Also shown in **Figure 1-2** are connections between the PWM, Timer C and ADC blocks. These connections allow the PWM and/or Timer C to control the timing of the start of ADC conversions. The Timer C channel indicated can generate periodic start (SYNC) signals to the ADC to start its conversions. In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C input channel as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC. To fully understand this interaction, please see the **56F8300 Peripheral User Manual** for clarification on the operation of all three of these peripherals.

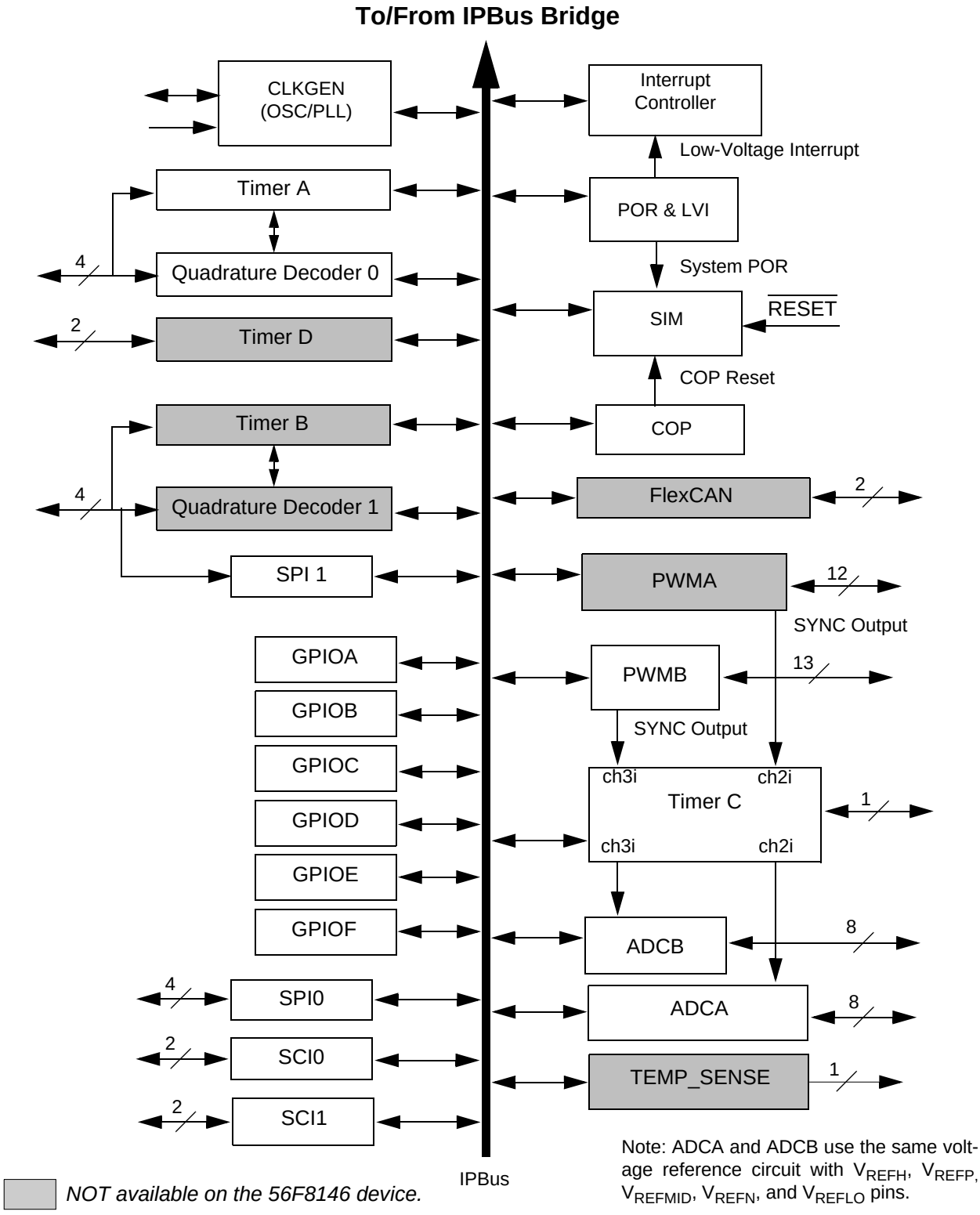


Figure 1-2 Peripheral Subsystem

Table 2-2 Signal and Package Information for the 144 Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
OCR_DIS	79	Input	Input	**On-Chip Regulator Disable** — Tie this pin to V_{SS} to enable the on-chip regulator Tie this pin to V_{DD} to disable the on-chip regulator **This pin is intended to be a static DC signal from power-up to shut down. Do not try to toggle this pin for power savings during operation.**
$V_{CAP}1$	51	Supply	Supply	**$V_{CAP}1$ - 4** — When OCR_DIS is tied to V_{SS} (regulator enabled), connect each pin to a 2.2µF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation. When OCR_DIS is tied to V_{DD} (regulator disabled), these pins become V_{DD_CORE} and should be connected to a regulated 2.5V power supply. **Note: This bypass is required even if the chip is powered with an external supply.**
$V_{CAP}2$	128			
$V_{CAP}3$	83			
$V_{CAP}4$	15			
$V_{PP}1$	125	Input	Input	**$V_{PP}1$ - 2** — These pins should be left unconnected as an open circuit for normal functionality.
$V_{PP}2$	2			
CLKMODE	87	Input	Input	**Clock Input Mode Selection** — This input determines the function of the XTAL and EXTAL pins. 1 = External clock input on XTAL is used to directly drive the input clock of the chip. The EXTAL pin should be grounded. 0 = A crystal or ceramic resonator should be connected between XTAL and EXTAL.
EXTAL	82	Input	Input	**External Crystal Oscillator Input** — This input can be connected to an 8MHz external crystal. Tie this pin low if XTAL is driven by an external clock source.
XTAL	81	Input/ Output	Chip-driven	**Crystal Oscillator Output** — This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL must be used as the input and EXTAL connected to GND. The input clock can be selected to provide the clock directly to the core. This input clock can also be selected as the input clock for the on-chip PLL.

Table 2-2 Signal and Package Information for the 144 Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
PHASEB1	7	Schmitt Input	Input, pull-up enabled	**Phase B1** — Quadrature Decoder 1, PHASEB input for decoder 1.
(TB1)		Schmitt Input/ Output		**TB1** — Timer B, Channel 1
(MOSI1)		Schmitt Input/ Output		**SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. To activate the SPI function, set the PHSB_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**.
(GPIOC1)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8346, the default state after reset is PHASEB1. In the 56F8146, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOC_PUR register.

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8346	56F8146	Use Restrictions
Data RAM	8KB	8KB	None
Program Boot Flash	8KB	8KB	Erase / Program via Flash Interface unit and word to CDBW

4.2 Program Map

The operating mode control bits (MA and MB) in the Operating Mode Register (OMR) control the Program memory map. At reset, these bits are set as indicated in **Table 4-2**. **Table 4-4** shows the memory map configurations that are possible at reset. After reset, the OMR MA bit can be changed and will have an effect on the P-space memory map, as shown in **Table 4-3**. Changing the OMR MB bit will have no effect.

Table 4-2 OMR MB/MA Value at Reset

OMR MB = Flash Secured State[1, 2]	OMR MA = EXTBOOT Pin	Chip Operating Mode
0	0	Mode 0 – Internal Boot; EMI is configured to use 16 address lines; Flash Memory is secured; external P-space is not allowed; the EOnCE is disabled
0	1	Not valid; cannot boot externally if the Flash is secured and will actually configure to 00 state
1	0	Mode 0 – Internal Boot; EMI is configured to use 16 address lines
1	1	Mode 1 – External Boot; Flash Memory is not secured; EMI configuration is determined by the state of the EMI_MODE pin

1. This bit is only configured at reset. If the Flash secured state changes, this will not be reflected in MB until the next reset.
2. Changing MB in software will not affect Flash memory security.

Table 4-3 Changing OMR MA Value During Normal Operation

OMR MA	Chip Operating Mode
0	Use internal P-space memory map configuration
1	Use external P-space memory map configuration – If MB = 0 at reset, changing this bit has no effect.

The device's external memory interface (EMI) can operate much like the 56F80x family's EMI, or it can be operated in a mode similar to that used on other products in the 56800E family. Initially, $\overline{CS0}$ and $\overline{CS1}$ are configured as $\overline{PS}$ and $\overline{DS}$, in a mode compatible with earlier 56800 devices.

Eighteen address lines are required to shadow the first 192K of internal program space when booting externally for development purposes. Therefore, the entire complement of on-chip memory cannot be accessed using a 16-bit 56800-compatible address bus. To address this situation, the EMI_MODE pin can be used to configure four GPIO pins as Address[19:16] upon reset (only one of these pins [A16] is usable

Table 4-13 Quad Timer C Registers Address Map (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC0_CMP1	$0	Compare Register 1
TMRC0_CMP2	$1	Compare Register 2
TMRC0_CAP	$2	Capture Register
TMRC0_LOAD	$3	Load Register
TMRC0_HOLD	$4	Hold Register
TMRC0_CNTR	$5	Counter Register
TMRC0_CTRL	$6	Control Register
TMRC0_SCR	$7	Status and Control Register
TMRC0_CMPLD1	$8	Comparator Load Register 1
TMRC0_CMPLD2	$9	Comparator Load Register 2
TMRC0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRC1_CMP1	$10	Compare Register 1
TMRC1_CMP2	$11	Compare Register 2
TMRC1_CAP	$12	Capture Register
TMRC1_LOAD	$13	Load Register
TMRC1_HOLD	$14	Hold Register
TMRC1_CNTR	$15	Counter Register
TMRC1_CTRL	$16	Control Register
TMRC1_SCR	$17	Status and Control Register
TMRC1_CMPLD1	$18	Comparator Load Register 1
TMRC1_CMPLD2	$19	Comparator Load Register 2
TMRC1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRC2_CMP1	$20	Compare Register 1
TMRC2_CMP2	$21	Compare Register 2
TMRC2_CAP	$22	Capture Register
TMRC2_LOAD	$23	Load Register
TMRC2_HOLD	$24	Hold Register
TMRC2_CNTR	$25	Counter Register
TMRC2_CTRL	$26	Control Register

Table 4-14 Quad Timer D Registers Address Map (Continued)
(TMRD_BASE = $00 F100)
Quad Timer D is NOT available in the 56F8146 device

Register Acronym	Address Offset	Register Description
TMRD3_CTRL	$36	Control Register
TMRD3_SCR	$37	Status and Control Register
TMRD3_CMPLD1	$38	Comparator Load Register 1
TMRD3_CMPLD2	$39	Comparator Load Register 2
TMRD3_COMSCR	$3A	Comparator Status and Control Register

Table 4-15 Pulse Width Modulator A Registers Address Map
(PWMA_BASE = $00 F140)
PWMA is NOT available in the 56F8146 device

Register Acronym	Address Offset	Register Description
PWMA_PMCTL	$0	Control Register
PWMA_PMFCTL	$1	Fault Control Register
PWMA_PMFSA	$2	Fault Status Acknowledge Register
PWMA_PMOUT	$3	Output Control Register
PWMA_PMCNT	$4	Counter Register
PWMA_PWMCM	$5	Counter Modulo Register
PWMA_PWMVAL0	$6	Value Register 0
PWMA_PWMVAL1	$7	Value Register 1
PWMA_PWMVAL2	$8	Value Register 2
PWMA_PWMVAL3	$9	Value Register 3
PWMA_PWMVAL4	$A	Value Register 4
PWMA_PWMVAL5	$B	Value Register 5
PWMA_PMDEADTM	$C	Dead Time Register
PWMA_PMDISMAP1	$D	Disable Mapping Register 1
PWMA_PMDISMAP2	$E	Disable Mapping Register 2
PWMA_PMCFG	$F	Configure Register
PWMA_PMCCR	$10	Channel Control Register
PWMA_PMPORT	$11	Port Register
PWMA_PMICCR	$12	PWM Internal Correction Control Register

Table 4-17 Quadrature Decoder 0 Registers Address Map (Continued) (DEC0_BASE = $00 F180)

Register Acronym	Address Offset	Register Description
DEC0_REV	$5	Revolution Counter Register
DEC0_REVH	$6	Revolution Hold Register
DEC0_UPOS	$7	Upper Position Counter Register
DEC0_LPOS	$8	Lower Position Counter Register
DEC0_UPOSH	$9	Upper Position Hold Register
DEC0_LPOSH	$A	Lower Position Hold Register
DEC0_UIR	$B	Upper Initialization Register
DEC0_LIR	$C	Lower Initialization Register
DEC0_IMR	$D	Input Monitor Register

Table 4-18 Quadrature Decoder 1 Registers Address Map (DEC1_BASE = $00 F190)
Quadrature Decoder 1 is NOT available on the 56F8146 device

Register Acronym	Address Offset	Register Description
DEC1_DECCR	$0	Decoder Control Register
DEC1_FIR	$1	Filter Interval Register
DEC1_WTR	$2	Watchdog Time-out Register
DEC1_POSD	$3	Position Difference Counter Register
DEC1_POSDH	$4	Position Difference Counter Hold Register
DEC1_REV	$5	Revolution Counter Register
DEC1_REVH	$6	Revolution Hold Register
DEC1_UPOS	$7	Upper Position Counter Register
DEC1_LPOS	$8	Lower Position Counter Register
DEC1_UPOSH	$9	Upper Position Hold Register
DEC1_LPOSH	$A	Lower Position Hold Register
DEC1_UIR	$B	Upper Initialization Register
DEC1_LIR	$C	Lower Initialization Register
DEC1_IMR	$D	Input Monitor Register

5.6.13 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-15 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

5.6.13.1 Fast Interrupt 0 Vector Address Low (FIVAL0)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAH0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.14 Fast Interrupt 0 Vector Address High Register (FIVAH0)

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-16 Fast Interrupt 0 Vector Address High Register (FIVAH0)

5.6.14.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.14.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.15 Fast Interrupt 1 Match Register (FIM1)

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-17 Fast Interrupt 1 Match Register (FIM1)

5.6.15.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0, but cannot be modified by writing.

5.6.15.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 1. Fast interrupts vector directly to a service

- 1 = An interrupt is being sent to the 56800E core

5.6.30.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

5.6.30.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows the vector number (VAB[7:1]) used at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.6.30.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.30.5 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.30.6 $\overline{\text{IRQB}}$ State Pin ($\overline{\text{IRQB}}$ STATE)—Bit 3

This *read-only* bit reflects the state of the external $\overline{\text{IRQB}}$ pin.

5.6.30.7 $\overline{\text{IRQA}}$ State Pin ($\overline{\text{IRQA}}$ STATE)—Bit 2

This *read-only* bit reflects the state of the external $\overline{\text{IRQA}}$ pin.

5.6.30.8 $\overline{\text{IRQB}}$ Edge Pin ($\overline{\text{IRQB}}$ Edg)—Bit 1

This bit controls whether the external $\overline{\text{IRQB}}$ interrupt is edge- or level-sensitive. During Stop and Wait modes, it is automatically level-sensitive.

- 0 = $\overline{\text{IRQB}}$ interrupt is a low-level sensitive (default)
- 1 = $\overline{\text{IRQB}}$ interrupt is falling-edge sensitive.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-7 Least Significant Half of JTAG ID (SIM_LSH_ID)

6.5.6 SIM Pull-up Disable Register (SIM_PUDR)

Most of the pins on the chip have on-chip pull-up resistors. Pins which can operate as GPIO can have these resistors disabled via the GPIO function. Non-GPIO pins can have their pull-ups disabled by setting the appropriate bit in this register. Disabling pull-ups is done on a peripheral-by-peripheral basis (for pins not muxed with GPIO). Each bit in the register (see **Figure 6-8**) corresponds to a functional group of pins. See **Table 2-2** to identify which pins can deactivate the internal pull-up resistor.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	PWMA1	CAN	EMI_MODE	$\overline{\text{RESET}}$	IRQ	XBOOT	PWMB	PWMA0	0	CTRL	0	JTAG	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-8 SIM Pull-up Disable Register (SIM_PUDR)

6.5.6.1 Reserved—Bit 15

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.2 PWMA1—Bit 14

This bit controls the pull-up resistors on the FAULTA3 pin.

6.5.6.3 CAN—Bit 13

This bit controls the pull-up resistors on the CAN_RX pin.

6.5.6.4 EMI_MODE—Bit 12

This bit controls the pull-up resistors on the EMI_MODE pin.

6.5.6.5 $\overline{\text{RESET}}$—Bit 11

This bit controls the pull-up resistors on the $\overline{\text{RESET}}$ pin.

6.5.6.6 IRQ—Bit 10

This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ pins.

6.5.6.7 XBOOT—Bit 9

This bit controls the pull-up resistors on the EXTBOOT pin.

6.5.6.8 PWMB—Bit 8

This bit controls the pull-up resistors on the FAULTB0, FAULTB1, FAULTB2, and FAULTB3 pins.

6.5.6.9 PWMA0—Bit 7

This bit controls the pull-up resistors on the FAULTA0, FAULTA1, and FAULTA2 pins.

6.5.6.10 Reserved—Bit 6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.11 CTRL—Bit 5

This bit controls the pull-up resistors on the $\overline{WR}$ and $\overline{RD}$ pins.

6.5.6.12 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.13 JTAG—Bit 3

This bit controls the pull-up resistors on the $\overline{TRST}$, TMS and TDI pins.

6.5.6.14 Reserved—Bits 2 - 0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7 CLKO Select Register (SIM_CLKOSR)

The CLKO select register can be used to multiplex out any one of the clocks generated inside the clock generation and SIM modules. The default value is SYS_CLK. All other clocks primarily muxed out are for test purposes only, and are subject to significant unspecified latencies at high frequencies.

The upper four bits of the GPIOB register can function as GPIO, A[23:20], or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOB_PER. If GPIOB[7:4] are programmed to operate as peripheral outputs, then the choice between A[23:20] and additional clock outputs is done here in the CLKOSR. The default state is for the peripheral function of GPIOB[7:4] to be programmed as A[23:20]. This can be changed by altering A[23:20], as shown in **Figure 6-9**.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	A23	A22	A21	A20	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-9 CLKO Select Register (SIM_CLKOSR)

6.5.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.4 FlexCAN Enable (CAN)—Bit 12

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.5 Decoder 1 Enable (DEC1)—Bit 11

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.6 Decoder 0 Enable (DEC0)—Bit 10

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.7 Quad Timer D Enable (TMRD)—Bit 9

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.8 Quad Timer C Enable (TMRC)—Bit 8

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.9 Quad Timer B Enable (TMRB)—Bit 7

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.10 Quad Timer A Enable (TMRA)—Bit 6

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.10.2 Input/Output Short Address Low (ISAL[21:6])—Bit 15–0

This field represents the lower 16 address bits of the “hard coded” I/O short address.

6.6 Clock Generation Overview

The SIM uses an internal master clock from the OCCS (CLKGEN) module to produce the peripheral and system (core and memory) clocks. The maximum master clock frequency is 120MHz. Peripheral and system clocks are generated at half the master clock frequency and therefore at a maximum 60MHz. The SIM provides power modes (Stop, Wait) and clock enables (SIM_PCE register, CLK_DIS, ONCE_EBL) to control which clocks are in operation. The OCCS, power modes, and clock enables provide a flexible means to manage power consumption.

Power utilization can be minimized in several ways. In the OCCS, crystal oscillator, and PLL may be shut down when not in use. When the PLL is in use, its prescaler and postscaler can be used to limit PLL and master clock frequency. Power modes permit system and/or peripheral clocks to be disabled when unused. Clock enables provide the means to disable individual clocks. Some peripherals provide further controls to disable unused subfunctions. Refer to the **Part 3 On-Chip Clock Synthesis (OCCS)**, and the **56F8300 Peripheral User Manual** for further details.

6.7 Power-Down Modes Overview

The 56F8346/56F8146 devices operate in one of three power-down modes, as shown in **Table 6-3**.

Table 6-3 Clock Operation in Power-Down Modes

Mode	Core Clocks	Peripheral Clocks	Description
Run	Active	Active	Device is fully functional
Wait	Core and memory clocks disabled	Active	Peripherals are active and can product interrupts if they have not been masked off. Interrupts will cause the core to come out of its suspended state and resume normal operation. Typically used for power-conscious applications.
Stop	System clocks continue to be generated in the SIM, but most are gated prior to reaching memory, core and peripherals.		The only possible recoveries from Stop mode are: 1. CAN traffic (1st message will be lost) 2. Non-clocked interrupts 3. COP reset 4. External reset 5. Power-on reset

All peripherals, except the COP/watchdog timer, run off the IPBus clock frequency, which is the same as the main processor frequency in this architecture. The maximum frequency of operation is SYS_CLK = 60MHz.

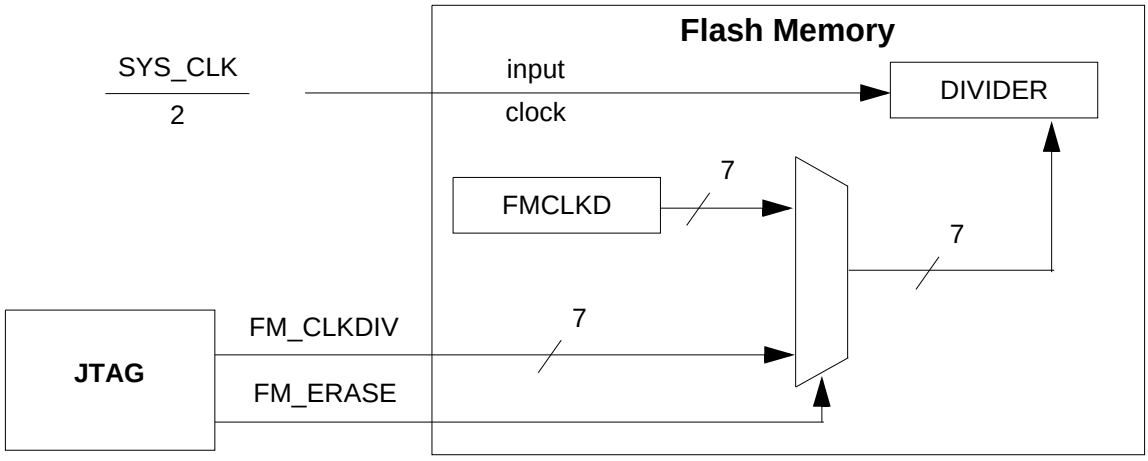


Figure 7-1 JTAG to FM Connection for Lockout Recovery

Two examples of FM_CLKDIV calculations follow.

EXAMPLE 1: If the system clock is the 8MHz crystal frequency because the PLL has not been set up, the input clock will be below 12.8MHz, so PRDIV8 = FM_CLKDIV[6] = 0. Using the following equation yields a DIV value of 19 for a clock of 200kHz, and a DIV value of 20 for a clock of 190kHz. This translates into an FM_CLKDIV[6:0] value of $13 or $14, respectively.

$$150[\text{kHz}] < \frac{\left(\frac{\text{SYS\_CLK}}{(2)}\right)}{(\text{DIV} + 1)} < 200[\text{kHz}]$$

EXAMPLE 2: In this example, the system clock has been set up with a value of 32MHz, making the FM input clock 16MHz. Because that is greater than 12.8MHz, PRDIV8 = FM_CLKDIV[6] = 1. Using the following equation yields a DIV value of 9 for a clock of 200kHz, and a DIV value of 10 for a clock of 181kHz. This translates to an FM_CLKDIV[6:0] value of $49 or $4A, respectively.

$$150[\text{kHz}] < \frac{\left(\frac{\text{SYS\_CLK}}{(2)}\right)}{(\text{DIV} + 1)} < 200[\text{kHz}]$$

Once the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, the user must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence has completed. For details, see the JTAG Section in the **56F8300 Peripheral User Manual**.

Table 8-3 GPIO External Signals Map (Continued)

Pins in shaded rows are not available in 56F8346/56F8146

Pins in italics are NOT available in the 56F8146 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin
GPIOE	0	Peripheral	TXD0	4
	1	Peripheral	RXD0	5
	2	Peripheral	A6	17
	3	Peripheral	A7	18
	4	Peripheral	SCLK0	130
	5	Peripheral	MOSI0	132
	6	Peripheral	MISO0	131
	7	Peripheral	$\overline{SS0}$	129
	8	Peripheral	TC0	118
	9	N/A		
	10	Peripheral	*TD0*	116
	11	Peripheral	*TD1*	117
	12	N/A		
	13	N/A		

See Pin Groups in **Table 10-1**

Table 10-6 Power on Reset Low Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Units
POR Trip Point	POR	1.75	1.8	1.9	V
LVI, 2.5 volt Supply, trip point[1]	$V_{EI2.5}$	—	2.14	—	V
LVI, 3.3 volt supply, trip point[2]	$V_{EI3.3}$	—	2.7	—	V
Bias Current	I_{bias}	—	110	130	µA

1. When V_{DD_CORE} drops below $V_{EI2.5}$, an interrupt is generated.
2. When V_{DD_CORE} drops below $V_{EI3.3}$, an interrupt is generated.

Table 10-7 Current Consumption per Power Supply Pin (Typical)
On-Chip Regulator Enabled (OCR_DIS = Low)

Mode	I_{DD_IO}[1]	I_{DD_ADC}	$I_{DD\_OSC\_PLL}$	Test Conditions
RUN1_MAC	155mA	50mA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • All peripherals running • Continuous MAC instructions with fetches from Data RAM • ADC powered on and clocked
Wait3	91mA	65µA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • ADC powered off
Stop1	5.8mA	0µA	155µA	• 8MHz Device Clock • All peripheral clocks are off • ADC powered off • PLL powered off
Stop2	5.1mA	0µA	145µA	• External Clock is off • All peripheral clocks are off • ADC powered off • PLL powered off

1. No Output Switching
2. Includes Processor Core current supplied by internal voltage regulator

$$R_{ES} = \frac{(V_{REFH} - V_{REFLO}) \times 1}{2^{12} \quad m}$$

3. This is the minimum time required after the PLL set up is changed to ensure reliable operation.

10.7 Crystal Oscillator Timing

Table 10-15 Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal Start-up time	T_{CS}	4	5	10	ms
Resonator Start-up time	T_{RS}	0.1	0.18	1	ms
Crystal ESR	R_{ESR}	—	—	120	ohms
Crystal Peak-to-Peak Jitter	T_D	70	—	250	ps
Crystal Min-Max Period Variation	T_{PV}	0.12	—	1.5	ns
Resonator Peak-to-Peak Jitter	T_{RJ}	—	—	300	ps
Resonator Min-Max Period Variation	T_{RP}	—	—	300	ps
Bias Current, high-drive mode	I_{BIASH}	—	250	290	µA
Bias Current, low-drive mode	I_{BIASL}	—	80	110	µA
Quiescent Current, power-down mode	I_{PD}	—	0	1	µA

10.8 External Memory Interface Timing

The External Memory Interface is designed to access static memory and peripheral devices. **Figure 10-4** shows sample timing and parameters that are detailed in **Table 10-16**.

The timing of each parameter consists of both a fixed delay portion and a clock related portion, as well as user controlled wait states. The equation:

$$t = D + P * (M + W)$$

should be used to determine the actual time of each parameter. The terms in this equation are defined as:

- t = Parameter delay time
- D = Fixed portion of the delay, due to on-chip path delays
- P = Period of the system clock, which determines the execution rate of the part (i.e., when the device is operating at 60MHz, P = 16.67 ns)
- M = Fixed portion of a clock period inherent in the design; this number is adjusted to account for possible derating of clock duty cycle
- W = Sum of the applicable wait state controls. The “Wait State Controls” column of **Table 10-16** shows the applicable controls for each parameter and the EMI chapter of the **56F8300 Peripheral User Manual** details what each wait state field controls.

When using the XTAL clock input directly as the chip clock without prescaling (ZSRC selects prescaler clock and prescaler is set to ÷ 1), the EMI quadrature clock is generated using both edges of the EXTAL clock input. In this situation only, parameter values must be adjusted for the duty cycle at XTAL. DCAOE

and DCAEO are used to make this duty cycle adjustment where needed.

DCAOE and DCAEO are calculated as follows:

DCAOE = 0.5 - MAX XTAL duty cycle, if ZSRC selects prescaler clock and the prescaler is set to ÷ 1
= 0.0 all other cases

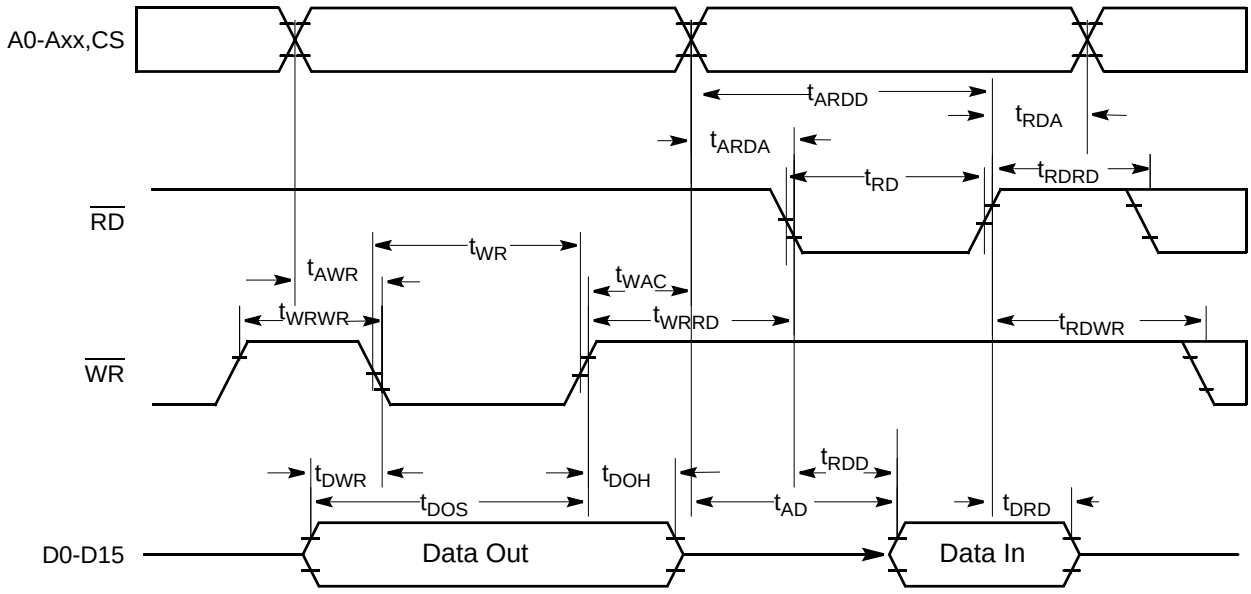
DCAEO = MIN XTAL duty cycle - 0.5, if ZSRC selects prescaler clock and the prescaler is set to ÷ 1
= 0.0 all other cases

Example of DCAOE and DCAEO calculation

Assuming prescaler is set for ÷ 1 and prescaler clock is selected by ZSRC, if XTAL duty cycle ranges between 45% and 60% high:

DCAOE = .50 - .60 = - 0.1
DCAEO = .45 - .50 = - 0.05

The timing of write cycles is different when WWS = 0 than when WWS > 0. Therefore, some parameters contain two sets of numbers to account for this difference. Use the “Wait States Configuration” column of **Table 10-16** to make the appropriate selection.



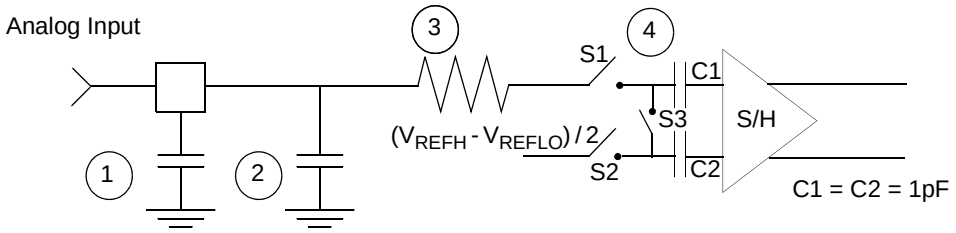
Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 10-4 External Memory Interface Timing

Note: When multiple lines are given for the same wait state configuration, calculate each and then select the smallest or most negative.

at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to V_{REFH} - V_{REFH} / 2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about V_{REFH} - V_{REFH} / 2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux; 500 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1pf

Figure 10-23 Equivalent Circuit for A/D Loading