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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	62
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8346vfver2

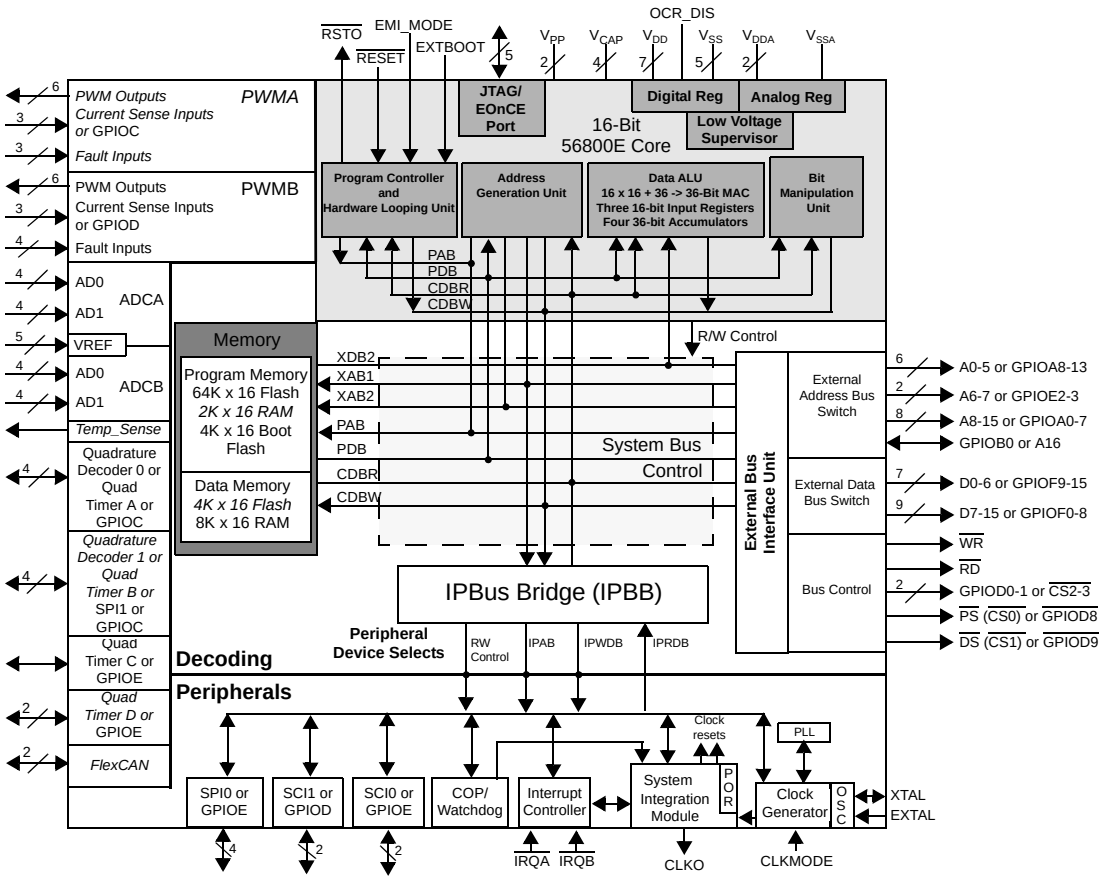
Document Revision History

Version History	Description of Change
Rev 1.0	Pre-Release version, Alpha customers only
Rev 2.0	Initial Public Release
Rev 3.0	Corrected typo in **Table 10-4**, Flash Endurance is 10,000 cycles. Addressed additional grammar issues.
Rev 4.0	Added “Typical Min” values to **Table 10-16**. Edited grammar, spelling, consistency of language throughout family. Updated values in Current Consumption per Power Supply Pin, **Table 10-7**, Regulator Parameters, **Table 10-9**, External Clock Operation Timing Requirements **Table 10-13**, SPI Timing, **Table 10-18**, ADC Parameters, **Table 10-24**, and IO Loading Coefficients at 10MHz, **Table 10-25**.
Rev 5.0	Added **Part 4.8**. Added the word “access” to FM Error Interrupt in **Table 4-5**. Removed min and max numbers. Clarified CSBAR 0 and CSBAR 1 reset values in **Table 4-10**. Removed min and max numbers, only documenting Typ. numbers for LVI in **Table 10-6**.
Rev 6.0	Updated numbers in **Table 10-7** and **Table 10-8** with more recent data. Corrected typo in **Table 10-3** in Pd characteristics.
Rev 7.0	Replaced any reference to Flash Interface Unit with Flash Memory Module. Added note to V_{CAP} pin in **Table 2-2**. Removed unneccessary notes in **Table 10-12**. Corrected temperature range in **Table 10-14**. Added ADC calibration information to **Table 10-24** and new graphs in **Figure 10-21**.
Rev 8.0	Clarified **Table 10-22**. Corrected Digital Input Current Low (pull-up enabled) numbers in **Table 10-5**. Removed text and Table 10-2. Replaced with note to **Table 10-1**.
Rev 9.0	Added 56F8146 information; edited to indicate differences in 56F8346 and 56F8146. Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables, then updated balance of electrical tables for consistency throughout family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 10.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 11.0	Updated **Table 10-24** to reflect new value for maximum Uncalibrated Gain Error
Rev 12.0	Deleted RSTO from Pin Group 2 (listed after **Table 10-1**). Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) in **Table 10-4**. Added RoHS-compliance and “pb-free” language to back cover.
Rev 13.0	Updated JTAG ID in **Section 6.5.4**. Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.

56F8346/56F8146 General Description

Note: *Features in italics are NOT available in the 56F8146 device.*

- Up to 60 MIPS at 60MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Access up to 1MB of off-chip program and data memory
- Chip Select Logic for glueless interface to ROM and SRAM
- 128KB of Program Flash
- *4KB of Program RAM*
- *8KB of Data Flash*
- 8KB of Data RAM
- 8KB of Boot Flash
- Up to two 6-channel PWM Modules
- Four 4-channel, 12-bit ADCs
- *Temperature Sensor*
- Up to two Quadrature Decoders
- Optional On-Chip Regulator
- *FlexCAN module*
- Two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interfaces (SPIs)
- Up to four general-purpose Quad Timers
- Computer Operating Properly (COP) / Watchdog
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 62 GPIO lines
- 144-pin LQFP Package



56F8346/56F8146 Block Diagram - 144 LQFP

1.1.3 Memory

Note: *Features in italics are NOT available in the 56F8146 device.*

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security protection feature
- On-chip memory, including a low-cost, high-volume Flash solution
  - 128KB of Program Flash
  - *4KB of Program RAM*
  - *8KB of Data Flash*
  - 8KB of Data RAM
  - 8KB of Boot Flash
- Off-chip memory expansion capabilities programmable for 0 - 30 wait states
  - Access up to 1MB of program memory or 1MB of data memory
  - Chip select logic for glueless interface to ROM and SRAM
- *EEPROM emulation capability*

1.1.4 Peripheral Circuits

Note: *Features in italics are NOT available in the 56F8146 device.*

- Pulse Width Modulator:
  - In the 56F8346, two Pulse Width Modulator modules, each with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
  - In the 56F8146, one Pulse Width Modulator module with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
- Four 12-bit, Analog-to-Digital Converters (ADCs), which support four simultaneous conversions with quad, 4-pin multiplexed inputs; ADC and PWM modules can be synchronized through Timer C, channels 2 and 3
- Quadrature Decoder:
  - In the 56F8346, two four-input Quadrature Decoders or two additional Quad Timers
  - In the 56F8146, one four-input Quadrature Decoder, which works in conjunction with Quad Timer A
- *Temperature Sensor diode can be connected, on the board, to any of the ADC inputs to monitor the on-chip temperature*
- Quad Timer:
  - In the 56F8346, four dedicated general-purpose Quad Timers totaling three dedicated pins: Timer C with one pin and Timer D with two pins
  - In the 56F8146, two Quad Timers; Timer A and Timer C both work in conjunction with GPIO
- Optional On-Chip Regulator
- *FlexCAN (CAN Version 2.0 B-compliant) module with 2-pin port for transmit and receive*

- Two Serial Communication Interfaces (SCIs), each with two pins (or four additional GPIO lines)
- Up to two Serial Peripheral Interfaces (SPIs), both with configurable 4-pin port (or eight additional GPIO lines)
  - In the 56F8346, SPI1 can also be used as Quadrature Decoder 1 or Quad Timer B
  - In the 56F8146, SPI1 can alternately be used only as GPIO
- Computer Operating Properly (COP)/Watchdog timer
- Two dedicated external interrupt pins
- 62 General Purpose I/O (GPIO) pins
- External reset input pin for hardware reset
- External reset output pin for system reset
- Integrated low-voltage interrupt module
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging
- Software-programmable, Phase Lock Loop (PLL)-based frequency synthesizer for the core clock

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- On-board 3.3V down to 2.6V voltage regulator for powering internal logic and memories; can be disabled
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 Device Description

The 56F8346 and 56F8146 are members of the 56800E core-based family of controllers. Each combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8346 and 56F8146 are well-suited for many applications. The devices include many peripherals that are especially useful for motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, *automotive* control (56F8346 only), engine management, noise suppression, remote utility metering, industrial control for power, lighting, and automation applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C/C++ Compilers to enable rapid development of optimized control applications.

The 56F8346 and 56F8146 support program execution from either internal or external memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. These devices also provide two external dedicated interrupt lines and up to 62 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

A key application-specific feature of the 56F8146 is the inclusion of one Pulse Width Modulator (PWM) module. This module incorporates three complementary, individually programmable PWM signal output pairs and can also support six independent PWM functions to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWM incorporates fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM module provides reference outputs to synchronize the Analog-to-Digital Converters through two channels of Quad Timer C.

The 56F8146 incorporates a Quadrature Decoder capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alert when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs); two Serial Peripheral Interfaces (SPIs); and two Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. An internal interrupt controller is also a part of the 56F8146.

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8146 device and are shaded in the following figures.*

The 56F8346/56F8146 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories, the external memory interface and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2, Signal/Connection Descriptions,** to see which signals are multiplexed with those of other peripherals.

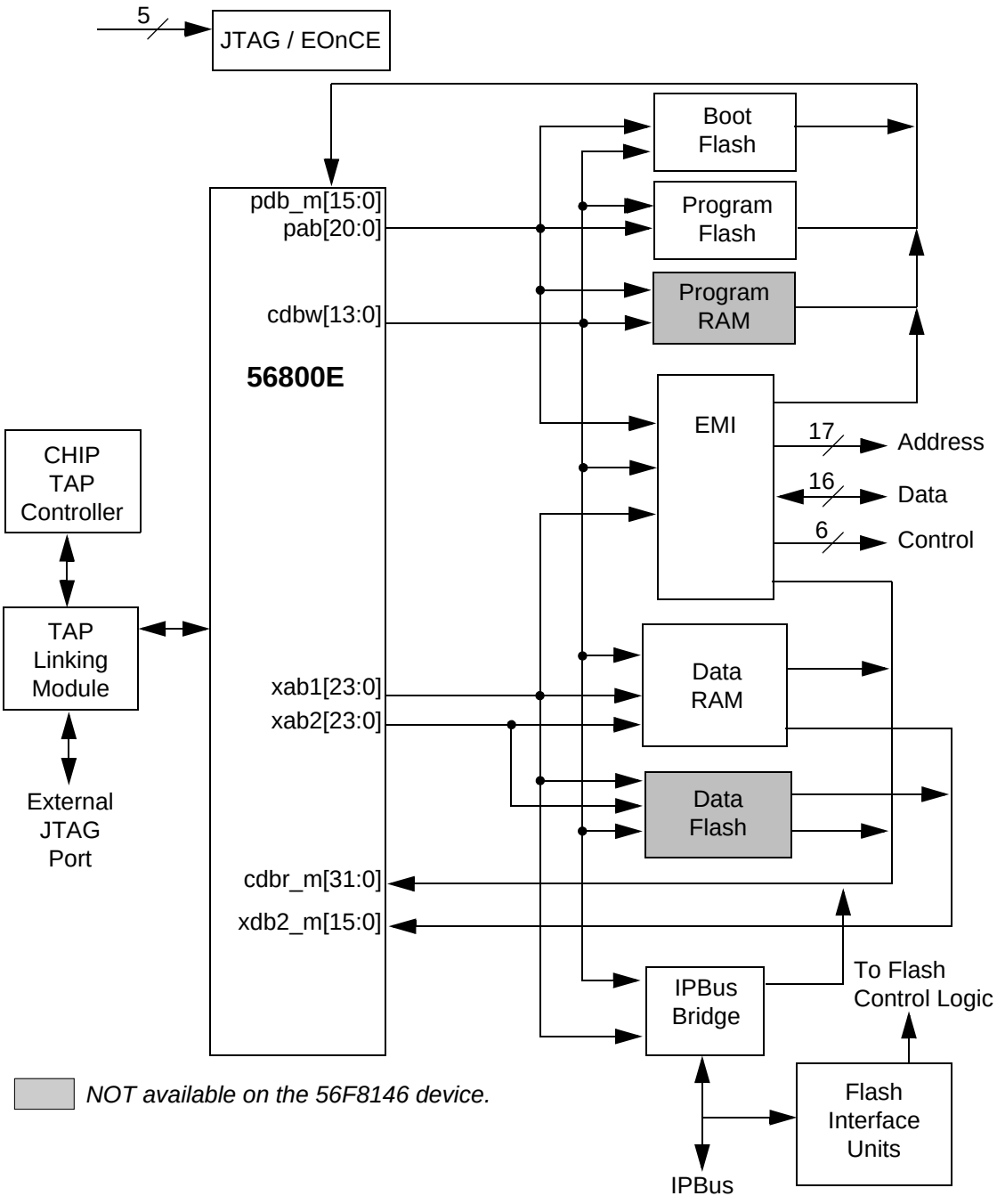


Figure 1-1 System Bus Interfaces

Note: Flash memories are encapsulated within the Flash Interface Unit (FIU). Flash control is accomplished by the I/O to the FIU over the peripheral bus, while reads and writes are completed between the core and the Flash memories.

Note: The primary data RAM port is 32 bits wide. Other data ports are 16 bits.

Table 2-2 Signal and Package Information for the 144 Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
$\overline{\text{RD}}$	45	Output	In reset, output is disabled, pull-up is enabled	**Read Enable** — $\overline{\text{RD}}$ is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low, pins D0 - D15 become inputs and an external device is enabled onto the data bus. When $\overline{\text{RD}}$ is deasserted high, the external data is latched inside the device. When $\overline{\text{RD}}$ is asserted, it qualifies the A0 - A16, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{CSn}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a static RAM or ROM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{RD}}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.
$\overline{\text{WR}}$	44	Output	In reset, output is disabled, pull-up is enabled	**Write Enable** — $\overline{\text{WR}}$ is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted low, pins D0 - D15 become outputs and the device puts data on the bus. When $\overline{\text{WR}}$ is deasserted high, the external data is latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0 - A16, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{CSn}}$ pins. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a static RAM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{WR}}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.
$\overline{\text{PS}}$ **($\overline{\text{CS0}}$)** **(GPIOD8)**	46	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Program Memory Select** — This signal is actually $\overline{\text{CS0}}$ in the EMI, which is programmed at reset for compatibility with the 56F80x $\overline{\text{PS}}$ signal. $\overline{\text{PS}}$ is asserted low for external program memory access. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{PS}}$ is tri-stated when the external bus is inactive. $\overline{\text{CS0}}$ resets to provide the $\overline{\text{PS}}$ function as defined on the 56F80x devices. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. To deactivate the internal pull-up resistor, clear bit 8 in the GPIOD_PUR register.

Table 2-2 Signal and Package Information for the 144 Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
RXD0 **(GPIOE1)**	5	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI0 receive data input **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOE_PUR register.
TXD1 **(GPIOD6)**	42	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI1 transmit data output **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 6 in the GPIOD_PUR register.
RXD1 **(GPIOD7)**	43	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI1 receive data input **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI input. To deactivate the internal pull-up resistor, clear bit 7 in the GPIOD_PUR register.
TCK	121	Schmitt Input	Input, pulled low internally	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-down resistor.
TMS	122	Schmitt Input	Input, pulled high internally	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	123	Schmitt Input	Input, pulled high internally	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register.

Table 2-2 Signal and Package Information for the 144 Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
SCLK0 **(GPIOE4)**	130	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0. To deactivate the internal pull-up resistor, clear bit 4 in the GPIOE_PUR register.
MOSI0 **(GPIOE5)**	132	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**SPI 0 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MOSI0. To deactivate the internal pull-up resistor, clear bit 5 in the GPIOE_PUR register.
MISO0 **(GPIOE6)**	131	Input/ Output Input/ Output	Input, pull-up enabled	**SPI 0 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MISO0. To deactivate the internal pull-up resistor, clear bit 6 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 144 Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
$\overline{\text{SS0}}$ **(GPIOE7)**	129	Input Input/ Output	Input, pull-up enabled	**SPI 0 Slave Select** — $\overline{\text{SS0}}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received. **Port E GPIO** — This GPIO pin can be individually programmed as input or output pin. After reset, the default state is $\overline{\text{SS0}}$. To deactivate the internal pull-up resistor, clear bit 7 in the GPIOE_PUR register.
PHASEA1 ***(TB0)*** **(SCLK1)** **(GPIOC0)**	6	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Phase A1** — Quadrature Decoder, PHASEA input for decoder 1. **TB0** — Timer B, Channel 0 **SPI 1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. To activate the SPI function, set the PHSA_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**. **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8346, the default state after reset is PHASEA1. In the 56F8146, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOC_PUR register.

Part 3 On-Chip Clock Synthesis (OCCS)

3.1 Introduction

Refer to the OCCS chapter of the **56F8300 Peripheral User Manual** for a full description of the OCCS. The material contained here identifies the specific features of the OCCS design. **Figure 3-1** shows the specific OCCS block diagram to reference in the OCCS chapter in the **56F8300 Peripheral User Manual**.

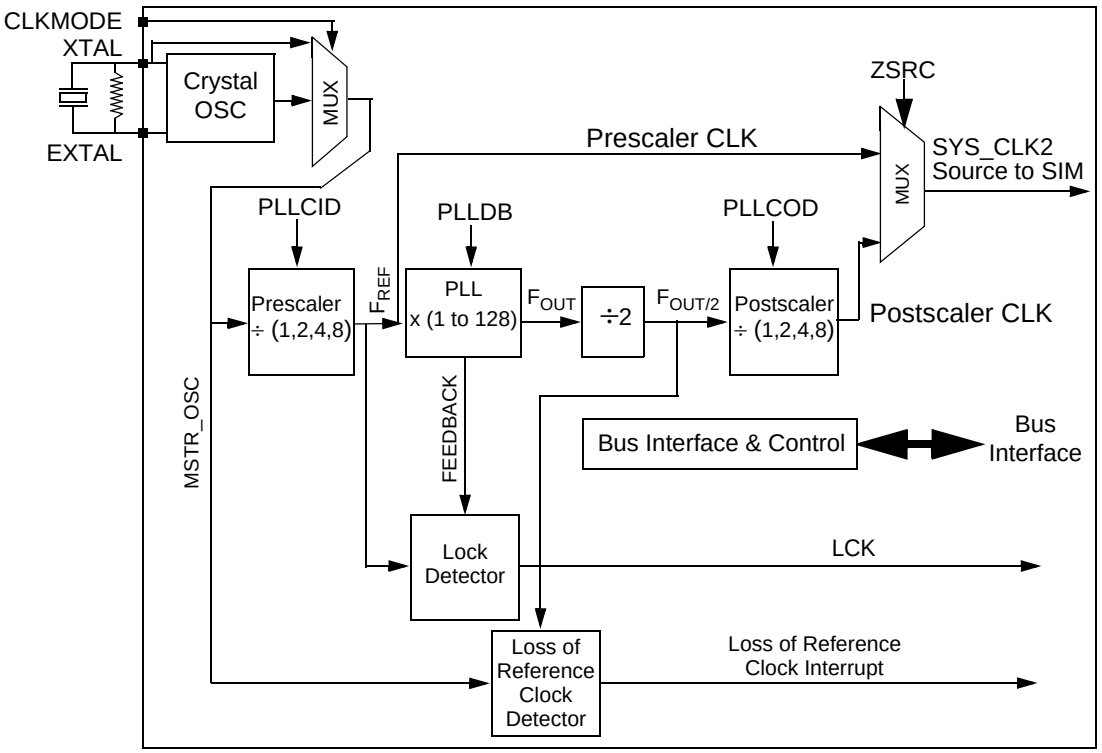


Figure 3-1 OCCS Block Diagram

3.2 External Clock Operation

The system clock can be derived from an external crystal, ceramic resonator, or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal or ceramic resonator, must be connected between the EXTAL and XTAL pins.

3.2.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 10-15**. A recommended crystal oscillator circuit is shown in **Figure 3-2**. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up.

Program Memory buses. They are controlled by one set of banked registers. Data Memory Flash resides on the Data Memory buses and is controlled separately by own set of banked registers.

The top nine words of the Program Memory Flash are treated as special memory locations. The content of these words is used to control the operation of the Flash Controller. Because these words are part of the Flash Memory content, their state is maintained during power-down and reset. During chip initialization, the content of these memory locations is loaded into Flash Memory control registers, detailed in the Flash Memory chapter of the **56F8300 Peripheral User Manual**. These configuration parameters are located between $00_FFF7 and $00_FFFF.

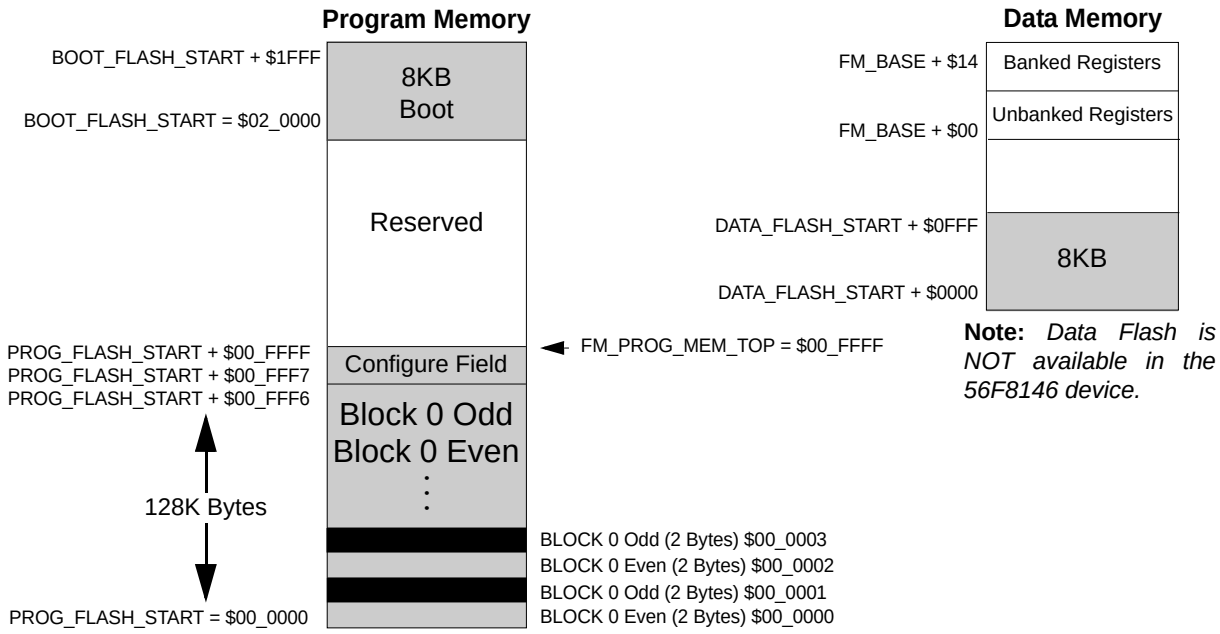


Figure 4-1 Flash Array Memory Maps

Table 4-7 shows the page and sector sizes used within each Flash memory block on the chip.

Note: *Data Flash is NOT available on the 56F8146 device.*

Table 4-7. Flash Memory Partitions

	Flash Size	Sectors	Sector Size	Page Size
Program Flash	128KB	16	4K x 16 bits	512 x 16 bits
Data Flash	8KB	16	256 x 16 bits	256 x 16 bits
Boot Flash	8KB	4	1K x 16 bits	256 x 16 bits

Please see **56F8300 Peripheral User Manual** for additional Flash information.

Table 4-16 Pulse Width Modulator B Registers Address Map (PWMB_BASE = $00 F160)

Register Acronym	Address Offset	Register Description
PWMB_PMCTL	$0	Control Register
PWMB_PMFCTL	$1	Fault Control Register
PWMB_PMFSA	$2	Fault Status Acknowledge Register
PWMB_PMOUT	$3	Output Control Register
PWMB_PMCNT	$4	Counter Register
PWMB_PWMCM	$5	Counter Modulo Register
PWMB_PWMVAL0	$6	Value Register 0
PWMB_PWMVAL1	$7	Value Register 1
PWMB_PWMVAL2	$8	Value Register 2
PWMB_PWMVAL3	$9	Value Register 3
PWMB_PWMVAL4	$A	Value Register 4
PWMB_PWMVAL5	$B	Value Register 5
PWMB_PMDEADTM	$C	Dead Time Register
PWMB_PMDISMAP1	$D	Disable Mapping Register 1
PWMB_PMDISMAP2	$E	Disable Mapping Register 2
PWMB_PMCFG	$F	Configure Register
PWMB_PMCCR	$10	Channel Control Register
PWMB_PMPORT	$11	Port Register
PWMB_PMICCR	$12	PWM Internal Correction Control Register

Table 4-17 Quadrature Decoder 0 Registers Address Map (DEC0_BASE = $00 F180)

Register Acronym	Address Offset	Register Description
DEC0_DECCR	$0	Decoder Control Register
DEC0_FIR	$1	Filter Interval Register
DEC0_WTR	$2	Watchdog Time-out Register
DEC0_POSD	$3	Position Difference Counter Register
DEC0_POSDH	$4	Position Difference Counter Hold Register

Table 4-33 GPIOE Registers Address Map (Continued) (GPIOE_BASE = $00 F330)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOE_PPMODE	$9	Push-Pull Mode Register	0 x 3FFF
GPIOE_RAWDATA	$A	Raw Data Input Register	—

Table 4-34 GPIOF Registers Address Map (GPIOF_BASE = $00 F340)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOF_PUR	$0	Pull-up Enable Register	0 x FFFF
GPIOF_DR	$1	Data Register	0 x 0000
GPIOF_DDR	$2	Data Direction Register	0 x 0000
GPIOF_PER	$3	Peripheral Enable Register	0 x FFFF
GPIOF_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOF_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOF_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOF_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOF_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOF_PPMODE	$9	Push-Pull Mode Register	0 x FFFF
GPIOF_RAWDATA	$A	Raw Data Input Register	—

Table 4-35 System Integration Module Registers Address Map (SIM_BASE = $00 F350)

Register Acronym	Address Offset	Register Description
SIM_CONTROL	$0	Control Register
SIM_RSTSTS	$1	Reset Status Register
SIM_SCR0	$2	Software Control Register 0
SIM_SCR1	$3	Software Control Register 1
SIM_SCR2	$4	Software Control Register 2
SIM_SCR3	$5	Software Control Register 3
SIM_MSH_ID	$6	Most Significant Half JTAG ID
SIM_LSH_ID	$7	Least Significant Half JTAG ID
SIM_PUDR	$8	Pull-up Disable Register
		Reserved

routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Part 5.3.3**. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-5**.

5.6.16 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

Base + $F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-18 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

5.6.16.1 Fast Interrupt 1 Vector Address Low (FIVAL1)—Bits 15–0

The lower 16 bits of vector address are used for Fast Interrupt 1. This register is combined with FIVAH1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.17 Fast Interrupt 1 Vector Address High Register (FIVAH1)

Base + $10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-19 Fast Interrupt 1 Vector Address High Register (FIVAH1)

5.6.17.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.17.2 Fast Interrupt 1 Vector Address High (FIVAH1)—Bits 4–0

The upper five bits of the vector address are used for Fast Interrupt 1. This register is combined with FIVAL1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.18 IRQ Pending 0 Register (IRQP0)

Base + $11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [16:2]															1
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-20 IRQ Pending 0 Register (IRQP0)

5.6.23.1 Reserved—Bits 96–82

This bit field is reserved or not implemented. The bits are read as 1 and cannot be modified by writing.

5.6.23.2 IRQ Pending (PENDING)—Bit 81

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.24 Reserved—Base + 17

5.6.25 Reserved—Base + 18

5.6.26 Reserved—Base + 19

5.6.27 Reserved—Base + 1A

5.6.28 Reserved—Base + 1B

5.6.29 Reserved—Base + 1C

5.6.30 ITCN Control Register (ICTL)

Base + $1D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	INT	IPIC		VAB							INT_DIS	1	$\overline{\text{IRQB}}$ STATE	$\overline{\text{IRQA}}$ STATE	$\overline{\text{IRQB}}$ EDG	$\overline{\text{IRQA}}$ EDG
Write																
RESET	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0

Figure 5-26 ITCN Control Register (ICTL)

5.6.30.1 Interrupt (INT)—Bit 15

This *read-only* bit reflects the state of the interrupt to the 56800E core.

- 0 = No interrupt is being sent to the 56800E core

$C	SIM_PCE	R	EMI	ADCB	ADCA	CAN	DEC1	DEC0	TMRD	TMRC	TMRB	TMRA	SCI1	SCI0	SPI1	SPI0	PWMB	PWMA
		W																
$D	SIM_ISALH	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ISAL[23:22]	
		W																
$E	SIM_ISALL	R	ISAL[21:6]															
		W																

= Reserved

Figure 6-2 SIM Register Map Summary (Continued)

6.5.1 SIM Control Register (SIM_CONTROL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	EMI_MODE	ONCE EBL	SW RST	STOP_DISABLE		WAIT_DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-3 SIM Control Register (SIM_CONTROL)

6.5.1.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.1.2 EMI_MODE (EMI_MODE)—Bit 6

This bit reflects the current (non-clocked) state of the EMI_MODE pin. During reset, this bit, coupled with the EXTBOOT signal, is used to initialize address bits [19:16] either as GPIO or as address. These settings can be explicitly overwritten using the appropriate GPIO peripheral enable register at any time after reset. In addition, this pin can be used as a general purpose input pin after reset.

- 0 = External address bits [19:16] are initially programmed as GPIO
- 1 = When booted with EXTBOOT = 1, A[19:16] are initially programmed as address. If EXTBOOT is 0, they are initialized as GPIO.

6.5.1.3 OnCE Enable (OnCE EBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

6.5.1.4 Software Reset (SWRST)—Bit 4

This bit is always read as 0. Writing a 1 to this field will cause the part to reset.

6.5.1.5 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 - STOP mode will be entered when the 56800E core executes a STOP instruction
- 01 - The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can be reprogrammed in the future

Part 7 Security Features

The 56F8346/56F8146 offer security features intended to prevent unauthorized users from reading the contents of the Flash Memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory section in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable external P-space accesses restricting code execution to internal memory, disable EXTBOOT = 1 mode, and disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Blocking Mechanisms

The 56F8346/56F8146 have several operating functional and test modes. Effective Flash security must address operating mode selection and anticipate modes in which the on-chip Flash can be compromised and read without explicit user permission. Methods to block these are outlined in the next subsections.

7.2.1 Forced Operating Mode Selection

At boot time, the SIM determines in which functional modes the device will operate. These are:

- Internal Boot Mode
- External Boot Mode
- Secure Mode

When Flash security is enabled as described in the Flash Memory module specification, the device will boot in internal boot mode, disable all access to external P-space, and start executing code from the Boot Flash at address 0x02_0000.

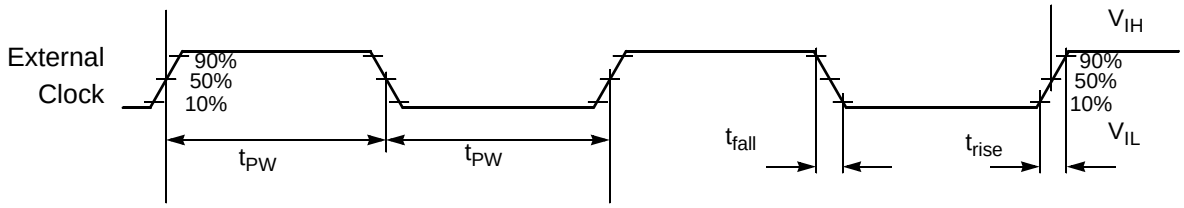
This security affords protection only to applications in which the device operates in internal Flash security

10.5 External Clock Operation Timing

Table 10-13 External Clock Operation Timing Requirements[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[2]	f_{osc}	0	—	120	MHz
Clock Pulse Width[3]	t_{PW}	3.0	—	—	ns
External clock input rise time[4]	t_{rise}	—	—	10	ns
External clock input fall time[5]	t_{fall}	—	—	10	ns

1. Parameters listed are guaranteed by design.
2. See **Figure 10-3** for details on using the recommended connection of an external clock driver.
3. The high or low pulse width must be no smaller than 8.0ns or the chip will not function.
4. External clock input rise time is measured from 10% to 90%.
5. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 10-3 External Clock Timing

10.6 Phase Locked Loop Timing

Table 10-14 PLL Timing

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	8.4	MHz
PLL output frequency[2] (f_{OUT})	f_{op}	160	—	260	MHz
PLL stabilization time[3] -40° to +125°C	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.
2. ZCLK may not exceed 60MHz. For additional information on ZCLK and (f_{OUT}/2), please refer to the OCCS chapter in the **56F8300 Peripheral User Manual**.

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter (^oC)/W
P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct device operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better performance tolerances.