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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	8MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212h2sdsp-w4

1. Overview

1.1 Features

The R8C/2H Group and R8C/2J Group of single-chip MCUs incorporate the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

1.1.1 Applications

Electric power meters, electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Table 1.1 outlines the Specifications for R8C/2H Group and Table 1.2 outlines the Specifications for R8C/2J Group.

1.2 Product List

Table 1.3 lists Product List for R8C/2H Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2H Group. Table 1.4 lists Product List for R8C/2J Group, Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2J Group.

Table 1.3 Product List for R8C/2H Group

Current of Mar. 2008

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212H1SNSP	4 Kbytes	256 bytes	PLSP0020JB-A	N version
R5F212H2SNSP	8 Kbytes	384 bytes	PLSP0020JB-A	
R5F212H1SDSP	4 Kbytes	256 bytes	PLSP0020JB-A	D version
R5F212H2SDSP	8 Kbytes	384 bytes	PLSP0020JB-A	

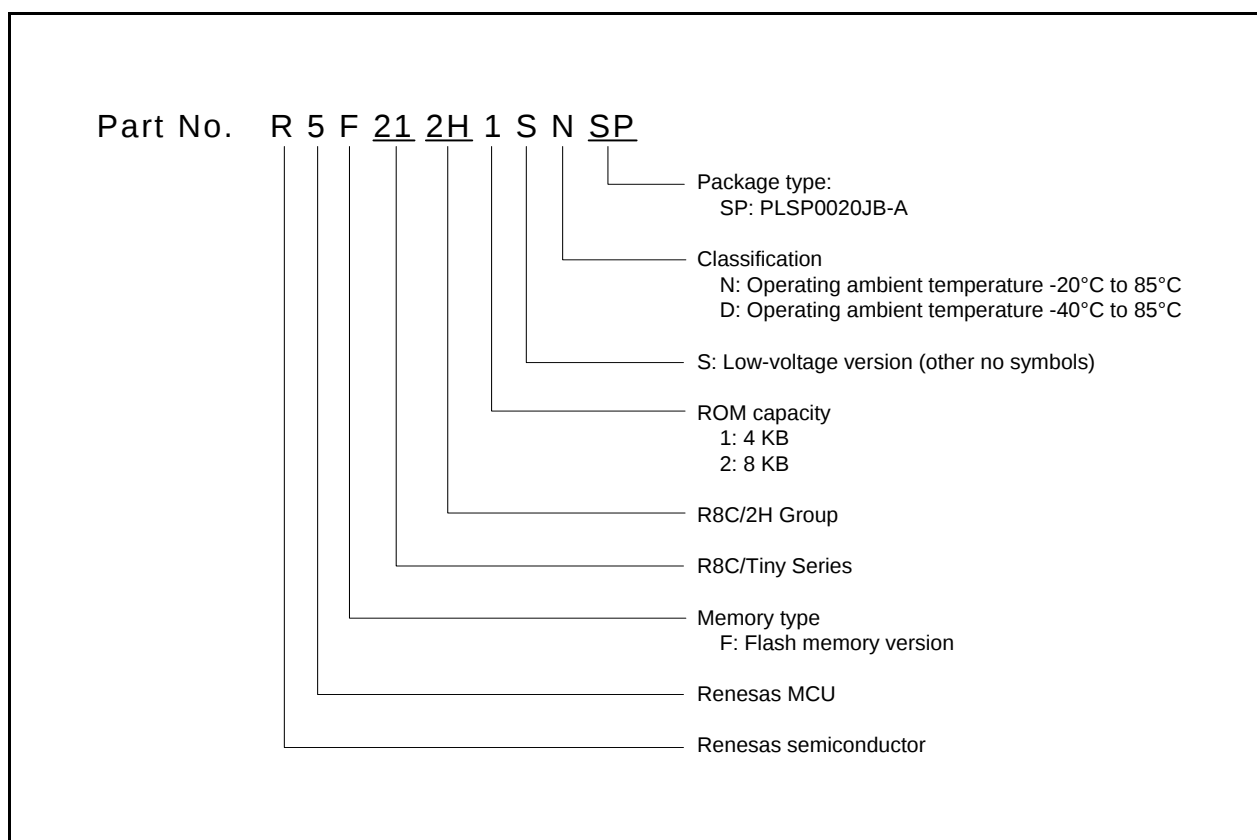


Figure 1.1 Part Number, Memory Size, and Package of R8C/2H Group

1.4 Pin Assignment

Figure 1.5 shows Pin Assignment (Top View) of R8C/2H Group. Table 1.5 outlines the Pin Name Information by Pin Number of R8C/2H Group.

Figure 1.6 shows Pin Assignment (Top View) of R8C/2J Group. Table 1.6 outlines the Pin Name Information by Pin Number of R8C/2J Group.

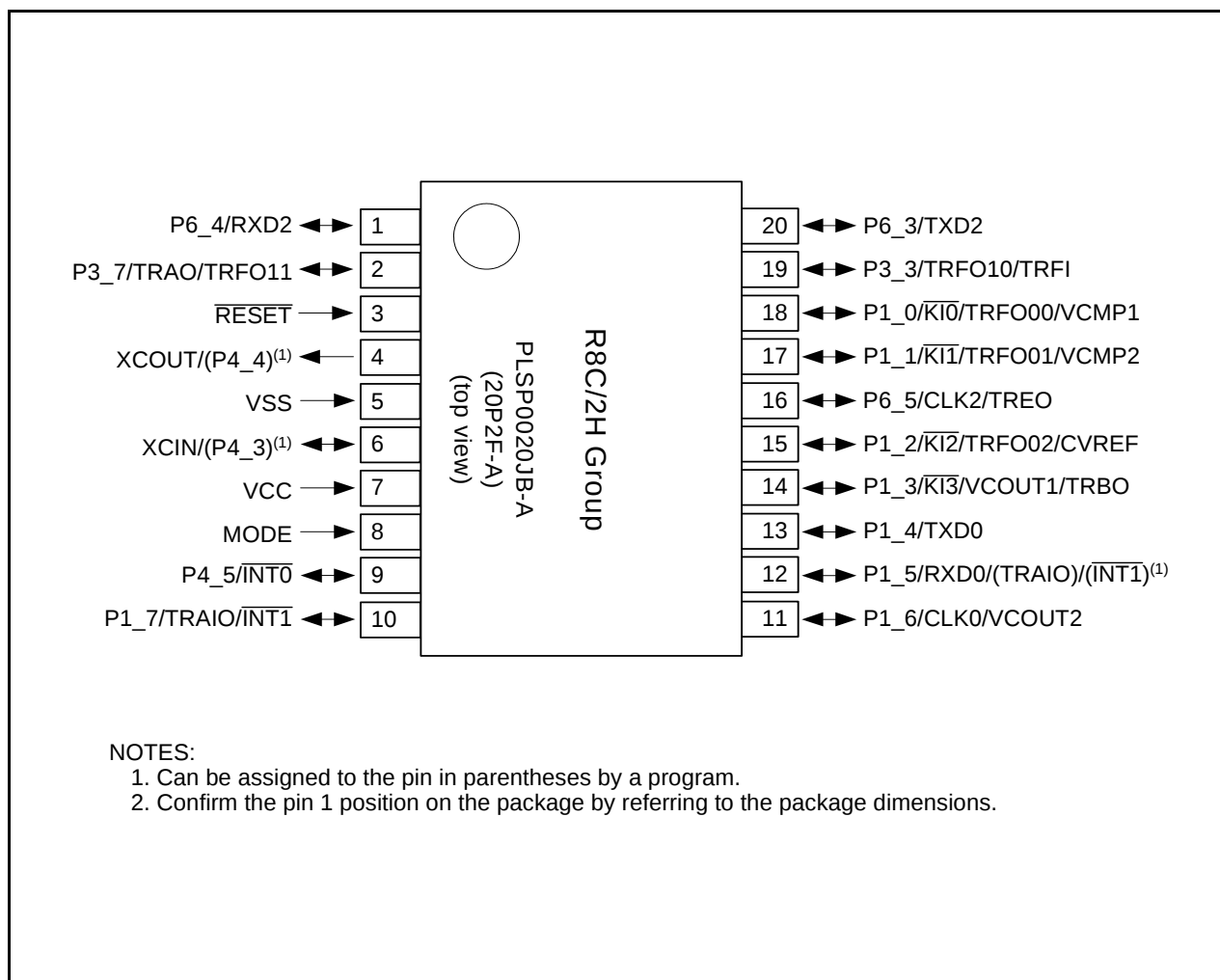


Figure 1.5 Pin Assignment (Top View) of R8C/2H Group

Table 1.5 Pin Name Information by Pin Number of R8C/2H Group

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
			Interrupt	Timer	Serial Interface	Comparator
1		P6_4			RXD2	
2		P3_7		TRAO/TRFO11		
3	RESET					
4	XCOUT	(P4_4)				
5	VSS					
6	XCIN	(P4_3)				
7	VCC					
8	MODE					
9		P4_5	INT0			
10		P1_7	INT1	TRAIO		
11		P1_6			CLK0	VCOUT2
12		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0	
13		P1_4			TXD0	
14		P1_3	KI3	TRBO		VCOUT1
15		P1_2	KI2	TRFO02		CVREF
16		P6_5		TREO	CLK2	
17		P1_1	KI1	TRFO01		VCMP2
18		P1_0	KI0	TRFO00		VCMP1
19		P3_3		TRFO10/TRFI		
20		P6_3			TXD2	

NOTE:

1. Can be assigned to the pin in parentheses by a program.

Table 1.6 Pin Name Information by Pin Number of R8C/2J Group

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
			Interrupt	Timer	Serial Interface	Comparator
1	NC ⁽²⁾					
2		P3_7		TRAO/TRFO11		
3	RESET					
4	NC ⁽²⁾					
5	VSS					
6	NC ⁽²⁾					
7	VCC					
8	MODE					
9		P4_5	INT0			
10		P1_7	INT1	TRAIO		
11		P1_6			CLK0	VCOUT2
12		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0	
13		P1_4			TXD0	
14		P1_3	KI3	TRBO		VCOUT1
15		P1_2	KI2	TRFO02		CVREF
16		P6_5				
17		P1_1	KI1	TRFO01		VCMP2
18		P1_0	KI0	TRFO00		VCMP1
19		P3_3		TRFO10/TRFI		
20	NC ⁽²⁾					

NOTES:

1. Can be assigned to the pin in parentheses by a program.
2. NC(Non-Connection)

Table 4.2 SFR Information (2)⁽¹⁾

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 00100000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁵⁾	VW1C	00001010b
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00000010b
0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	1000X010b ⁽³⁾ 1100X011b ⁽⁴⁾
0039h			
003Ah			
003Bh	Voltage Detection Circuit External Input Control Register	VCAB	00h
003Ch	Comparator Mode Register	ALCMR	00h
003Dh	Voltage Monitor Circuit Edge Select Register	VCAC	00h
003Eh	BGR Control Register	BGRCR	00h
003Fh	BGR Trimming Register	BGRTRM	When Shipping
0040h			
0041h	Comparator 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0042h	Comparator 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register ⁽⁶⁾	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register ⁽⁶⁾	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register ⁽⁶⁾	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah			
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh	Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
6. This register is not implemented in the R8C/2J Group.

Table 4.5 SFR Information (5)⁽¹⁾

Address	Register	Symbol	After reset
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h	Pin Select Register 2	PINSR2	00h
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh			
00FFh			
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register ⁽²⁾	TRESEC	XXh
0119h	Timer RE Minute Data Register / Compare Data Register ⁽²⁾	TREMIN	XXh
011Ah	Timer RE Hour Data Register ⁽²⁾	TREHR	X0XXXXXXb
011Bh	Timer RE Day of Week Data Register ⁽²⁾	TREWK	X0000XXXb
011Ch	Timer RE Control Register 1 ⁽²⁾	TRECR1	XXX0X0X0b
011Dh	Timer RE Control Register 2 ⁽²⁾	TRECR2	00XXXXXXb
011Eh	Timer RE Count Source Select Register ⁽²⁾	TRECSR	00001000b
011Fh	Timer RE Real-Time Clock Precision Adjust Register ⁽²⁾	TREOPR	00h
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions
2. This register is not implemented in the R8C/2J Group.

Table 4.8 SFR Information (8)⁽¹⁾

Address	Register	Symbol	After reset
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			

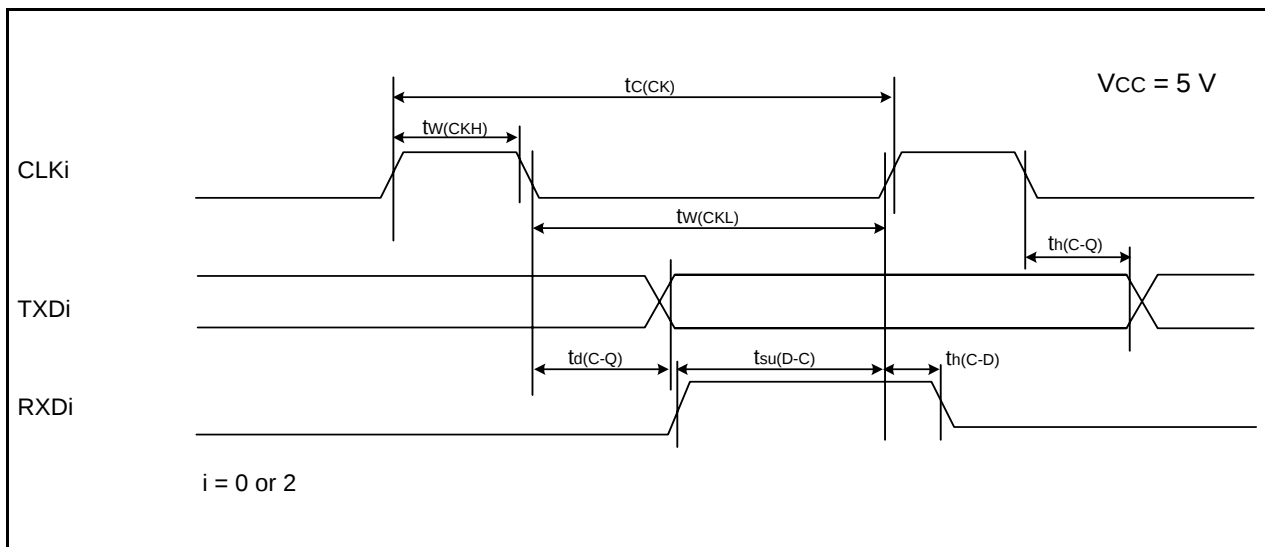
X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 5.16 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ or } 2$ **Figure 5.5 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.17 External Interrupt $\overline{INTi}$ ($i = 0 \text{ or } 1$) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

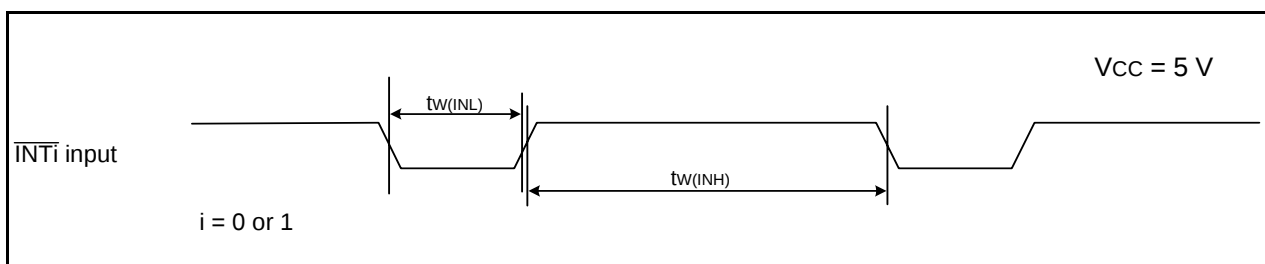
**Figure 5.6 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Table 5.18 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output "H" voltage		I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage		I _{OL} = 1 mA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}},$ $\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$ $\overline{\text{RXD0}}, \overline{\text{RXD2}},$ $\overline{\text{CLK0}}, \overline{\text{CLK2}}$		0.1	0.3	—	V
		$\overline{\text{RESET}}$		0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3 V	—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3 V	—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3 V	66	160	500	kΩ
R _{FXCIN}	Feedback resistance	XCIN		—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

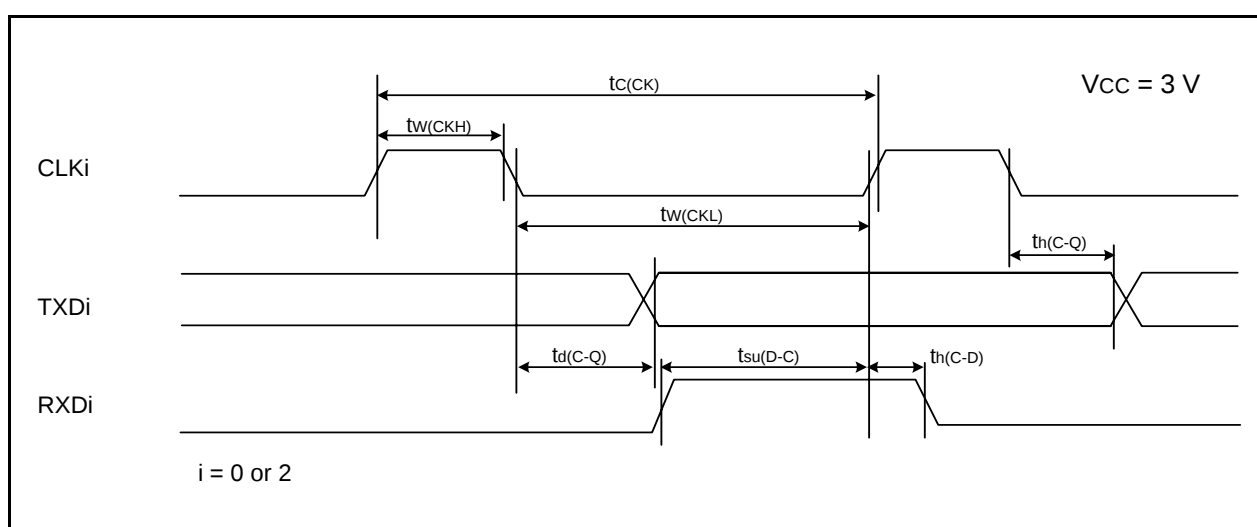
NOTE:

- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.22 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 2

**Figure 5.9 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.23 External Interrupt $\overline{INTi}$ (i = 0 or 1) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	380 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

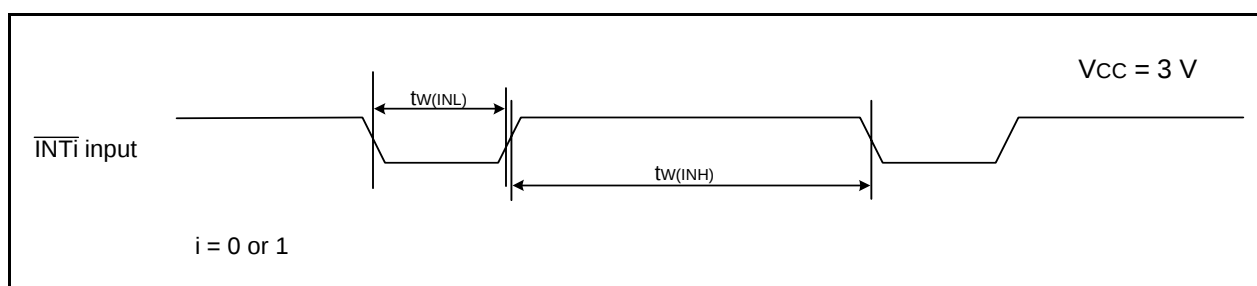
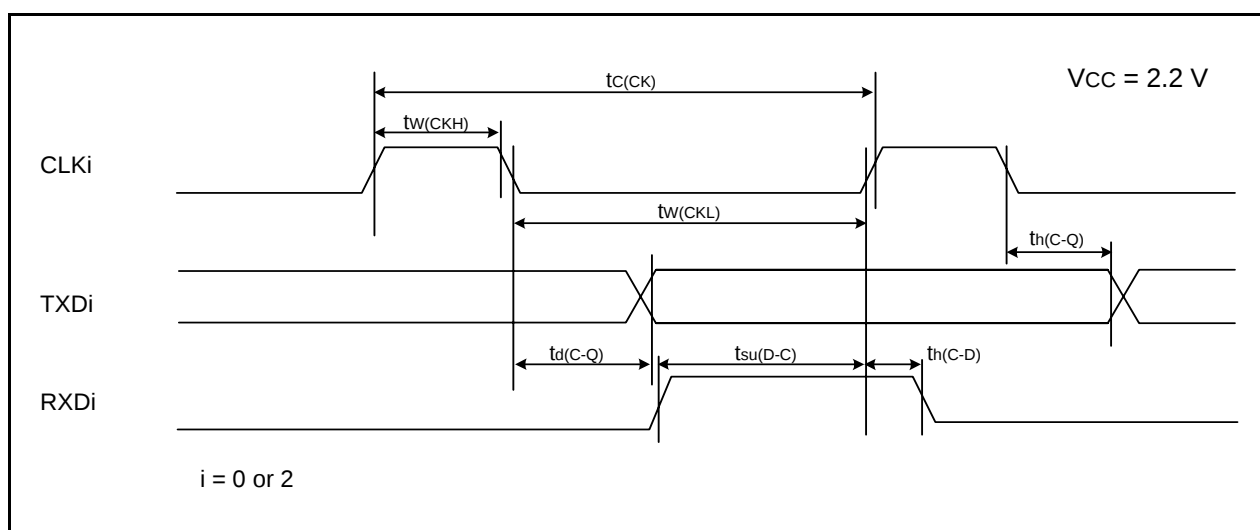
**Figure 5.10 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V**

Table 5.28 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 2

**Figure 5.13 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.29 External Interrupt $\overline{INTi}$ (i = 0 or 1) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	1000 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

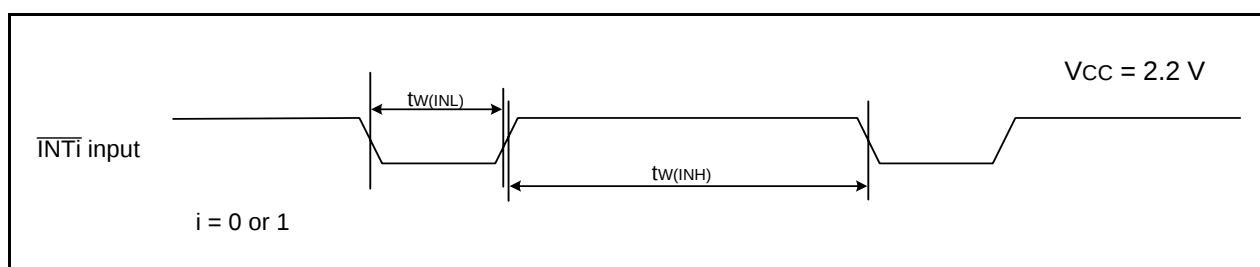
**Figure 5.14 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 2.2 V**

Table 5.33 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level		2.2	2.3	2.4	V
—	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 5.0 V	—	0.9	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	300	μs
V _{ccmin}	MCU operating voltage minimum value		2.2	—	—	V

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.34 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level ⁽⁴⁾		2.70	2.85	3.00	V
—	Voltage monitor 1 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	—	0.6	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.35 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage detection level		3.3	3.6	3.9	V
—	Voltage monitor 2 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V _{CC} = 5.0 V	—	0.6	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.36 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V _{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V _{det0}	V
tr _{th}	External power V _{CC} rise gradient ⁽²⁾		20	–	–	mV/msec

NOTES:

1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30 s or more if –20°C ≤ T_{opr} ≤ 85°C, maintain t_{w(por1)} for 3,000 s or more if –40°C ≤ T_{opr} < –20°C.

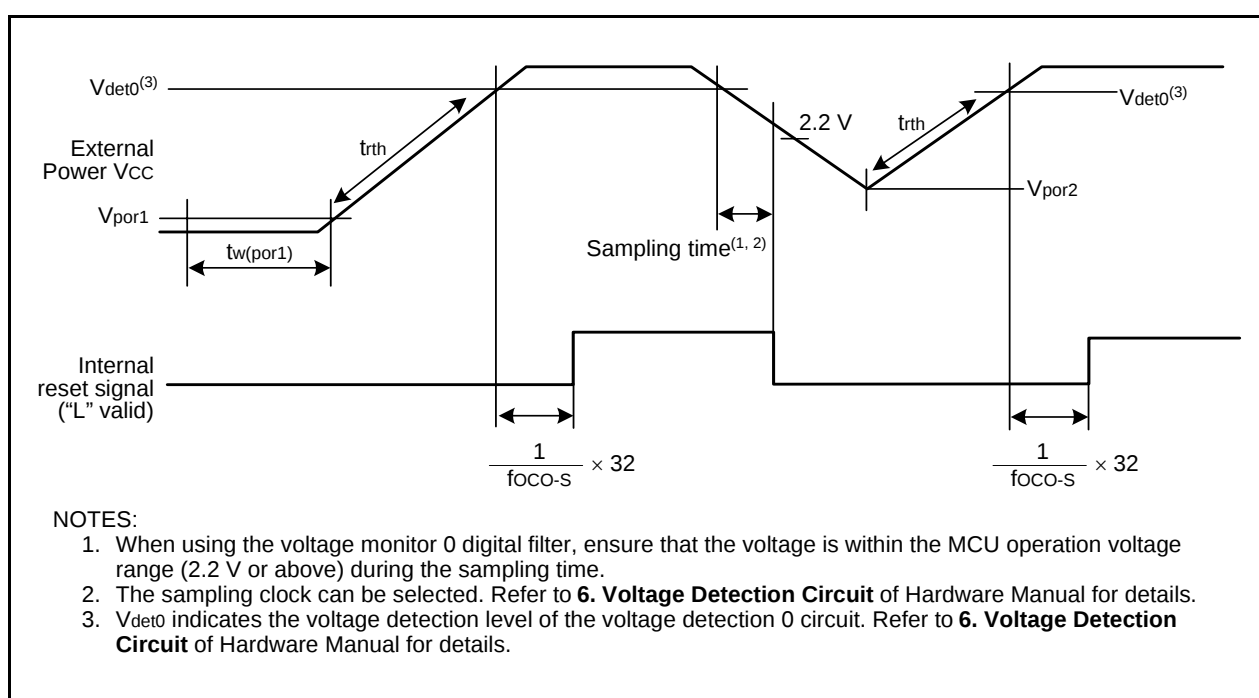
**Figure 5.16 Reset Circuit Electrical Characteristics**

Table 5.42 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	8	mA
			High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	μA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	μA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	μA
		Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.8	3	μA
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.2	–	μA
			Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	8	μA
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	μA

Table 5.46 Electrical Characteristics (3) [V_{CC} = 3 V]

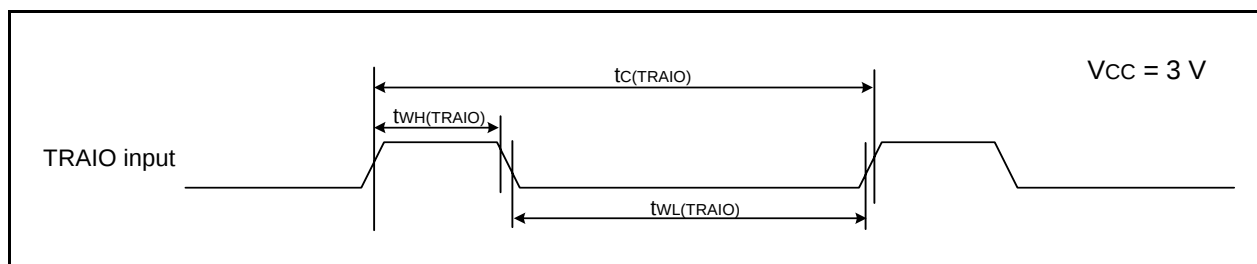
Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output "H" voltage		I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage		I _{OL} = 1 mA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}},$ $\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$ $\overline{\text{RXD0}}, \overline{\text{CLK0}}$		0.1	0.3	—	V
		$\overline{\text{RESET}}$		0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3 V	—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3 V	—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3 V	66	160	500	kΩ
V _{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

NOTE:

- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

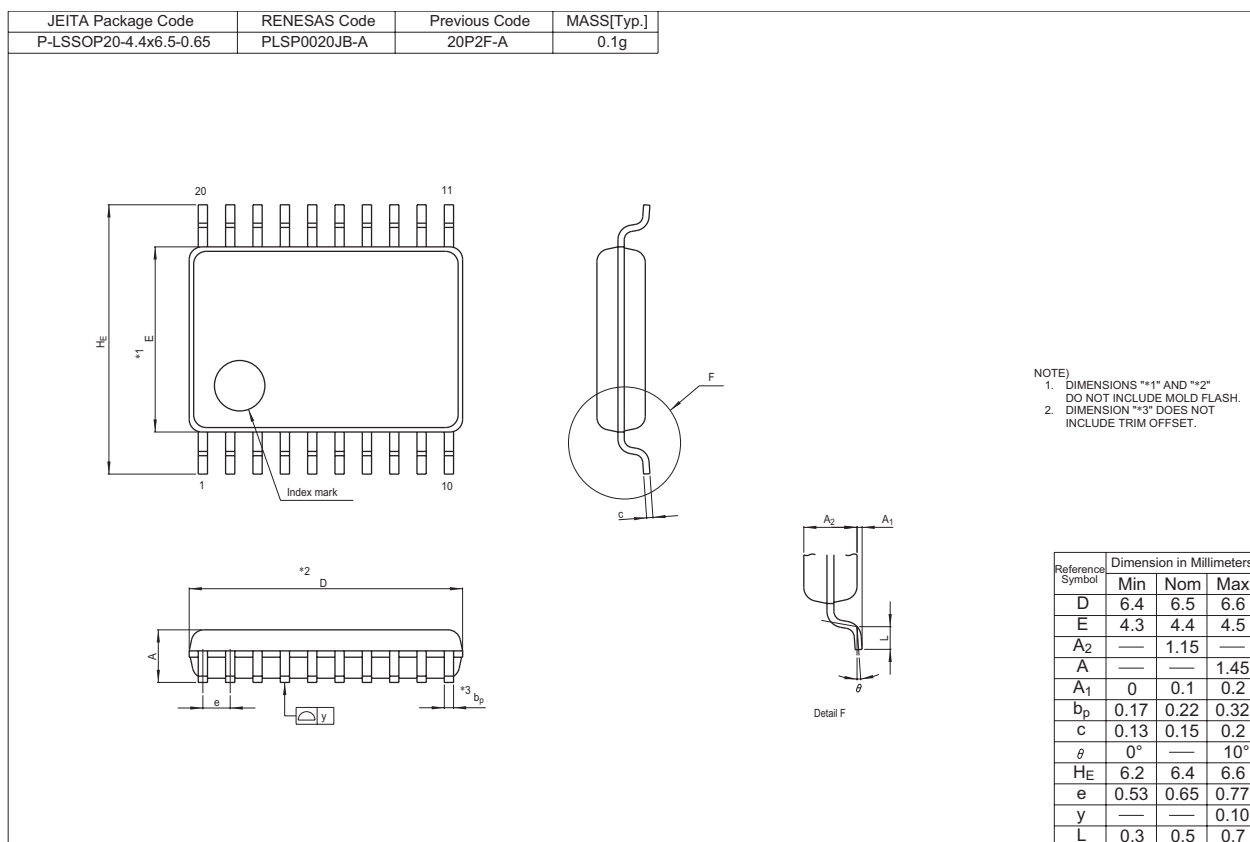
Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.48 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{TRAIO})$	TRAIO input cycle time	300	–	ns
$t_{WH}(\text{TRAIO})$	TRAIO input "H" width	120	–	ns
$t_{WL}(\text{TRAIO})$	TRAIO input "L" width	120	–	ns

**Figure 5.20 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/2H Group, R8C/2J Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Jun 18, 2007	–	First Edition issued
0.10	Jul 20, 2007	20	Table 4.2: 0038h After reset; “0000X010b” → “1000X010b”, “0100X011b” → “1100X011b”
		31 to 64	5. Electrical Characteristics added
0.20	Nov 12, 2007	2	Table 1.1 I/O Ports: “• Output-only: 1” added
			“• CMOS I/O ports: 16” → “• CMOS I/O ports: 15”
		6	Figure 1.3 revised
		8	Figure 1.5 revised
		9	Table 1.5 Pin Number: 4, 6, 16 revised
		12	Table 1.7 I/O port: “P4_3 to P4_5” → “P4_3, P4_5”
			Timer RE, Output port added
		19	Table 4.1 0006h “01001000b” → “01011000b”
		23	Table 4.5 0118h to 011Dh: After reset revised
			011Fh “Timer RE Real-Time Clock Precision Adjust Register” added
		31, 48	Table 5.2, Table 5.31 NOTE2 revised
		54, 58	Table 5.42, Table 5.47 revised
		62	Table 5.52 revised
1.00	Mar 28, 2008	All pages	“Under development” deleted
		2, 3	Table 1.1, Table 1.2 revised
		4, 5	Table 1.3, Table 1.4; “(D): Under development” deleted
		17, 18	Figure 3.1, Figure 3.2; “Expanded area” deleted
		19	Table 4.1 “002Eh” “002Fh” revised
		20	Table 4.2 “003Eh” “003Fh” revised
		32	Table 5.3 revised
			Old Figure 5.2 deleted
		35	Table 5.8, Table 5.11 revised
			Table 5.9 revised, NOTE3 added
		37	Table 5.13 revised
		41	Table 5.19 revised
		45	Table 5.25 revised
		49	Table 5.32 revised
			Old Figure 5.17 deleted
		52	Table 5.37, Table 5.40 revised
			Table 5.38 revised, NOTE3 added
		54	Table 5.42 revised
		58	Table 5.47 revised

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Rev.	Date	Description	
		Page	Summary
1.00	Mar 28, 2008	62	Table 5.52 revised

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