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NXP USA Inc. - MK30DN512VLL10 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, IrDA, SD, SPI, UART/USART
Peripherals	DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 38x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk30dn512vll10

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK30 and MK30.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
K##	Kinetis family	• K30
A	Key attribute	 D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
М	Flash memory type	 N = Program flash only X = Program flash and FlexMemory

Table continues on the next page...





3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF



3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μΑ

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	C°
V _{DD}	3.3 V supply voltage	3.3	V



Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	185	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V _{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	V _{DD} + 0.3	V
I _D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V
V _{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + $(V_{IH} - V_{IL})/2$.

Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

- 1. output pins
 - have $C_L=30$ pF loads,
 - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
 - are configured for high drive strength (PORTx_PCRn[DSE]=1)
- 2. input pins
 - have their passive filter disabled (PORTx_PCRn[PFE]=0)

5.2 Nonswitching electrical specifications



Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • V_{DD} slew rate ≥ 5.7 kV/s • V_{DD} slew rate < 5.7 kV/s		300 1.7 V / (V _{DD} slew rate)	μs	1
	• VLLS1 → RUN	_	130	μs	
	• VLLS2 \rightarrow RUN		92	μs	
	• VLLS3 → RUN	_	92	μs	
	• LLS → RUN	—	5.9	μs	
	• VLPS → RUN		5.0	μs	
	• STOP \rightarrow RUN		5.0	μs	

Table 5. Power mode transition operating behaviors

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 1.8V • @ 3.0V		37 38	63 64	mA mA	2
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash • @ 1.8V • @ 3.0V • @ 25°C • @ 125°C	 	46 47 58	77 63 79	mA mA mA	3, 4
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	_	20	_	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	_	9		mA	5
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	_	1.12	—	mA	6

Table continues on the next page...



- 2. $V_{DD} = 3.3 \text{ V}, T_A = 25 \text{ °C}, f_{OSC} = 12 \text{ MHz} \text{ (crystal)}, f_{SYS} = 96 \text{ MHz}, f_{BUS} = 48 \text{ MHz}$
- 3. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions TEM Cell and Wideband TEM Cell Method

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to www.freescale.com.
- 2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	_	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes	
	Normal run mode					
f _{SYS}	System and core clock	—	100	MHz		
f _{BUS}	Bus clock	_	50	MHz		
f _{FLASH}	Flash clock		25	MHz		
f _{LPTMR}	LPTMR clock	_	25	MHz		
	VLPR mode ¹			•		
f _{SYS}	System and core clock		4	MHz		
f _{BUS}	Bus clock	—	4	MHz		
f _{FLASH}	Flash clock	_	1	MHz		
f _{ERCLK}	External reference clock		16	MHz		
f _{LPTMR_pin}	LPTMR clock	—	25	MHz		
f _{LPTMR_ERCLK}	LPTMR external reference clock	_	16	MHz		
f _{FlexCAN_ERCLK}	FlexCAN external reference clock		8	MHz		

Table continues on the next page...

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Symbol	Description	Min.	Max.	Unit
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	20	
	Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	—	ns
	JTAG and CJTAG	25	—	ns
	Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	_	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	_	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z		25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	TRST assert time	100		ns
J14	TRST setup time (negation) to TCLK high	8		ns

Table 14. JTAG full voltage range electricals (continued)



Figure 5. Test clock input timing







6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	_	32.768	—	kHz	
f _{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	_	39.0625	kHz	
$\Delta_{fdco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	%f _{dco}	1
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	_	± 0.2	± 0.5	%f _{dco}	1
∆f _{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	_	+0.5/-0.7	± 3	%f _{dco}	1,
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		± 0.3	± 3	%f _{dco}	1
f _{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		4	_	MHz	
f _{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	_	5	MHz	
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00	(3/5) x f _{ints_t}			kHz	
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	(16/5) x f _{ints_t}			kHz	

Table 15. MCG specifications

Table continues on the next page...

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Symbol	Description		Min.	Тур.	Max.	Unit	Notes
	•	F	LL				
f _{fll_ref}	FLL reference free	luency range	31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fil, rof}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01)	40	41.94	50	MHz	
		Mid-high range (DRS=10)	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll ref}	80	83.89	100	MHz	
f _{dco_t_DMX32}	DCO output frequency	Low range (DRS=00) $732 \times f_{\text{fl} ref}$		23.99		MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fll_ref}	_	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fll_ref}	_	71.99	_	MHz	
		High range (DRS=11) 2929 × f _{fll_ref}	_	95.98	_	MHz	
J _{cyc_fll}	FLL period jitter		_	180	_	ps	
	 f_{DCO} = 48 MHz f_{DCO} = 98 MHz 		_	150	_		
t _{fll_acquire}	FLL target frequer	ncy acquisition time	—	—	1	ms	6
		P	ĹĹ				
f _{vco}	VCO operating fre	quency	48.0	—	100	MHz	
I _{pll}	PLL operating curr PLL @ 96 N 2 MHz, VDIV	rent IHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = / multiplier = 48)	_	1060	_	μA	7
I _{pll}	PLL operating curi PLL @ 48 N 2 MHz, VDIV	rent IHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = / multiplier = 24)	_	600	_	μA	7
f _{pll_ref}	PLL reference free	quency range	2.0		4.0	MHz	
J _{cyc_pll}	PLL period jitter (F	RMS)					8
	• f _{vco} = 48 MH	z	_	120	_	ps	
	• f _{vco} = 100 MHz		_	50	_	ps	
J _{acc_pll}	PLL accumulated	jitter over 1µs (RMS)					8
	• f _{vco} = 48 MH	z	_	1350	_	ps	
	• f _{vco} = 100 M	Hz	_	600	_	ps	
D _{lock}	Lock entry frequer	ncy tolerance	± 1.49		± 2.98	%	
D _{unl}	Lock exit frequenc	y tolerance	± 4.47		± 5.97	%	

Table continues on the next page ...



6.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes		
Program Flash								
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years			
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	—	years			
n _{nvmcycp}	Cycling endurance	10 K	50 K		cycles	2		

 Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40°C \leq T_i \leq 125°C.

6.4.2 EzPort switching specifications Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{SYS} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f _{SYS} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}		ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	_	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5		ns
EP5	EZP_D input valid to EZP_CK high (setup)	2		ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5		ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns





Figure 9. EzPort Timing Diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 25 and Table 26 are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 27 and Table 28.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.



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Figure 10. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics Table 26. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions ¹ .	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
	ADC	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/$
	asynchronous clock source	• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	† _{ADACK}
[†] ADACK		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter	for sample t	imes			
TUE	Total unadjusted	12-bit modes	_	±4	±6.8	LSB ⁴	5
	error	 <12-bit modes 	—	±1.4	±2.1		
DNL	Differential non-	12-bit modes	_	±0.7	-1.1 to +1.9	LSB ⁴	5
	linearity				-0.3 to 0.5		
		 <12-bit modes 	—	±0.2			
INL	Integral non-	12-bit modes	_	±1.0	-2.7 to +1.9	LSB ⁴	5
	linearity				-0.7 to +0.5		
		 <12-bit modes 	—	±0.5			
E _{FS}	Full-scale error	12-bit modes		-4	-5.4	LSB ⁴	V _{ADIN} =
		 <12-bit modes 	—	-1.4	-1.8		V _{DDA}
							5

Table continues on the next page...

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6.6.2 CMP and 6-bit DAC electrical specifications Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage	1.71	—	3.6	V
I _{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	_	_	200	μA
I _{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	_	—	20	μA
V _{AIN}	Analog input voltage	V _{SS} – 0.3	—	V _{DD}	V
V _{AIO}	Analog input offset voltage	_	—	20	mV
V _H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	_	5	—	mV
	• CR0[HYSTCTR] = 01	_	10	_	mV
	• CR0[HYSTCTR] = 10	_	20	_	mV
	 CR0[HYSTCTR] = 11 	_	30	_	mV
V _{CMPOh}	Output high	V _{DD} – 0.5	_	_	V
V _{CMPOI}	Output low	—	—	0.5	V
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	_	_	40	μs
I _{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6 V.

2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.

3. 1 LSB = $V_{reference}/64$



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Figure 15. Typical INL error vs. digital code



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Figure 16. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 32.	VREF full-range	operating	requirements
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Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
T _A	Temperature	Operating temperature range of the device		°C	
CL	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

 The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.



Figure 20. DSPI classic SPI timing — slave mode

6.8.4 Inter-Integrated Circuit Interface (I²C) timing Table 40. I²C timing

Characteristic	Symbol	Standa	rd Mode	Fast	Unit	
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f _{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	4	_	0.6	_	μs
LOW period of the SCL clock	t _{LOW}	4.7	_	1.3	—	μs
HIGH period of the SCL clock	t _{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	4.7	—	0.6	_	μs
Data hold time for I ₂ C bus devices	t _{HD} ; DAT	0 ¹	3.45 ²	0 ³	0.9 ¹	μs
Data set-up time	t _{SU} ; DAT	250 ⁴	_	100 ^{2, 5}	_	ns
Rise time of SDA and SCL signals	t _r	—	1000	20 +0.1C _b ⁶	300	ns
Fall time of SDA and SCL signals	t _f	—	300	20 +0.1C _b ⁵	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4		0.6		μs
Bus free time between STOP and START condition	t _{BUF}	4.7	_	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.

- 3. Input signal Slew = 10 ns and Output Load = 50 pF
- 4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
- 5. A Fast mode l²C bus device can be used in a Standard mode l2C bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard mode l²C bus specification) before the SCL line is released.

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6. C_b = total capacitance of the one bus line in pF.



Figure 21. Timing definition for fast and standard mode devices on the I²C bus

6.8.5 UART switching specifications

See General switching specifications.

6.8.6 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
		Card input clock		•	•
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f _{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t _{WL}	Clock low time	7	—	ns
SD3	t _{WH}	Clock high time	7	—	ns
SD4	t _{TLH}	Clock rise time	_	3	ns
SD5	t _{THL}	Clock fall time	—	3	ns
		SDHC output / card inputs SDHC_CMD, SDHC_DAT	(reference to	SDHC_CLK)	•
SD6	t _{OD}	SDHC output delay (output valid)	-5	8.3	ns
		SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to	SDHC_CLK)	
SD7	t _{ISU}	SDHC input setup time	5	_	ns
SD8	t _{IH}	SDHC input hold time	0	_	ns

Table 41. SDHC switching specifications



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Figure 22. SDHC timing

6.8.7 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.7.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	_	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	_	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns

 Table 42.
 I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Table continues on the next page...



Table 44. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



Figure 25. I2S/SAI timing — master modes

Table 45. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid			ns
	Multiple SAI Synchronous mode	_	24	
	All other modes	—	20.6	
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	_	ns

Table continues on the next page ...



rempheral operating requirements and behaviors





6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 48. TSI electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1
f _{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f _{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C _{REF}	Internal reference capacitor	_	1	—	pF	
V _{DELTA}	Oscillator delta voltage	—	500	—	mV	2, 5
I _{REF}	Reference oscillator current source base current • 2 μA setting (REFCHRG = 0)	_	2	3	μΑ	2, 6
	 32 µA setting (REFCHRG = 15) 	—	36	50		
I _{ELE}	Electrode oscillator current source base current • 2 µA setting (EXTCHRG = 0)	_	2	3	μΑ	2, 7
	• 32 µA setting (EXTCHRG = 15)	—	36	50		
Pres5	Electrode capacitance measurement precision	_	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	_	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution	_	_	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μs	12
I _{TSI_RUN}	Current added in run mode	—	55	—	μA	
I _{TSI_LP}	Low power mode current adder	_	1.3	2.5	μΑ	13