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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, SD, SPI, UART/USART
Peripherals	DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 31x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk30dx64vlk7r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • V_{DD} slew rate ≥ 5.7 kV/s • V_{DD} slew rate < 5.7 kV/s		300 1.7 V / (V _{DD} slew rate)	μs	1
	• VLLS1 → RUN	_	130	μs	
	• VLLS2 \rightarrow RUN		92	μs	
	• VLLS3 → RUN	_	92	μs	
	• LLS → RUN	—	5.9	μs	
	• VLPS → RUN		5.0	μs	
	• STOP \rightarrow RUN		5.0	μs	

Table 5. Power mode transition operating behaviors

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 1.8V • @ 3.0V		37 38	63 64	mA mA	2
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash • @ 1.8V • @ 3.0V • @ 25°C • @ 125°C	 	46 47 58	77 63 79	mA mA mA	3, 4
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	_	20	_	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	_	9		mA	5
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	_	1.12	—	mA	6

Table continues on the next page...



General



Figure 2. Run mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 144LQFP and144MAPBGA

Symbol	Description	Frequency band (MHz)	144LQFP	144MAPBGA	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	23	12	dBµV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	27	24	dBµV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	28	27	dBµV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	14	11	dBµV	
V _{RE_IEC}	IEC level	0.15–1000	К	К		2, 3

 Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions – TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.



- 3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
- 4. 75 pF load
- 5. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T _A	Ambient temperature	-40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	Unit	Notes
Single-layer (1s)	R _{eJA}	Thermal resistance, junction to ambient (natural convection)	47	°C/W	1
Four-layer (2s2p)	R _{ejA}	Thermal resistance, junction to ambient (natural convection)	35	°C/W	1
Single-layer (1s)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	37	°C/W	1
Four-layer (2s2p)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	29	°C/W	1
—	R _{eJB}	Thermal resistance, junction to board	20	°C/W	2
_	R _{θJC}	Thermal resistance, junction to case	9	°C/W	3

Table continues on the next page ...



6.3.2.2 Oscillator frequency specifications Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	_	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	_	8	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	_	32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	_	750		ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	_	250		ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	_	0.6	_	ms	•
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	_	1	_	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.

2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.

3. Proper PC board layout procedures must be followed to achieve specifications.

4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{BAT}	Supply voltage	1.71	—	3.6	V
R _F	Internal feedback resistor		100		MΩ

Table continues on the next page ...



6.4.1.2 Flash timing specifications — commands Table 21. Flash command timing specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	Read 1s Block execution time					
t _{rd1blk256k}	256 KB program/data flash	_	—	1.7	ms	
t _{rd1sec2k}	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t _{pgmchk}	Program Check execution time	—	—	45	μs	1
t _{rdrsrc}	Read Resource execution time	—	—	30	μs	1
t _{pgm4}	Program Longword execution time	—	65	145	μs	
	Erase Flash Block execution time					2
t _{ersblk256k}	256 KB program/data flash	_	122	985	ms	
t _{ersscr}	Erase Flash Sector execution time	_	14	114	ms	2
	Program Section execution time					
t _{pgmsec512}	 512 bytes flash 	_	2.4	—	ms	
t _{pgmsec1k}	• 1 KB flash	_	4.7	_	ms	
t _{pgmsec2k}	• 2 KB flash	_	9.3	_	ms	
t _{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t _{rdonce}	Read Once execution time	—	—	25	μs	1
t _{pgmonce}	Program Once execution time	—	65	_	μs	
t _{ersall}	Erase All Blocks execution time	_	250	2000	ms	2
t _{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
	Swap Control execution time					
t _{swapx01}	control code 0x01	_	200	_	μs	
t _{swapx02}	control code 0x02	-	70	150	μs	
t _{swapx04}	control code 0x04		70	150	μs	
t _{swapx08}	control code 0x08	_	_	30	μs	

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.4.1.3 Flash high voltage current behaviors Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA



6.6.1.1 16-bit ADC operating conditions Table 25. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} – V _{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} – V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	16-bit differential mode	VREFL	_	31/32 * VREFH	V	
		All other modes	VREFL	—	VREFH		
C _{ADIN}	Input capacitance	16-bit mode	_	8	10	pF	
		 8-bit / 10-bit / 12-bit modes 	_	4	5		
R _{ADIN}	Input resistance		_	2	5	kΩ	
R _{AS}	Analog source resistance	13-bit / 12-bit modes f _{ADCK} < 4 MHz	_	_	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0		18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	_	12.0	MHz	4
C _{rate}	ADC conversion	≤ 13-bit modes					5
	rate	No ADC hardware averaging	20.000	_	818.330	Ksps	
		Continuous conversions enabled, subsequent conversion time					
C _{rate}	ADC conversion	16-bit mode					5
		No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037		461.467	Ksps	

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.

- 2. DC potential difference.
- 3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Symbol	Description	Conditions ¹ .	Min.	Typ. ²	Max.	Unit	Notes
EQ	Quantization error	16-bit modes	_	-1 to 0	_	LSB ⁴	
		 ≤13-bit modes 	_	_	±0.5		
ENOB	Effective number	16-bit differential mode					6
	OT DITS	• Avg = 32	12.8	14.5	—	bits	
		• Avg = 4	11.9	13.8	_	bits	
		16-bit single-ended mode					
		• Avg = 32	12.2	13.9	_	bits	
		• Avg = 4	11.4	13.1	_	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02	2 × ENOB + 1	1.76	dB	
THD	Total harmonic distortion	16-bit differential modeAvg = 32	_	-94	_	dB	7
		16-bit single-ended modeAvg = 32	_	-85	_	dB	
SFDR	Spurious free dynamic range	16-bit differential modeAvg = 32	82	95	_	dB	7
		16-bit single-ended modeAvg = 32	78	90	_	dB	
E _{IL}	Input leakage error			$I_{In} \times R_{AS}$		mV	I _{In} = leakage current
							(refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

- 1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
- Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.



6.6.1.3 16-bit ADC with PGA operating conditions Table 27. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V _{REFPGA}	PGA ref voltage		VREF_OU T	VREF_OU T	VREF_OU T	V	2, 3
V _{ADIN}	Input voltage		V _{SSA}	_	V _{DDA}	V	
V _{CM}	Input Common Mode range		V _{SSA}	—	V _{DDA}	V	
R _{PGAD}	Differential input	Gain = 1, 2, 4, 8		128		kΩ	IN+ to IN- ⁴
	impedance	Gain = 16, 32	—	64	—		
		Gain = 64	_	32	—		
R _{AS}	Analog source resistance			100	_	Ω	5
T _S	ADC sampling time		1.25	_	_	μs	6
C _{rate}	ADC conversion rate	 ≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz 	18.484	_	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	_	250	Ksps	8

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 2. ADC must be configured to use the internal voltage reference (VREF_OUT)
- 3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
- 4. For single ended configurations the input impedance of the driven input is $R_{\text{PGAD}}/2$
- 5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
- The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
- 7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
- 8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1



Peripheral operating requirements and behaviors



Figure 13. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)



rempheral operating requirements and behaviors



Figure 14. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements Table 30. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
V _{DACR}	Reference voltage	1.13	3.6	V	1
T _A	Temperature	Operating temperature range of the device		°C	
CL	Output load capacitance	_	100	pF	2
١L	Output load current		1	mA	

1. The DAC reference can be selected to be V_{DDA} or the voltage output of the VREF module (VREF_OUT)

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC



6.6.3.2 12-bit DAC operating behaviors Table 31. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL}	Supply current — low-power mode	_	_	330	μΑ	
I _{DDA_DACH}	Supply current — high-speed mode		_	1200	μΑ	
tDACLP	Full-scale settling time (0x080 to 0xF7F) — low-power mode	_	100	200	μs	1
t _{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode		0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	_	_	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	_	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode	_	_	±8	LSB	2
DNL	Differential non-linearity error — V _{DACR} > 2 V	_	_	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT	_	—	±1	LSB	4
VOFFSET	Offset error	_	±0.4	±0.8	%FSR	5
E _G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} > = 2.4 V$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T _{GE}	Temperature coefficient gain error	_	0.000421	_	%FSR/C	
Rop	Output resistance load = $3 \text{ k}\Omega$	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP _{HP})	1.2	1.7			
	Low power (SP _{LP})	0.05	0.12	—		
СТ	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	 High power (SP_{HP}) 	550	_	—		
	Low power (SP _{LP})	40	_	—		

1. Settling within ±1 LSB

- 2. The INL is measured for 0+100mV to V_{DACR} -100 mV
- 3. The DNL is measured for 0+100 mV to V_{DACR} -100 mV
- 4. The DNL is measured for 0+100mV to $V_{DACR}\mbox{--}100$ mV with $V_{DDA}\mbox{-}2.4V$
- 5. Calculated by a best fit curve from $V_{\text{SS}}\text{+}100\mbox{ mV}$ to $V_{\text{DACR}}\text{-}100\mbox{ mV}$
- 6. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_CO:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C



Num	Description	Min.	Max.	Unit	Notes
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) - 4	(t _{SCK/2)} + 4	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	_	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	_	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

Table 38. Master mode DSPI timing (full voltage range) (continued)

- 1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
- 2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
- 3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 19. DSPI classic SPI timing — master mode

Table 39. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	_	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t _{BUS}		ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) - 4	(t _{SCK/2)} + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	24	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2		ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven		19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns



Figure 20. DSPI classic SPI timing — slave mode

6.8.4 Inter-Integrated Circuit Interface (I²C) timing Table 40. I²C timing

Characteristic	Symbol	Standa	rd Mode	Fast	Unit	
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f _{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	4	_	0.6	_	μs
LOW period of the SCL clock	t _{LOW}	4.7	_	1.3	—	μs
HIGH period of the SCL clock	t _{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	4.7	—	0.6	_	μs
Data hold time for I ₂ C bus devices	t _{HD} ; DAT	0 ¹	3.45 ²	0 ³	0.9 ¹	μs
Data set-up time	t _{SU} ; DAT	250 ⁴	_	100 ^{2, 5}	_	ns
Rise time of SDA and SCL signals	t _r	—	1000	20 +0.1C _b ⁶	300	ns
Fall time of SDA and SCL signals	t _f	—	300	20 +0.1C _b ⁵	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4		0.6		μs
Bus free time between STOP and START condition	t _{BUF}	4.7	_	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.

- 3. Input signal Slew = 10 ns and Output Load = 50 pF
- 4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
- 5. A Fast mode l²C bus device can be used in a Standard mode l2C bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard mode l²C bus specification) before the SCL line is released.





Figure 22. SDHC timing

6.8.7 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.7.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	_	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	_	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns

 Table 42.
 I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Table continues on the next page...



Table 43. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	_	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



Figure 24. I2S/SAI timing — slave modes

6.8.7.2 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

 Table 44.
 I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	_	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	_	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0		ns

Table continues on the next page...



Table 46. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



Figure 27. I2S/SAI timing — master modes

Table 47. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



Symbol Description Min. Unit Notes Typ. Max. VIREG current adder - RVEN = 1 1 4 IVIREG μΑ **RBIAS** current adder IRBIAS 10 μΑ • LADJ = 10 or 11 — High load (LCD glass 1 capacitance \leq 8000 pF) μΑ LADJ = 00 or 01 — Low load (LCD glass capacitance \leq 2000 pF) **RBIAS** resistor values R_{RBIAS} LADJ = 10 or 11 — High load (LCD glass 0.28 MΩ capacitance $\leq 8000 \text{ pF}$) • LADJ = 00 or 01 — Low load (LCD glass 2.98 MΩ capacitance $\leq 2000 \text{ pF}$) VLL2 VLL2 voltage HREFSEL = 0 2.0 - 5% 2.0 ٧ • HREFSEL = 1 3.3 - 5% 3.3 ۷ VLL3 VLL3 voltage HREFSEL = 0 3.0 – 5% 3.0 ۷ HREFSEL = 1 5 – 5% 5 V

Table 49.	LCD	electricals	(continued))
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1. The actual value used could vary with tolerance.

2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.

3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V

4. 2000 pF load LCD, 32 Hz frame frequency

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number					
100-pin LQFP	98ASS23308W					
104-pin MAPBGA	98ASA00344D					



8 Pinout

8.1 K30 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

100 LQFP	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1	FB_AD27	I2C1_SDA	RTC_CLKOUT	
2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0	FB_AD26	I2C1_SCL	SPI1_SIN	
3	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK	FB_AD25			
4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD	FB_AD24		SPI1_SOUT	
5	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3	FB_CS3_b/ FB_BE7_0_b	FB_TA_b		
6	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2	FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b			
7	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK	FB_ALE/ FB_CS1_b/ FB_TS_b			
8	VDD	VDD	VDD								
9	VSS	VSS	VSS								
10	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
11	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
12	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
13	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				
14	ADC0_DP1	ADC0_DP1	ADC0_DP1								
15	ADC0_DM1	ADC0_DM1	ADC0_DM1								
16	ADC1_DP1	ADC1_DP1	ADC1_DP1								
17	ADC1_DM1	ADC1_DM1	ADC1_DM1								
18	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
19	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
20	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								



100 LQFP	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
21	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
22	VDDA	VDDA	VDDA								
23	VREFH	VREFH	VREFH								
24	VREFL	VREFL	VREFL								
25	VSSA	VSSA	VSSA								
26	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
27	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
28	XTAL32	XTAL32	XTAL32								
29	EXTAL32	EXTAL32	EXTAL32								
30	VBAT	VBAT	VBAT								
31	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	UART4_TX			EWM_OUT_b		
32	PTE25	ADC0_SE18	ADC0_SE18	PTE25	CAN1_RX	UART4_RX		FB_AD23	EWM_IN		
33	PTE26	DISABLED		PTE26		UART4_CTS_b		FB_AD22	RTC_CLKOUT		
34	PTAO	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
35	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
36	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
37	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
38	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
39	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_TX_BCLK	JTAG_TRST_b	
40	VDD	VDD	VDD								
41	VSS	VSS	VSS								
42	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b	I2S0_TXD0	FTM1_QD_ PHA	
43	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	12S0_TX_FS	FTM1_QD_ PHB	
44	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX		FB_AD31	I2S0_RX_BCLK	I2S0_TXD1	
45	PTA15	DISABLED		PTA15	SPI0_SCK	UARTO_RX		FB_AD30	I2S0_RXD0		
46	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_ b/ UART0_COL_b		FB_AD29	I2S0_RX_FS	12S0_RXD1	
47	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b		FB_AD28	I2S0_MCLK		



100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
100	PTD7	LCD_P47	LCD_P47	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1	LCD_P47	

8.2 K30 pinouts

The figure below shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Pinout