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Details

Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	12
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	16-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qg44cpbe

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7.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08, all memory, status and control registers, and input/output (I/O) ports share a single 64-Kbyte linear address space so a 16-bit binary address can uniquely identify any memory location. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

7.3.1 Inherent Addressing Mode (INH)

In this addressing mode, operands needed to complete the instruction (if any) are located within CPU registers so the CPU does not need to access memory to get any operands.

7.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed 8-bit offset value is located in the memory location immediately following the opcode. During execution, if the branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address.

7.3.3 Immediate Addressing Mode (IMM)

In immediate addressing mode, the operand needed to complete the instruction is included in the object code immediately following the instruction opcode in memory. In the case of a 16-bit immediate operand, the high-order byte is located in the next memory location after the opcode, and the low-order byte is located in the next memory location after that.

7.3.4 Direct Addressing Mode (DIR)

In direct addressing mode, the instruction includes the low-order eight bits of an address in the direct page (0x0000-0x00FF). During execution a 16-bit address is formed by concatenating an implied 0x00 for the high-order half of the address and the direct address from the instruction to get the 16-bit address where the desired operand is located. This is faster and more memory efficient than specifying a complete 16-bit address for the operand.



Chapter 7 Central Processor Unit (S08CPUV2)

Bit-Mani	pulation	Branch	Rea	ad-Modify-Write	Control			Register/	Memory		
				9E60 6 NEG 3 SP1					9ED0 5 SUB 4 SP2	9EE0 4 SUB 3 SP1	
				9E61 6 CBEQ 4 SP1					9ED1 5 CMP 4 SP2	9EE1 4 CMP 3 SP1	
									9ED2 5 SBC 4 SP2	9EE2 4 SBC 3 SP1	
				9E63 6 COM 3 SP1					9ED3 5 CPX 4 SP2	9EE3 4 CPX 3 SP1	9EF3 6 CPHX 3 SP1
				9E64 6 LSR 3 SP1					9ED4 5 AND 4 SP2	9EE4 4 AND 3 SP1	
									9ED5 5 BIT 4 SP2	9EE5 4 BIT 3 SP1	
				9E66 6 ROR 3 SP1					9ED6 5 LDA 4 SP2	9EE6 4 LDA 3 SP1	
				9E67 6 ASR 3 SP1					9ED7 5 STA 4 SP2	9EE7 4 STA 3 SP1	
				9E68 6 LSL 3 SP1					9ED8 5 EOR 4 SP2	9EE8 4 EOR 3 SP1	
				9E69 6 ROL 3 SP1					9ED9 5 ADC 4 SP2	9EE9 4 ADC 3 SP1	
				9E6A 6 DEC 3 SP1					9EDA 5 ORA 4 SP2	9EEA 4 ORA 3 SP1	
				9E6B 8 DBNZ 4 SP1					9EDB 5 ADD 4 SP2	9EEB 4 ADD 3 SP1	
				9E6C 6 INC 3 SP1							
				9E6D 5 TST 3 SP1							
						9EAE 5 LDHX 2 IX	9EBE 6 LDHX 4 IX2	9ECE 5 LDHX 3 IX1	9EDE 5 LDX 4 SP2	9EEE 4 LDX 3 SP1	9EFE 5 LDHX 3 SP1
				9E6F 6 CLR 3 SP1					9EDF 5 STX 4 SP2	9EEF 4 STX 3 SP1	9EFF 5 STHX 3 SP1

Table 7-3. Opcode Map (Sheet 2 of 2)

Inherent Immediate Direct Extended DIR to DIR IX+ to DIR REL IX IX1 IX2 IMD DIX+ INH IMM DIR EXT DD IX+D

Relative Indexed, No Offset Indexed, 8-Bit Offset Indexed, 16-Bit Offset IMM to DIR DIR to IX+

Stack Pointer, 8-Bit Offset Stack Pointer, 16-Bit Offset Indexed, No Offset with Post Increment Indexed, 1-Byte Offset with Post Increment

SP1 SP2 IX+

IX1+

Note: All Sheet 2 Opcodes are Preceded by the Page 2 Prebyte (9E)

Prebyte (9E) and Opcode in Hexadecimal 9E60 6 NEG Number of Bytes 3 SP1 Addressing Mode



8.1.3 Features

The ACMP has the following features:

- Full rail-to-rail supply operation.
- Less than 40 mV of input offset.
- Less than 15 mV of hysteresis.
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output.
- Option to compare to fixed internal bandgap reference voltage.
- Option to allow comparator output to be visible on a pin, ACMPO.

8.1.4 Modes of Operation

This section defines the ACMP operation in wait, stop, and background debug modes.

8.1.4.1 ACMP in Wait Mode

The ACMP continues to run in wait mode if enabled before executing the WAIT instruction. Therefore, the ACMP can be used to bring the MCU out of wait mode if the ACMP interrupt, ACIE, is enabled. For lowest possible current consumption, the ACMP should be disabled by software if not required as an interrupt source during wait mode.

8.1.4.2 ACMP in Stop Modes

The ACMP is disabled in all stop modes, regardless of the settings before executing the STOP instruction. Therefore, the ACMP cannot be used as a wake up source from stop modes.

During either stop1 or stop2 mode, the ACMP module will be fully powered down. Upon wake-up from stop1 or stop2 mode, the ACMP module will be in the reset state.

During stop3 mode, clocks to the ACMP module are halted. No registers are affected. In addition, the ACMP comparator circuit will enter a low power state. No compare operation will occur while in stop3.

If stop3 is exited with a reset, the ACMP will be put into its reset state. If stop3 is exited with an interrupt, the ACMP continues from the state it was in when stop3 was entered.

8.1.4.3 ACMP in Active Background Mode

When the microcontroller is in active background mode, the ACMP will continue to operate normally.

8.1.5 Block Diagram

The block diagram for the analog comparator module is shown Figure 8-2.



9.1.1 Module Configurations

This section provides device-specific information for configuring the ADC on MC9S08QG8/4 devices.

9.1.1.1 Analog Supply and Voltage Reference Connections

The V_{DDAD} and V_{REFH} sources for the ADC are internally connected to the V_{DD} pin. The V_{SSAD} and V_{REFL} sources for the ADC are internally connected to the V_{SS} pin.

9.1.1.2 Channel Assignments

The ADC channel assignments for the MC9S08QG8/4 devices are shown in Table 9-1. Reserved channels convert to an unknown value.

ADCH	Channel	Input	Pin Control
00000	AD0	PTA0/ADP0	ADPC0
00001	AD1	PTA1/ADP1	ADPC1
00010	AD2	PTA2/ADP2	ADPC2
00011	AD3	PTA3/ADP3	ADPC3
00100	AD4	PTB0/ADP4	ADPC4
00101	AD5	PTB1/ADP5	ADPC5
00110	AD6	PTB2/ADP6	ADPC6
00111	AD7	PTB3/ADP7	ADPC7
01000	AD8	V _{SS}	N/A
01001	AD9	V _{SS}	N/A
01010	AD10	V _{SS}	N/A
01011	AD11	V _{SS}	N/A
01100	AD12	V _{SS}	N/A
01101	AD13	V _{SS}	N/A
01110	AD14	V _{SS}	N/A
01111	AD15	V _{SS}	N/A

Table 9-1. ADC Channel Assignment

ADCH	Channel	Input	Pin Control
10000	AD16	V _{SS}	N/A
10001	AD17	V _{SS}	N/A
10010	AD18	V _{SS}	N/A
10011	AD19	V _{SS}	N/A
10100	AD20	V _{SS}	N/A
10101	AD21	V _{SS}	N/A
10110	AD22	Reserved	N/A
10111	AD23	Reserved	N/A
11000	AD24	Reserved	N/A
11001	AD25	Reserved	N/A
11010	AD26	Temperature Sensor ¹	N/A
11011	AD27	Internal Bandgap	N/A
11100	—	Reserved	N/A
11101	V _{REFH}	V _{DD}	N/A
11110	V _{REFL}	V _{SS}	N/A
11111	Module Disabled	None	N/A

¹ For information, see Section 9.1.1.6, "Temperature Sensor."

NOTE

Selecting the internal bandgap channel requires BGBE =1 in SPMSC1; see Section 5.8.8, "System Power Management Status and Control 1 Register (SPMSC1)." For the value of the bandgap voltage reference see Section A.5, "DC Characteristics."



are too fast, then the clock must be divided to the appropriate frequency. This divider is specified by the ADIV bits and can be divide-by 1, 2, 4, or 8.

9.4.2 Input Select and Pin Control

The pin control registers (APCTL3, APCTL2, and APCTL1) are used to disable the I/O port control of the pins used as analog inputs. When a pin control register bit is set, the following conditions are forced for the associated MCU pin:

- The output buffer is forced to its high impedance state.
- The input buffer is disabled. A read of the I/O port returns a zero for any pin with its input buffer disabled.
- The pullup is disabled.

9.4.3 Hardware Trigger

The ADC module has a selectable asynchronous hardware conversion trigger, ADHWT, that is enabled when the ADTRG bit is set. This source is not available on all MCUs. Consult the module introduction for information on the ADHWT source specific to this MCU.

When ADHWT source is available and hardware trigger is enabled (ADTRG=1), a conversion is initiated on the rising edge of ADHWT. If a conversion is in progress when a rising edge occurs, the rising edge is ignored. In continuous convert configuration, only the initial rising edge to launch continuous conversions is observed. The hardware trigger function operates in conjunction with any of the conversion modes and configurations.

9.4.4 Conversion Control

Conversions can be performed in either 10-bit mode or 8-bit mode as determined by the MODE bits. Conversions can be initiated by either a software or hardware trigger. In addition, the ADC module can be configured for low power operation, long sample time, continuous conversion, and automatic compare of the conversion result to a software determined compare value.

9.4.4.1 Initiating Conversions

A conversion is initiated:

- Following a write to ADCSC1 (with ADCH bits not all 1s) if software triggered operation is selected.
- Following a hardware trigger (ADHWT) event if hardware triggered operation is selected.
- Following the transfer of the result to the data registers when continuous conversion is enabled.

If continuous conversions are enabled a new conversion is automatically initiated after the completion of the current conversion. In software triggered operation, continuous conversions begin after ADCSC1 is written and continue until aborted. In hardware triggered operation, continuous conversions begin after a hardware trigger event and continue until aborted.

Analog-to-Digital Converter (S08ADC10V1)

- 2. Update status and control register 2 (ADCSC2) to select the conversion trigger (hardware or software) and compare function options, if enabled.
- 3. Update status and control register 1 (ADCSC1) to select whether conversions will be continuous or completed only once, and to enable or disable conversion complete interrupts. The input channel on which conversions will be performed is also selected here.

9.5.1.2 Pseudo — Code Example

In this example, the ADC module will be set up with interrupts enabled to perform a single 10-bit conversion at low power with a long sample time on input channel 1, where the internal ADCK clock will be derived from the bus clock divided by 1.

ADCCFG = 0x98 (%10011000)

Bit 7	ADLPC	1	Configures for low power (lowers maximum clock speed)
Bit 6:5	ADIV	00	Sets the ADCK to the input clock \div 1
Bit 4	ADLSMP	1	Configures for long sample time
Bit 3:2	MODE	10	Sets mode at 10-bit conversions
Bit 1:0	ADICLK	00	Selects bus clock as input clock source

ADCSC2 = 0x00 (%00000000)

Bit 7	ADACT	0	Flag indicates if a conversion is in progress
Bit 6	ADTRG	0	Software trigger selected
Bit 5	ACFE	0	Compare function disabled
Bit 4	ACFGT	0	Not used in this example
Bit 3:2		00	Unimplemented or reserved, always reads zero
Bit 1:0		00	Reserved for Freescale's internal use; always write zero

ADCSC1 = 0x41 (%01000001)

Bit 7	COCO	0	Read-only flag which is set when a conversion completes
Bit 6	AIEN	1	Conversion complete interrupt enabled
Bit 5	ADCO	0	One conversion only (continuous conversions disabled)
Bit 4:0	ADCH	00001	Input channel 1 selected as ADC input channel

ADCRH/L = 0xxx

Holds results of conversion. Read high byte (ADCRH) before low byte (ADCRL) so that conversion data cannot be overwritten with data from the next conversion.

ADCCVH/L = 0xxx

Holds compare value when compare function enabled

APCTL1=0x02

AD1 pin I/O control disabled. All other AD pins remain general purpose I/O pins

APCTL2=0x00

All other AD pins remain general purpose I/O pins



Internal Clock Source (S08ICSV1)

times the filter frequency, as selected by the RDIV bits, so that the ICSLCLK will be available for BDC communications, and the external reference clock is enabled.

10.4.1.6 FLL Bypassed External Low Power (FBELP)

The FLL bypassed external low power (FBELP) mode is entered when all the following conditions occur:

- CLKS bits are written to 10.
- IREFS bit is written to 0.
- BDM mode is not active and LP bit is written to 1.

In FLL bypassed external low power mode, the ICSOUT clock is derived from the external reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications. The external reference clock is enabled.

10.4.1.7 Stop

ICS stop mode is entered whenever the MCU enters stop. In this mode, all ICS clock signals are stopped except in the following cases:

ICSIRCLK will be active in stop mode when all the following conditions occur:

- IRCLKEN bit is written to 1
- IREFSTEN bit is written to 1

ICSERCLK will be active in stop mode when all the following conditions occur:

- ERCLKEN bit is written to 1
- EREFSTEN bit is written to 1

10.4.2 Mode Switching

When switching between FLL engaged internal (FEI) and FLL engaged external (FEE) modes the IREFS bit can be changed at anytime, but the RDIV bits must be changed simultaneously so that the resulting frequency stays in the range of 31.25 kHz to 39.0625 kHz. After a change in the IREFS value the FLL will begin locking again after a few full cycles of the resulting divided reference frequency.

The CLKS bits can also be changed at anytime, but the RDIV bits must be changed simultaneously so that the resulting frequency stays in the range of 31.25 kHz to 39.0625 kHz. The actual switch to the newly selected clock will not occur until after a few full cycles of the new clock. If the newly selected clock is not available, the previous clock will remain selected.

10.4.3 Bus Frequency Divider

The BDIV bits can be changed at anytime and the actual switch to the new frequency will occur immediately.





14.2 Register Definition

The SCI has eight 8-bit registers to control baud rate, select SCI options, report SCI status, and for transmit/receive data.

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all SCI registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

14.2.1 SCI Baud Rate Registers (SCIBDH, SCIBDL)

This pair of registers controls the prescale divisor for SCI baud rate generation. To update the 13-bit baud rate setting [SBR12:SBR0], first write to SCIBDH to buffer the high half of the new value and then write to SCIBDL. The working value in SCIBDH does not change until SCIBDL is written.

SCIBDL is reset to a non-zero value, so after reset the baud rate generator remains disabled until the first time the receiver or transmitter is enabled (RE or TE bits in SCIC2 are written to 1).



Figure 14-5. SCI Baud Rate Register (SCIBDH)

Table 14-1. SCIBDH Register Field Descriptions

Field	Description
4:0 SBR[12:8]	Baud Rate Modulo Divisor — These 13 bits are referred to collectively as BR, and they set the modulo divide rate for the SCI baud rate generator. When BR = 0, the SCI baud rate generator is disabled to reduce supply
02.1[12.0]	current. When $BR = 1$ to 8191, the SCI baud rate = BUSCLK/(16×BR). See also BR bits in Table 14-2.



Figure 14-6. SCI Baud Rate Register (SCIBDL)



14.2.5 SCI Status Register 2 (SCIS2)

This register has one read-only status flag. Writes have no effect.



Figure 14-10. SCI Status Register 2 (SCIS2)

Table 14-6. SCIS2 Register Field Descriptions

Field	Description
2 BRK13	 Break Character Length — BRK13 is used to select a longer break character length. Detection of a framing error is not affected by the state of this bit. 0 Break character is 10 bit times (11 if M = 1) 1 Break character is 13 bit times (14 if M = 1)
0 RAF	 Receiver Active Flag — RAF is set when the SCI receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. This status flag can be used to check whether an SCI character is being received before instructing the MCU to go to stop mode. SCI receiver idle waiting for a start bit. SCI receiver active (RxD input not idle).

14.2.6 SCI Control Register 3 (SCIC3)



Figure 14-11. SCI Control Register 3 (SCIC3)

Table 14-7. SCIC3 Register Field Descriptions

Field	Description
7 R8	Ninth Data Bit for Receiver — When the SCI is configured for 9-bit data ($M = 1$), R8 can be thought of as a ninth receive data bit to the left of the MSB of the buffered data in the SCID register. When reading 9-bit data, read R8 before reading SCID because reading SCID completes automatic flag clearing sequences which could allow R8 and SCID to be overwritten with new data.
6 T8	Ninth Data Bit for Transmitter — When the SCI is configured for 9-bit data ($M = 1$), T8 may be thought of as a ninth transmit data bit to the left of the MSB of the data in the SCID register. When writing 9-bit data, the entire 9-bit value is transferred to the SCI shift register after SCID is written so T8 should be written (if it needs to change from its previous value) before SCID is written. If T8 does not need to change in the new value (such as when it is used to generate mark or space parity), it need not be written each time SCID is written.



Serial Peripheral Interface (S08SPIV3)



15.2 External Signal Description

The SPI optionally shares four port pins. The function of these pins depends on the settings of SPI control bits. When the SPI is disabled (SPE = 0), these four pins revert to being general-purpose port I/O pins that are not controlled by the SPI.

15.2.1 SPSCK — SPI Serial Clock

When the SPI is enabled as a slave, this pin is the serial clock input. When the SPI is enabled as a master, this pin is the serial clock output.

15.2.2 MOSI — Master Data Out, Slave Data In

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data output. When the SPI is enabled as a slave and SPC0 = 0, this pin is the serial data input. If SPC0 = 1 to select single-wire bidirectional mode, and master mode is selected, this pin becomes the bidirectional data I/O pin (MOMI). Also, the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE = 0) or an output (BIDIROE = 1). If SPC0 = 1 and slave mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

15.2.3 MISO — Master Data In, Slave Data Out

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data input. When the SPI is enabled as a slave and SPC0 = 0, this pin is the serial data output. If SPC0 = 1 to select single-wire bidirectional mode, and slave mode is selected, this pin becomes the bidirectional data I/O pin (SISO) and the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE = 0) or an output (BIDIROE = 1). If SPC0 = 1 and master mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

15.2.4 SS — Slave Select

When the SPI is enabled as a slave, this pin is the low-true slave select input. When the SPI is enabled as a master and mode fault enable is off (MODFEN = 0), this pin is not used by the SPI and reverts to being a general-purpose port I/O pin. When the SPI is enabled as a master and MODFEN = 1, the slave select output enable bit determines whether this pin acts as the mode fault input (SSOE = 0) or as the slave select output (SSOE = 1).



15.3 Modes of Operation

15.3.1 SPI in Stop Modes

The SPI is disabled in all stop modes, regardless of the settings before executing the STOP instruction. During either stop1 or stop2 mode, the SPI module will be fully powered down. Upon wake-up from stop1 or stop2 mode, the SPI module will be in the reset state. During stop3 mode, clocks to the SPI module are halted. No registers are affected. If stop3 is exited with a reset, the SPI will be put into its reset state. If stop3 is exited with an interrupt, the SPI continues from the state it was in when stop3 was entered.

15.4 Register Definition

The SPI has five 8-bit registers to select SPI options, control baud rate, report SPI status, and for transmit/receive data.

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all SPI registers. This section refers to registers and control bits only by their names, and a Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

15.4.1 SPI Control Register 1 (SPIC1)

This read/write register includes the SPI enable control, interrupt enables, and configuration options.



Figure 15-5. SPI Control Register 1 (SPIC1)

Table	15-1.	SPIC1	Field	Descriptions
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Field	Description
7 SPIE	 SPI Interrupt Enable (for SPRF and MODF) — This is the interrupt enable for SPI receive buffer full (SPRF) and mode fault (MODF) events. Interrupts from SPRF and MODF inhibited (use polling) When SPRF or MODF is 1, request a hardware interrupt
6 SPE	 SPI System Enable — Disabling the SPI halts any transfer that is in progress, clears data buffers, and initializes internal state machines. SPRF is cleared and SPTEF is set to indicate the SPI transmit data buffer is empty. SPI system inactive SPI system enabled
5 SPTIE	 SPI Transmit Interrupt Enable — This is the interrupt enable bit for SPI transmit buffer empty (SPTEF). Interrupts from SPTEF inhibited (use polling) When SPTEF is 1, hardware interrupt requested

NP

Timer/Pulse-Width Modulator (S08TPMV2)



Figure 16-2. TPM Block Diagram

The central component of the TPM is the 16-bit counter that can operate as a free-running counter, a modulo counter, or an up-/down-counter when the TPM is configured for center-aligned PWM. The TPM counter (when operating in normal up-counting mode) provides the timing reference for the input capture, output compare, and edge-aligned PWM functions. The timer counter modulo registers, TPMMODH:TPMMODL, control the modulo value of the counter. (The values 0x0000 or 0xFFFF effectively make the counter free running.) Software can read the counter value at any time without affecting the counting sequence. Any write to either byte of the TPMCNT counter resets the counter regardless of the data value written.



CLKSB:CLKSA	TPM Clock Source to Prescaler Input
0:0	No clock selected (TPM disabled)
0:1	Bus rate clock (BUSCLK)
1:0	Fixed system clock (XCLK)
1:1	External source (TPMCLK) ^{1,2}

Table 16-2. TPM Clock Source Selection

¹ The maximum frequency that is allowed as an external clock is one-fourth of the bus frequency.

² If the external clock input is shared with channel n and is selected as the TPM clock source, the corresponding ELSnB:ELSnA control bits should be set to 0:0 so channel n does not try to use the same pin for a conflicting function.

PS2:PS1:PS0	TPM Clock Source Divided-By
0:0:0	1
0:0:1	2
0:1:0	4
0:1:1	8
1:0:0	16
1:0:1	32
1:1:0	64
1:1:1	128

Table 16-3. Prescale Divisor Selection

16.3.2 Timer Counter Registers (TPMCNTH:TPMCNTL)

The two read-only TPM counter registers contain the high and low bytes of the value in the TPM counter. Reading either byte (TPMCNTH or TPMCNTL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. This allows coherent 16-bit reads in either order. The coherency mechanism is automatically restarted by an MCU reset, a write of any value to TPMCNTH or TPMCNTL, or any write to the timer status/control register (TPMSC).

Reset clears the TPM counter registers.





Timer/Pulse-Width Modulator (S08TPMV2)



When background mode is active, the timer counter and the coherency mechanism are frozen such that the buffer latches remain in the state they were in when the background mode became active even if one or both bytes of the counter are read while background mode is active.

16.3.3 Timer Counter Modulo Registers (TPMMODH:TPMMODL)

The read/write TPM modulo registers contain the modulo value for the TPM counter. After the TPM counter reaches the modulo value, the TPM counter resumes counting from 0x0000 at the next clock (CPWMS = 0) or starts counting down (CPWMS = 1), and the overflow flag (TOF) becomes set. Writing to TPMMODH or TPMMODL inhibits TOF and overflow interrupts until the other byte is written. Reset sets the TPM counter modulo registers to 0x0000, which results in a free-running timer counter (modulo disabled).



It is good practice to wait for an overflow interrupt so both bytes of the modulo register can be written well before a new overflow. An alternative approach is to reset the TPM counter before writing to the TPM modulo registers to avoid confusion about when the first counter overflow will occur.



Development Support

17.1.2 Features

Features of the BDC module include:

- Single pin for mode selection and background communications
- BDC registers are not located in the memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC
- Oscillator runs in stop mode, if BDC enabled
- COP watchdog disabled while in active background mode

Features of the ICE system include:

- Two trigger comparators: Two address + read/write (R/W) or one full address + data + R/W
- Flexible 8-word by 16-bit FIFO (first-in, first-out) buffer for capture information:
 - Change-of-flow addresses or
 - Event-only data
- Two types of breakpoints:
 - Tag breakpoints for instruction opcodes
 - Force breakpoints for any address access
- Nine trigger modes:
 - Basic: A-only, A OR B
 - Sequence: A then B
 - Full: A AND B data, A AND NOT B data
 - Event (store data): Event-only B, A then event-only B
 - Range: Inside range (A \leq address \leq B), outside range (address < A or address > B)

17.2 Background Debug Controller (BDC)

All MCUs in the HCS08 Family contain a single-wire background debug interface that supports in-circuit programming of on-chip nonvolatile memory and sophisticated non-intrusive debug capabilities. Unlike debug interfaces on earlier 8-bit MCUs, this system does not interfere with normal application resources. It does not use any user memory or locations in the memory map and does not share any on-chip peripherals.

BDC commands are divided into two groups:

• Active background mode commands require that the target MCU is in active background mode (the user program is not running). Active background mode commands allow the CPU registers to be





Figure 17-2. BDC Host-to-Target Serial Bit Timing

Figure 17-3 shows the host receiving a logic 1 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target MCU. The host holds the BKGD pin low long enough for the target to recognize it (at least two target BDC cycles). The host must release the low drive before the target MCU drives a brief active-high speedup pulse seven cycles after the perceived start of the bit time. The host should sample the bit level about 10 cycles after it started the bit time.



Figure 17-3. BDC Target-to-Host Serial Bit Timing (Logic 1)



Characteristic		Min	Тур	Мах	Unit
Resolution of trimmed DCO output frequency at fixed voltage and temperature ⁴		_	±0.1	± 0.2	%f _{dco}
Total deviation of DCO output from trimmed frequency: ³ At 8MHz over full voltage and temperature range (M Suffix)		_	-1.5 to ±0.5	± 3	
At 8MHz over full voltage and temperature rang (C Suffix)	Δf_{dco_t}	—	-1.0 to ±0.5	± 2	%f _{dco}
At 8MHz and 3.6V from 0 to 70° C (C Suffix)		—	±0.5	± 1	
FLL acquisition time ^{4,6}	t _{Acquire}			1.5	ms
Long term jitter of DCO output clock (averaged over 2-ms interval) ⁷	C _{Jitter}		0.02	0.2	%f _{dco}

Table A-8. XOSC and ICS Specifications (Temperature Range = -40 to 125°C Ambient)

¹ When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

² See crystal or resonator manufacturer's recommendation.

- ³ This parameter is characterized and not tested on each device.
- ⁴ Proper PC board layout procedures must be followed to achieve specifications.
- ⁵ TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).
- ⁶ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- ⁷ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.



Figure A-7. Typical Crystal or Resonator Circuit



A.11 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Characteristic	Symbol	Min	Typical	Мах	Unit
Supply voltage for program/erase:					
T ≤ 85°C	V _{prog/erase}	1.8	—	3.6	V
T > 85 °C		2.1	—	3.6	
Supply voltage for read operation	V _{Read}	1.8	—	3.6	V
Internal FCLK frequency ¹	f _{FCLK}	150	—	200	kHz
Internal FCLK period (1/FCLK)	t _{Fcyc}	5	—	6.67	μS
Byte program time (random location) ⁽²⁾	t _{prog}		9		t _{Fcyc}
Byte program time (burst mode) ⁽²⁾	t _{Burst}		4		t _{Fcyc}
Page erase time ²	t _{Page}		4000		t _{Fcyc}
Mass erase time ⁽²⁾	t _{Mass}		20,000		t _{Fcyc}
Program/erase endurance ³					
T_L to $T_H = -40^{\circ}C$ to + 125°C		10,000	—	—	cycles
T = 25°C			100,000	—	
Data retention ⁴	t _{D_ret}	15	100	—	years

Table	A-15.	FLASH	Characteristics
Table	A-13.	LAOII	onaracteristics

¹ The frequency of this clock is controlled by a software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

³ **Typical endurance for FLASH** was evaluated for this product family on the 9S12Dx64. For additional information on how Motorola defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

⁴ Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Motorola defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*







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