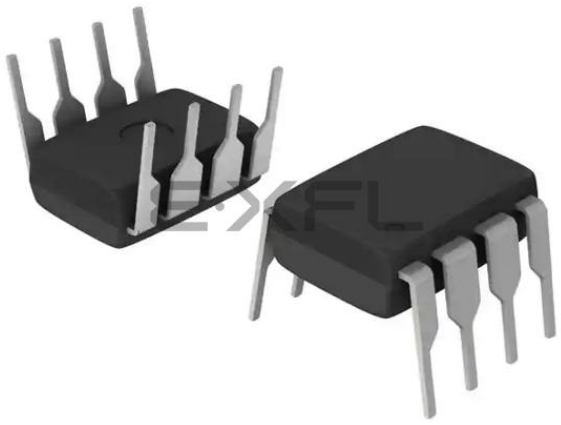

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	4
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qg4cpae

MC9S08QG8
MC9S08QG4

Data Sheet

HCS08
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MC9S08QG8
Rev. 5
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Chapter 10
Internal Clock Source (S08ICSV1)

Chapter 11
Inter-Integrated Circuit (S08IICV1)

Section Number Title Page

Chapter 14
Serial Communications Interface (S08SCIV3)

Chapter 15
Serial Peripheral Interface (S08SPIV3)

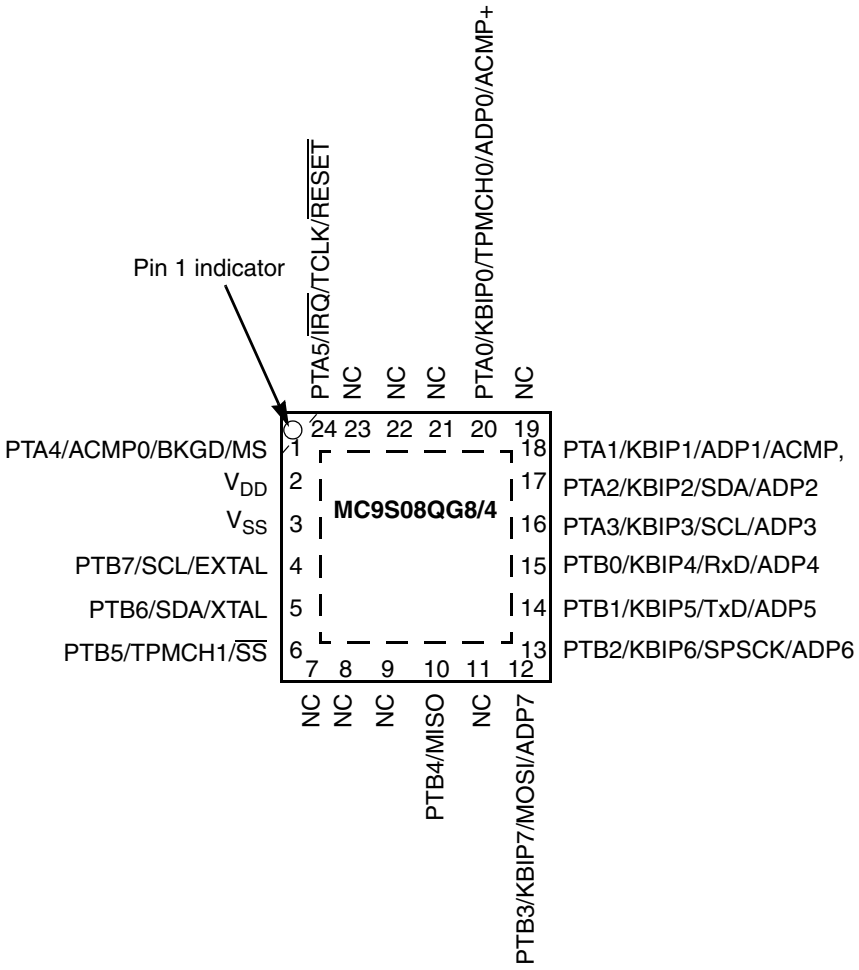


Figure 2-3. 24-Pin Packages

2.2 Recommended System Connections

Figure 2-4 shows pin connections that are common to almost all MC9S08QG8/4 application systems.

4.2 Reset and Interrupt Vector Assignments

Table 4-1 shows address assignments for reset and interrupt vectors. The vector names shown in this table are the labels used in the Freescale Semiconductor-provided equate file for the MC9S08QG8/4.

Table 4-1. Reset and Interrupt Vectors

Address (High:Low)	Vector	Vector Name
0xFFC0:FFC1 ⇕ 0xFFCE:FFCF	Unused Vector Space (available for user program)	
0xFFD0:FFD1	RTI	Vrti
0xFFD2:FFD3	Reserved	—
0xFFD4:FFD5	Reserved	—
0xFFD6:FFD7	ACMP	Vacmp
0xFFD8:FFD9	ADC Conversion	Vadc
0xFFDA:FFDB	KBI Interrupt	Vkeyboard
0xFFDC:FFDD	IIC	Viic
0xFFDE:FFDF	SCI Transmit	Vscitx
0xFFE0:FFE1	SCI Receive	Vscirx
0xFFE2:FFE3	SCI Error	Vscierr
0xFFE4:FFE5	SPI	Vspi
0xFFE6:FFE7	MTIM Overflow	Vmtim
0xFFE8:FFE9	Reserved	—
0xFFEA:FFEB	Reserved	—
0xFFEC:FFED	Reserved	—
0xFFEE:FFEF	Reserved	—
0xFFF0:FFF1	TPM Overflow	Vtpmovf
0xFFF2:FFF3	TPM Channel 1	Vtpmch1
0xFFF4:FFF5	TPM Channel 0	Vtpmch0
0xFFF6:FFF7	Reserved	—
0xFFF8:FFF9	Low Voltage Detect	Vlvd
0xFFFA:FFFB	IRQ	Virq
0xFFFC:FFFD	SWI	Vswi
0xFFFE:FFFF	Reset	Vreset

5.4 Computer Operating Properly (COP) Watchdog

The COP watchdog is intended to force a system reset when the application software fails to execute as expected. To prevent a system reset from the COP timer (when it is enabled), application software must reset the COP counter periodically. If the application program gets lost and fails to reset the COP counter before it times out, a system reset is generated to force the system back to a known starting point.

After any reset, the COPE becomes set in SOPT1 enabling the COP watchdog (see Section 5.8.4, "System Options Register 1 (SOPT1)," for additional information). If the COP watchdog is not used in an application, it can be disabled by clearing COPE. The COP counter is reset by writing any value to the address of SRS. This write does not affect the data in the read-only SRS. Instead, the act of writing to this address is decoded and sends a reset signal to the COP counter.

The COPCLKS bit in SOPT2 (see Section 5.8.5, "System Options Register 2 (SOPT2)," for additional information) selects the clock source used for the COP timer. The clock source options are either the bus clock or an internal 1-kHz clock source. With each clock source, there is an associated short and long time-out controlled by COPT in SOPT1. Table 5-1 summaries the control functions of the COPCLKS and COPT bits. The COP watchdog defaults to operation from the 1-kHz clock source and the associated long time-out (2^8 cycles).

Table 5-1. COP Configuration Options

Control Bits		Clock Source	COP Overflow Count
COPCLKS	COPT		
0	0	~1 kHz	2^5 cycles (32 ms)[1]
0	1	~1 kHz	2^8 cycles (256 ms)[1]
1	0	Bus	2^{13} cycles
1	1	Bus	2^{18} cycles

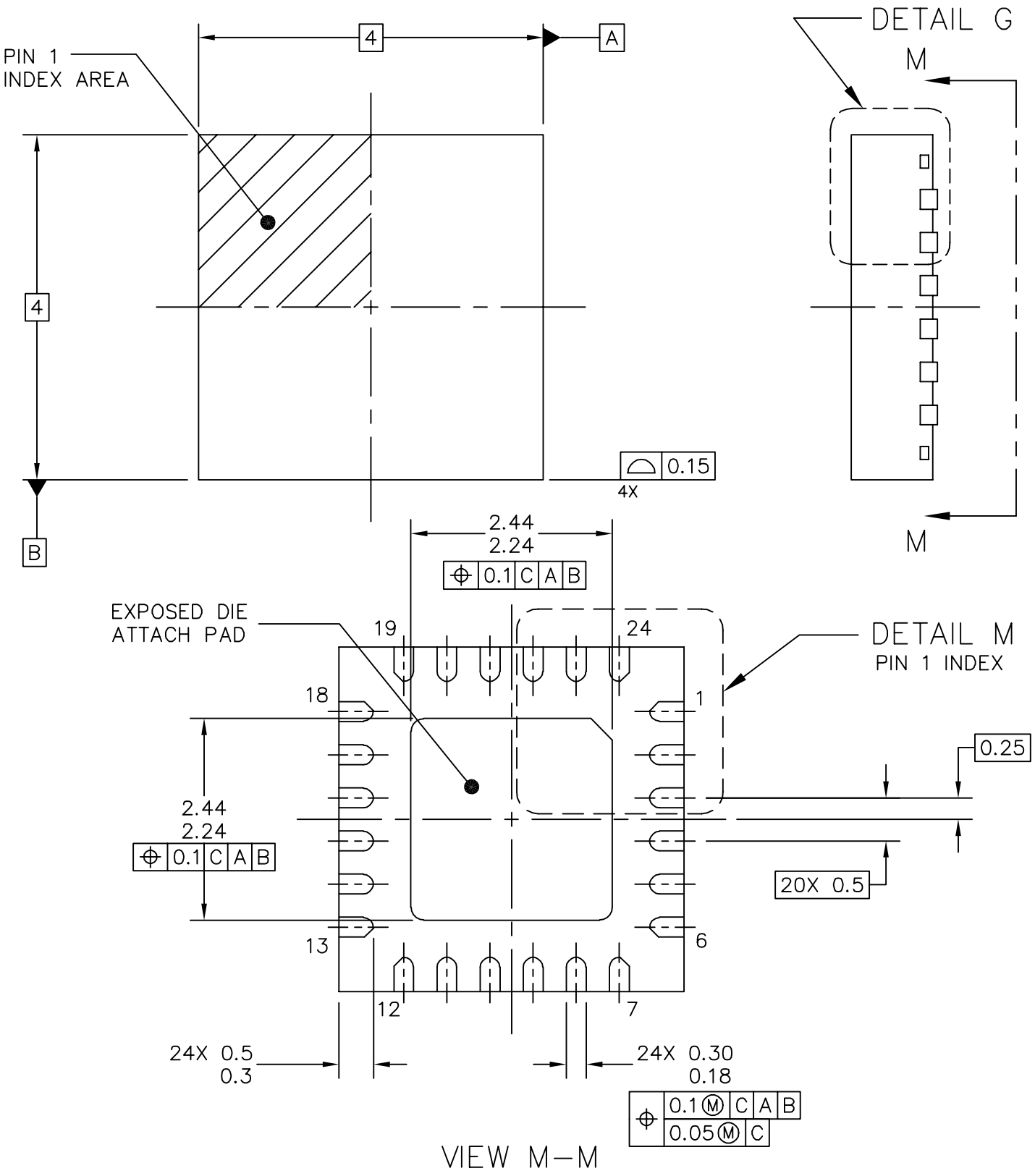
[1] Values are shown in this column based on t_{RTI} = 1 ms. See t_{RTI} in the appendix Section A.8.1, "Control Timing," for the tolerance of this value.

Even if the application will use the reset default settings of COPE, COPCLKS, and COPT, the user must write to the write-once SOPT1 and SOPT2 registers during reset initialization to lock in the settings. That way, they cannot be changed accidentally if the application program gets lost. The initial writes to SOPT1 and SOPT2 will reset the COP counter.

The write to SRS that services (clears) the COP counter must not be placed in an interrupt service routine (ISR) because the ISR could continue to be executed periodically even if the main application program fails.

In background debug mode, the COP counter will not increment.

When the bus clock source is selected, the COP counter does not increment while the system is in stop mode. The COP counter resumes as soon as the MCU exits stop mode.



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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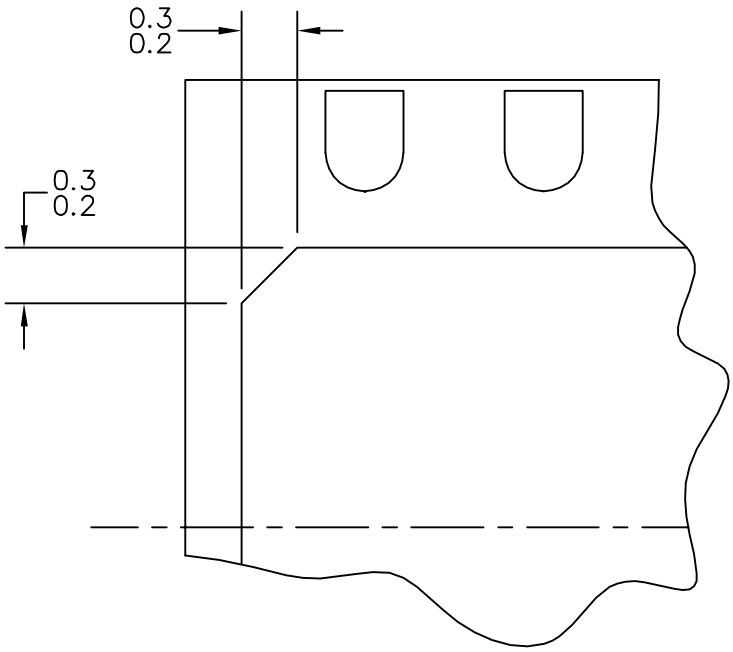
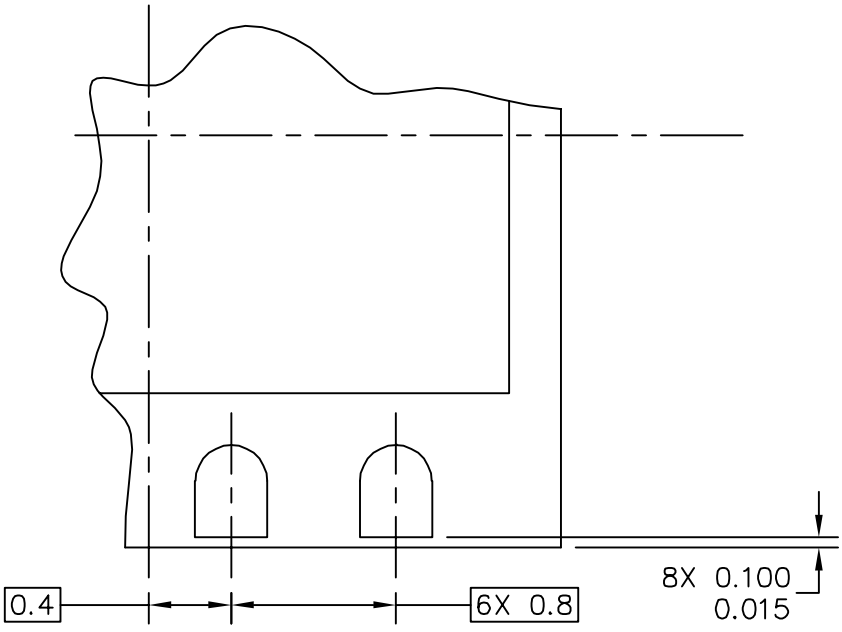
	CASE NUMBER: 1897–01	08 SEP 2006
	STANDARD: JEDEC MO–220 VGGD–8	



DETAIL M
BACKSIDE PIN 1 INDEX



DETAIL N

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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	CASE NUMBER: 1452–02	28 DEC 2005
	STANDARD: NON–JEDEC	