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Details

Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	4
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
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MC9S08QG8 Data Sheet

Covers MC9S08QG8 MC9S08QG4

> MC9S08QG8 Rev. 5 11/2009

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Chapter 2 External Signal Description

2.2.4 Background / Mode Select (BKGD/MS)

During a power-on-reset (POR) or background debug force reset (see 5.8.3, "System Background Debug Force Reset Register (SBDFR)," for more information), the PTA4/ACMPO/BKGD/MS pin functions as a mode select pin. Immediately after any reset, the pin functions as the background pin and can be used for background debug communication. When enabled as the BKGD/MS pin (BKGDPE = 1), an internal pullup device is automatically enabled.

The background debug communication function is enabled when BKGDPE in SOPT1 is set. BKGDPE is set following any reset of the MCU and must be cleared to use the PTA4/ACMPO/BKGD/MS pin's alternative pin functions.

If nothing is connected to this pin, the MCU will enter normal operating mode at the rising edge of the internal reset after a POR or force BDC reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during a POR or immediately after issuing a background debug force reset, which will force the MCU to active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU's BDC clock per bit time. The target MCU's BDC clock could be as fast as the maximum bus clock rate, so there must never be any significant capacitance connected to the BKGD/MS pin that could interfere with background serial communications.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high speedup pulses to ensure fast rise times. Small capacitances from cables and the absolute value of the internal pullup device play almost no role in determining rise and fall times on the BKGD pin.

2.2.5 General-Purpose I/O and Peripheral Ports

The MC9S08QG8/4 series of MCUs support up to 12 general-purpose I/O pins, 1 input-only pin, and 1 output-only pin, which are shared with on-chip peripheral functions (timers, serial I/O, ADC, keyboard interrupts, etc.). On each MC9S08QG8/4 device, there is one input-only and one output-only port pin.

When a port pin is configured as a general-purpose output or a peripheral uses the port pin as an output, software can select one of two drive strengths and enable or disable slew rate control. When a port pin is configured as a general-purpose input or a peripheral uses the port pin as an input, software can enable a pullup device.

For information about controlling these pins as general-purpose I/O pins, see the Chapter 6, "Parallel Input/Output Control." For information about how and when on-chip peripheral systems use these pins, see the appropriate chapter referenced in Table 2-2.

Immediately after reset, all pins that are not output-only are configured as high-impedance general-purpose inputs with internal pullup devices disabled. After reset, the output-only port function is not enabled but is configured for low output drive strength with slew rate control enabled. The PTA4 pin defaults to BKGD/MS on any reset.



Chapter 4 Memory Map and Register Definition

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
0x00 14	ADCCVH	0	0	0	0	0	0	ADCV9	ADCV8	
0x00 15	ADCCVL	ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0	
0x00 16	ADCCFG	ADLPC ADIV		VIV	ADLSMP	MC	MODE		ADICLK	
0x00 17	APCTL1	ADPC7	ADPC6	ADPC5	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	
0x00 18	Reserved	0	0	0	0	0	0	0	0	
0x00 19	Reserved	0	0	0	0	0	0	0	0	
0x00 1A	ACMPSC	ACME	ACBGS	ACF	ACIE	ACO	ACOPE	ACN	IOD	
0x001 B – 0x001 F	Reserved	_		_	_		_	_		
0x00 20	SCIBDH	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8	
0x00 21	SCIBDL	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	
0x00 22	SCIC1	LOOPS	SCISWAI	RSRC	М	WAKE	ILT	PE	PT	
0x00 23	SCIC2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	
0x00 24	SCIS1	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	
0x00 25	SCIS2	0	0	0	0	0	BRK13	0	RAF	
0x00 26	SCIC3	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE	
0x00 27	SCID	Bit 7	6	5	4	3	2	1	Bit 0	
0x00 28	SPIC1	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE	
0x00 29	SPIC2	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0	
0x00 2A	SPIBR	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0	
0x00 2B	SPIS	SPRF	0	SPTEF	MODF	0	0	0	0	
0x00 2C	Reserved	0	0	0	0	0	0	0	0	
0x00 2D	SPID	Bit 7	6	5	4	3	2	1	Bit 0	
0x00 2E	Reserved	_	—	_	—	-	_	—	_	
0x00 2F	Reserved	_	_	_	—	-	_	—	_	
0x00 30	IICA				ADDR				0	
0x00 31	licf	ML	ILT			IC	R			
0x00 32	IICC	IICEN	IICIE	MST	TX	TXAK	RSTA	0	0	
0x00 33	IICS	TCF	IAAS	BUSY	ARBL	0	SRW	IICIF	RXAK	
0x00 34	licd				DA	TA				
0x00 35	Reserved	_	—		_				—	
0x00 36	Reserved	_	—		—	_		_	—	
0x00 37	Reserved	_	_		—	_			_	
0x00 38	ICSC1	CL	KS		RDIV		IREFS	IRCLKEN	IREFSTEN	
0x00 39	ICSC2	BD	NV	RANGE	HGO	LP	EREFS	ERCLKEN	EREFSTEN	
0x00 3A	ICSTRM				TF	IM				
0x00 3B	ICSSC	0	0	0	0	CLł	KST	OSCINIT	FTRIM	
0x00 3C	MTIMSC	TOF	TOIE	TRST	TSTP	0	0	0	0	
0x00 3D	MTIMCLK	0	0	CL	KS		Р	S		
0x00 3E	MTIMCNT	COUNT								



Chapter 4 Memory Map and Register Definition

4.5 FLASH

The FLASH memory is intended primarily for program storage. In-circuit programming allows the operating program to be loaded into the FLASH memory after final assembly of the application product. It is possible to program the entire array through the single-wire background debug interface. Because no special voltages are needed for FLASH erase and programming operations, in-application programming is also possible through other software-controlled communication paths. For a more detailed discussion of in-circuit and in-application programming, refer to the *HCS08 Family Reference Manual, Volume I,* Freescale Semiconductor document order number HCS08RMv1/D.



Table 4-11. FPROT Register Field Descriptions

Field	Description
7:1 FPS	FLASH Protect Select Bits — When FPDIS = 0, this 7-bit field determines the ending address of unprotected FLASH locations at the high address end of the FLASH. Protected FLASH locations cannot be erased or programmed.
0 FPDIS	 FLASH Protection Disable 0 FLASH block specified by FPS7:FPS1 is block protected (program or erase not allowed). 1 No FLASH block is protected.

4.7.5 FLASH Status Register (FSTAT)



Figure 4-9. FLASH Status Register (FSTAT)

Table 4-12. FSTAT Register Field Descriptions

Field	Description
7 FCBEF	 FLASH Command Buffer Empty Flag — The FCBEF bit is used to launch commands. It also indicates that the command buffer is empty so that a new command sequence can be executed when performing burst programming. The FCBEF bit is cleared by writing a 1 to it or when a burst program command is transferred to the array for programming. Only burst program commands can be buffered. 0 Command buffer is full (not ready for additional commands). 1 A new burst program command can be written to the command buffer.
6 FCCF	 FLASH Command Complete Flag — FCCF is set automatically when the command buffer is empty and no command is being processed. FCCF is cleared automatically when a new command is started (by writing 1 to FCBEF to register a command). Writing to FCCF has no meaning or effect. 0 Command in progress 1 All commands complete
5 FPVIOL	 Protection Violation Flag — FPVIOL is set automatically when FCBEF is cleared to register a command that attempts to erase or program a location in a protected block (the erroneous command is ignored). FPVIOL is cleared by writing a 1 to FPVIOL. 0 No protection violation. 1 An attempt was made to erase or program a protected location.



Chapter 5 Resets, Interrupts, and General System Control

5.1 Introduction

This section discusses basic reset and interrupt mechanisms and the various sources of reset and interrupts in the MC9S08QG8/4. Some interrupt sources from peripheral modules are discussed in greater detail within other sections of this data sheet. This section gathers basic information about all reset and interrupt sources in one place for easy reference. A few reset and interrupt sources, including the computer operating properly (COP) watchdog and real-time interrupt (RTI), are not part of on-chip peripheral systems with their own chapters but are part of the system control logic.

5.2 Features

Reset and interrupt features include:

- Multiple sources of reset for flexible system configuration and reliable operation
- Reset status register (SRS) to indicate source of most recent reset
- Separate interrupt vectors for each module (reduces polling overhead) (see Table 5-2)

5.3 MCU Reset

Resetting the MCU provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector (0xFFFE:0xFFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose, high-impedance inputs with pullup devices disabled. The I bit in the condition code register (CCR) is set to block maskable interrupts so the user program has a chance to initialize the stack pointer (SP) and system control settings. SP is forced to 0x00FF at reset.

The MC9S08QG8/4 has the following sources for reset:

- External pin reset (PIN) enabled using RSTPE in SOPT1
- Power-on reset (POR)
- Low-voltage detect (LVD)
- Computer operating properly (COP) timer
- Illegal opcode detect (ILOP)
- Illegal address detect (ILAD)
- Background debug force reset

Each of these sources, with the exception of the background debug force reset, has an associated bit in the system reset status register.

Table 6-1. PTAD Register Field Descriptions

Field	Description
5:0 PTAD[5:0]	Port A Data Register Bits — For port A pins that are inputs, reads return the logic level on the pin. For port A pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port A pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTAD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

6.4.1.2 Port A Data Direction (PTADD)



Figure 6-3. Port A Data Direction Register (PTADD)

¹ PTADD5 has no effect on the input-only PTA5 pin.

² PTADD4 has no effect on the output-only PTA4 pin.

Table 6-2. PTADD Register Field Descriptions

Field	Description
5:0 PTADD[5:0]	Data Direction for Port A Bits — These read/write bits control the direction of port A pins and what is read for PTAD reads.
	 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port A bit n and PTAD reads return the contents of PTADn.

6.4.2 Port A Control Registers

The pins associated with port A are controlled by the registers in this section. These registers control the pin pullup, slew rate, and drive strength of the port A pins independent of the parallel I/O register.



Chapter 11 Inter-Integrated Circuit (S08IICV1)



NOTES:

¹ Not all pins or pin functions are available on all devices, see Table 1-1 for available functions on each device.

- ² Port pins are software configurable with pullup device if input port.
- ³ Port pins are software configurable for output drive strength.
- ⁴ Port pins are software configurable for output slew rate control.
- ⁵ IRQ contains a software configurable (IRQPDD) pullup device if PTA5 enabled as IRQ pin function (IRQPE = 1).
- ⁶ RESET contains integrated pullup device if PTA5 enabled as reset pin function (RSTPE = 1).
- ⁷ PTA4 contains integrated pullup device if BKGD enabled (BKGDPE = 1).
- ⁸ SDA and SCL pin locations can be repositioned under software control (IICPS), defaults on PTA2 and PTA3.
- ⁹ When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

Figure 11-1. MC9S08QG8/4 Block Diagram Highlighting IIC Block and Pins



Inter-Integrated Circuit (S08IICV1)

11.3.3 IIC Control Register (IICC)



Figure 11-5. IIC Control Register (IICC)

Field	Description
7 IICEN	 IIC Enable — The IICEN bit determines whether the IIC module is enabled. 0 IIC is not enabled. 1 IIC is enabled.
6 IICIE	 IIC Interrupt Enable — The IICIE bit determines whether an IIC interrupt is requested. IIC interrupt request not enabled. IIC interrupt request enabled.
5 MST	 Master Mode Select — The MST bit is changed from a 0 to a 1 when a START signal is generated on the bus and master mode is selected. When this bit changes from a 1 to a 0 a STOP signal is generated and the mode of operation changes from master to slave. 0 Slave Mode. 1 Master Mode.
4 TX	 Transmit Mode Select — The TX bit selects the direction of master and slave transfers. In master mode this bit should be set according to the type of transfer required. Therefore, for address cycles, this bit will always be high. When addressed as a slave this bit should be set by software according to the SRW bit in the status register. Receive. Transmit.
3 ТХАК	 Transmit Acknowledge Enable — This bit specifies the value driven onto the SDA during data acknowledge cycles for both master and slave receivers. An acknowledge signal will be sent out to the bus after receiving one data byte. No acknowledge signal response is sent.
2 RSTA	Repeat START — Writing a one to this bit will generate a repeated START condition provided it is the current master. This bit will always be read as a low. Attempting a repeat at the wrong time will result in loss of arbitration.



Inter-Integrated Circuit (S08IICV1)

11.7 Initialization/Application Information

4	Write: IIC	Module Initialization (Slave)			
1.	— to se	A It the slave address			
2.	Write: IIC	C			
0	— to en	able IIC and interrupts			
3. 4.	Initialize I	RAM variables (ICEN = 1 and ICE = 1) for transmit data RAM variables used to achieve the routine shown in Figure 11-11			
		Module Initialization (Master)			
1.	Write: IIC	F			
~	— to se	t the IIC baud rate (example provided in this chapter)			
2.	write: IIC	c able IIC and interrupts			
3.	Initialize I	RAM variables (IICEN = 1 and IICIE = 1) for transmit data			
4.	Initialize I	RAM variables used to achieve the routine shown in Figure 11-11			
5.	Write: IIC	C			
6	— to en				
0.	— to en	able MST (master mode)			
7.	Write: IIC	D			
	— with	the address of the target slave. (The LSB of this byte will determine whether the communication is			
	mast	er receive or transmit.)			
	The routine shown in Figure 11-11 can handle both master and slave IIC operations. For slave operation, an incoming IIC message that contains the proper address will begin IIC communication. For master operation, communication must be initiated by writing to the IICD register.				
	Register Model				
	IICA				
		Address to which the module will respond when addressed as a slave (in slave mode)			
	IICF	Baud rate – BUSCI K / (2 x MULT x (SCL DI)//IDER))			
	IICC	IICEN IICIE MST TX TXAK RSTA 0 0			
	Module configuration				
	IICS	TCF IAAS BUSY ARBL 0 SRW IICIF RXAK			
		Module status flags			
	IICD	IICD DATA			
		Data register: Write to transmit IIC data read to read IIC data			

Figure 11-10. IIC Module Quick Start



Chapter 15 Serial Peripheral Interface (S08SPIV3)

15.1 Introduction

Figure 15-1 shows the MC9S08QG8/4 block diagram with the SPI highlighted.



Serial Peripheral Interface (S08SPIV3)

in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The \overline{SS} OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master \overline{SS} output goes to active low at the start of the first bit time of the transfer and goes back high one-half SPSCK cycle after the end of the eighth bit time of the transfer. The \overline{SS} IN waveform applies to the slave select input of a slave.





When CPHA = 0, the slave begins to drive its MISO output with the first data bit value (MSB or LSB depending on LSBFE) when \overline{SS} goes to active low. The first SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the second SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CPHA = 0, the slave's \overline{SS} input must go to its inactive high level between transfers.





Figure 17-2. BDC Host-to-Target Serial Bit Timing

Figure 17-3 shows the host receiving a logic 1 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target MCU. The host holds the BKGD pin low long enough for the target to recognize it (at least two target BDC cycles). The host must release the low drive before the target MCU drives a brief active-high speedup pulse seven cycles after the perceived start of the bit time. The host should sample the bit level about 10 cycles after it started the bit time.



Figure 17-3. BDC Target-to-Host Serial Bit Timing (Logic 1)



the host must perform ((8 - CNT) - 1) dummy reads of the FIFO to advance it to the first significant entry in the FIFO.

In most trigger modes, the information stored in the FIFO consists of 16-bit change-of-flow addresses. In these cases, read DBGFH then DBGFL to get one coherent word of information out of the FIFO. Reading DBGFL (the low-order byte of the FIFO data port) causes the FIFO to shift so the next word of information is available at the FIFO data port. In the event-only trigger modes (see Section 17.3.5, "Trigger Modes"), 8-bit data information is stored into the FIFO. In these cases, the high-order half of the FIFO (DBGFH) is not used and data is read out of the FIFO by simply reading DBGFL. Each time DBGFL is read, the FIFO is shifted so the next data value is available through the FIFO data port at DBGFL.

In trigger modes where the FIFO is storing change-of-flow addresses, there is a delay between CPU addresses and the input side of the FIFO. Because of this delay, if the trigger event itself is a change-of-flow address or a change-of-flow address appears during the next two bus cycles after a trigger event starts the FIFO, it will not be saved into the FIFO. In the case of an end-trace, if the trigger event is a change-of-flow, it will be saved as the last change-of-flow entry for that debug run.

The FIFO can also be used to generate a profile of executed instruction addresses when the debugger is not armed. When ARM = 0, reading DBGFL causes the address of the most-recently fetched opcode to be saved in the FIFO. To use the profiling feature, a host debugger would read addresses out of the FIFO by reading DBGFH then DBGFL at regular periodic intervals. The first eight values would be discarded because they correspond to the eight DBGFL reads needed to initially fill the FIFO. Additional periodic reads of DBGFH and DBGFL return delayed information about executed instructions so the host debugger can develop a profile of executed instruction addresses.

17.3.3 Change-of-Flow Information

To minimize the amount of information stored in the FIFO, only information related to instructions that cause a change to the normal sequential execution of instructions is stored. With knowledge of the source and object code program stored in the target system, an external debugger system can reconstruct the path of execution through many instructions from the change-of-flow information stored in the FIFO.

For conditional branch instructions where the branch is taken (branch condition was true), the source address is stored (the address of the conditional branch opcode). Because BRA and BRN instructions are not conditional, these events do not cause change-of-flow information to be stored in the FIFO.

Indirect JMP and JSR instructions use the current contents of the H:X index register pair to determine the destination address, so the debug system stores the run-time destination address for any indirect JMP or JSR. For interrupts, RTI, or RTS, the destination address is stored in the FIFO as change-of-flow information.

17.3.4 Tag vs. Force Breakpoints and Triggers

Tagging is a term that refers to identifying an instruction opcode as it is fetched into the instruction queue, but not taking any other action until and unless that instruction is actually executed by the CPU. This distinction is important because any change-of-flow from a jump, branch, subroutine call, or interrupt causes some instructions that have been fetched into the instruction queue to be thrown away without being executed.



17.4.1.1 BDC Status and Control Register (BDCSCR)

This register can be read or written by serial BDC commands (READ_STATUS and WRITE_CONTROL) but is not accessible to user programs because it is not located in the normal memory map of the MCU.



= Unimplemented or Reserved

Figure 17-5. BDC Status and Control Register (BDCSCR)

Table 17-2. BDCSCR Register Field Descriptions

Field	Description
7 ENBDM	 Enable BDM (Permit Active Background Mode) — Typically, this bit is written to 1 by the debug host shortly after the beginning of a debug session or whenever the debug host resets the target and remains 1 until a normal reset clears it. 0 BDM cannot be made active (non-intrusive commands still allowed) 1 BDM can be made active to allow active background mode commands
6 BDMACT	 Background Mode Active Status — This is a read-only status bit. 0 BDM not active (user application program running) 1 BDM active and waiting for serial commands
5 BKPTEN	 BDC Breakpoint Enable — If this bit is clear, the BDC breakpoint is disabled and the FTS (force tag select) control bit and BDCBKPT match register are ignored. 0 BDC breakpoint disabled 1 BDC breakpoint enabled
4 FTS	 Force/Tag Select — When FTS = 1, a breakpoint is requested whenever the CPU address bus matches the BDCBKPT match register. When FTS = 0, a match between the CPU address bus and the BDCBKPT register causes the fetched opcode to be tagged. If this tagged opcode ever reaches the end of the instruction queue, the CPU enters active background mode rather than executing the tagged opcode. 0 Tag opcode at breakpoint address and enter active background mode if CPU attempts to execute that instruction 1 Breakpoint match forces active background mode at next instruction boundary (address need not be an opcode)
3 CLKSW	Select Source for BDC Communications Clock — CLKSW defaults to 0, which selects the alternate BDC clock source. 0 Alternate BDC clock source 1 MCU bus clock





¹ BDFR is writable only through serial background mode debug commands, not from user programs.

Figure 17-6. System Background Debug Force Reset Register (SBDFR)

Table 17-3. SBDFR Register Field Description

Field	Description
0 BDFR	Background Debug Force Reset — A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.

17.4.3 DBG Registers and Control Bits

The debug module includes nine bytes of register space for three 16-bit registers and three 8-bit control and status registers. These registers are located in the high register space of the normal memory map so they are accessible to normal application programs. These registers are rarely if ever accessed by normal user application programs with the possible exception of a ROM patching mechanism that uses the breakpoint logic.

17.4.3.1 Debug Comparator A High Register (DBGCAH)

This register contains compare value bits for the high-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.2 Debug Comparator A Low Register (DBGCAL)

This register contains compare value bits for the low-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.3 Debug Comparator B High Register (DBGCBH)

This register contains compare value bits for the high-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.4 Debug Comparator B Low Register (DBGCBL)

This register contains compare value bits for the low-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.



Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Conversion time (including sample time)	Short sample (ADLSMP=0)	t _{ADC}		20	_	ADCK cycles	See Table 9-12 for conversion time variances
	Long sample (ADLSMP=1)		_	40	_		
Sample time	Short sample (ADLSMP=0)	t _{ADS}	_	3.5	—	ADCK cycles	
	Long sample (ADLSMP=1)		_	23.5	—		
Total unadjusted error	10 bit mode	E _{TUE} — ±1.5	±3.5	LSB ²	Includes		
	8 bit mode		_	±0.7	±1.5		quantization
Differential non-linearity	10 bit mode	DNL	_	±0.5	±1.0	LSB ²	Monotonicity and no missing codes guaranteed
	8 bit mode		_	±0.3	±0.5		
Integral non-linearity	10 bit mode	INL	_	±0.5	±1.0	LSB ²	
	8 bit mode			±0.3	±0.5		
Zero-scale error	10 bit mode	E _{ZS}		±1.5	±2.1	LSB ²	$V_{ADIN} = V_{SS}$
	8 bit mode			±0.5	±0.7		
Full-scale error	10 bit mode	E _{FS}	0	±1.0	±1.5	LSB ²	$V_{ADIN} = V_{DD}$
	8 bit mode		0	±0.5	±0.5		
Quantization error	10 bit mode	EQ	_	—	±0.5	LSB ²	
	8 bit mode		_	—	±0.5		
Input leakage error	10 bit mode	E _{IL}	0	±0.2	±4	LSB ²	Pad leakage ³ * R _{AS}
	8 bit mode		0	±0.1	±1.2		
Temp sensor slope	-40°C– 25°C	m	—	1.646	—	mV/°C	
	25°C– 85°C		_	1.769	_		
Temp sensor voltage	25°C	V _{TEMP25}	_	701.2	—	mV	

Table A-14. 3 Volt 10-bit ADC Character	ristics (continued)
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¹ Typical values assume V_{DD} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
 ² 1 LSB = (V_{REFH} - V_{REFL})/2^N

³ Based on input pad leakage current. Refer to pad electricals.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFN.

4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.

5. MIN. METAL GAP SHOULD BE 0.2 MM.

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TITLE: THERMALLY ENHANCED QUAD		DOCUMENT NO: 98ARL10605D		REV: O	
FLAT NON-LEADED PACKAG	CASE NUMBER: 1897-01 08 SEP 200				
24 TERMINAL, 0.5 PITCH (4 X 4 X 1)		STANDARD: JEDEC M0-220 VGGD-8			







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TITLE:		DOCUMENT NO): 98ASB42564B	REV: V	
8LD SOIC NARROW	BODY	CASE NUMBER	20 NOV 2007		
		STANDARD: JE	DEC MS-012AA		