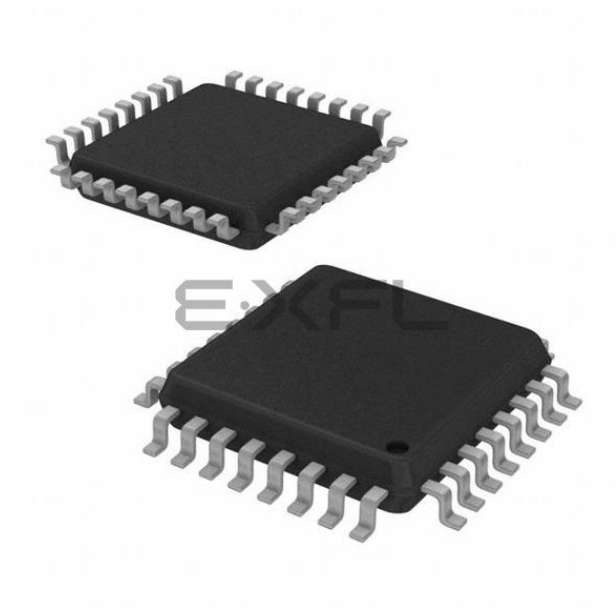

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | S08 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | SCI |
| Peripherals | LVD, PWM, WDT |
| Number of I/O | 30 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 12x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08fl16clc |

# 1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of MC9S08FL16 series MCU.

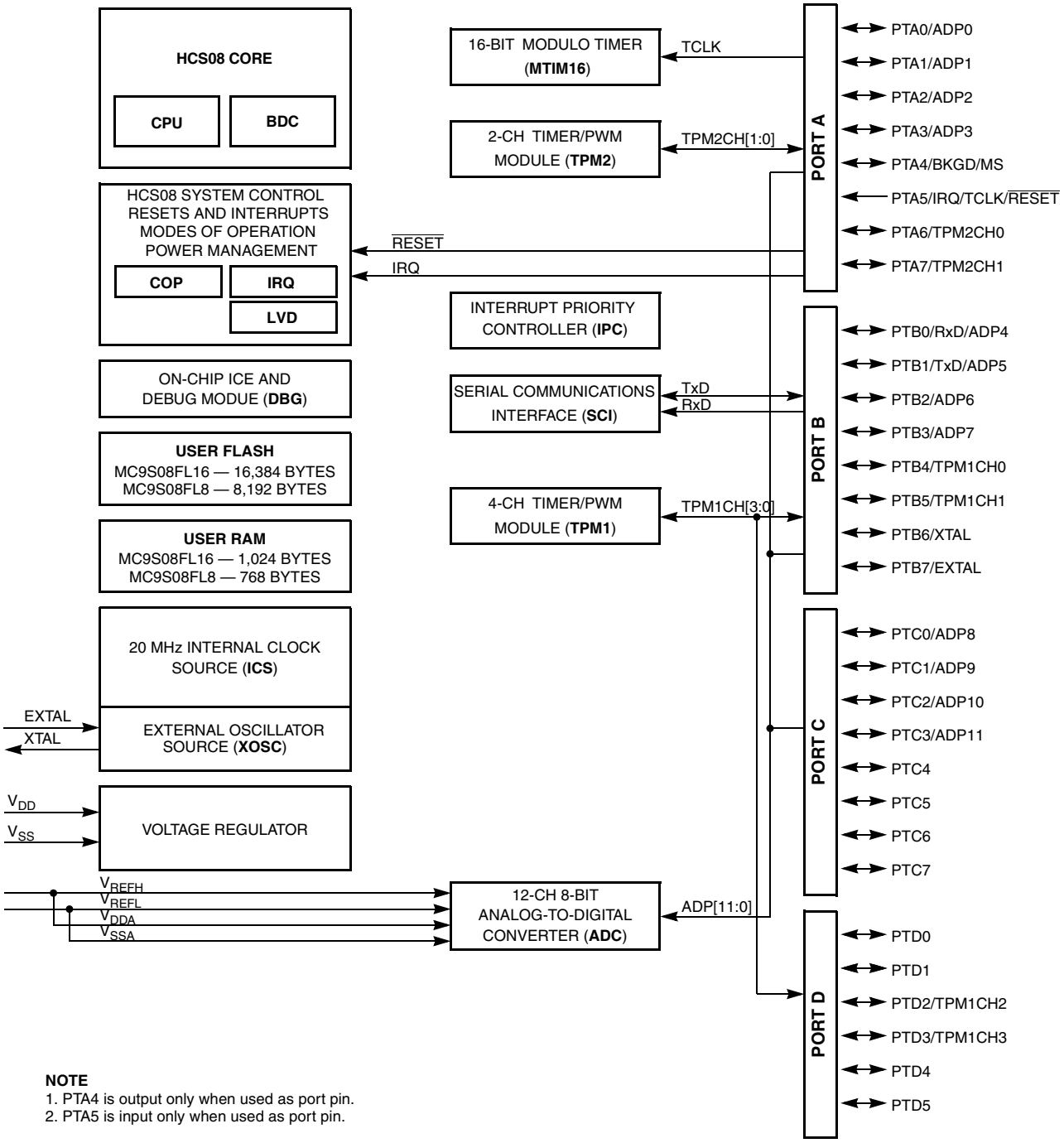



**Figure 1. MC9S08FL16 Series Block Diagram**

# 2 System Clock Distribution

MC9S08FL16 series use ICS module as clock sources. The ICS module can use internal or external clock source as reference to provide up to 20 MHz CPU clock. The output of ICS module includes,

- OSCOUT — XOSC output provides external reference clock to ADC.
- ICSFFCLK — ICS fixed frequency clock reference (around 32.768 kHz) provides double of the fixed lock signal to TPMs and MTIM16.
- ICSOUT — ICS CPU clock provides double of the bus clock which is basic clock reference of peripherals.
- ICSLCLK — Alternate BDC clock provides debug signal to BDC module.

The TCLK pin is an extra external clock source. When TCLK is enabled, it can provide alternate clock source to TPMs and MTIM16. The on-chip 1 kHz clock provides clock source of COP module.

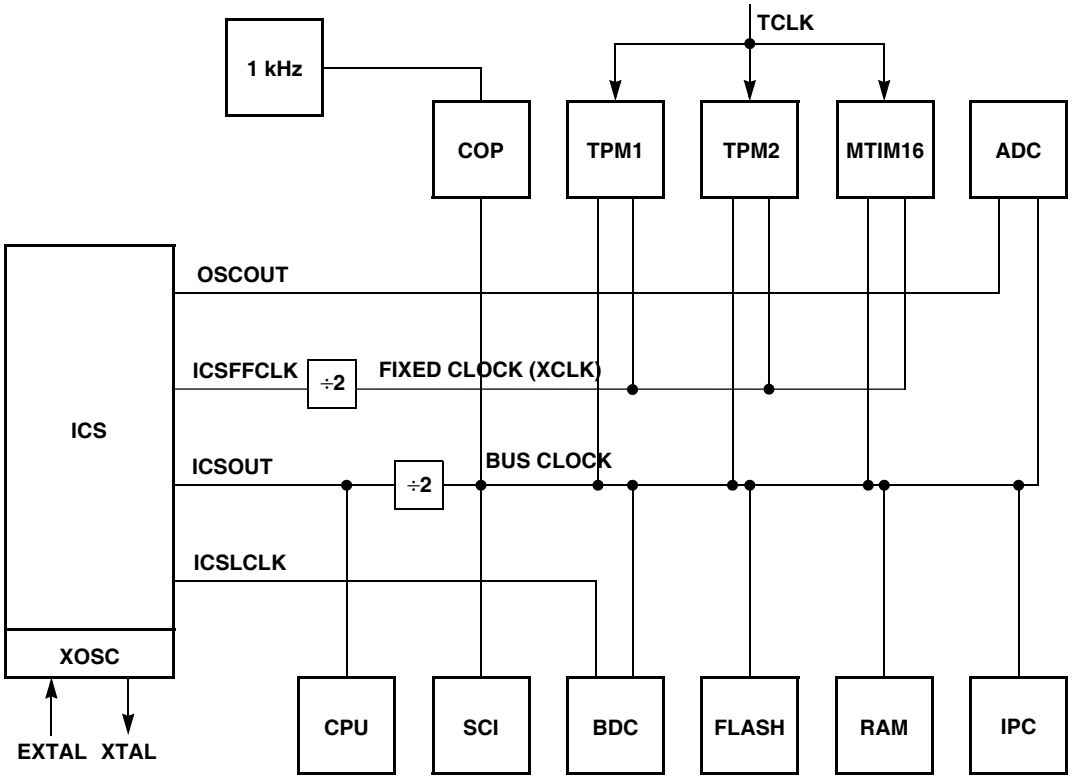



**Figure 2. System Clock Distribution Diagram**

# 3 Pin Assignments

This section shows the pin assignments for the MC9S08FL16 series devices.

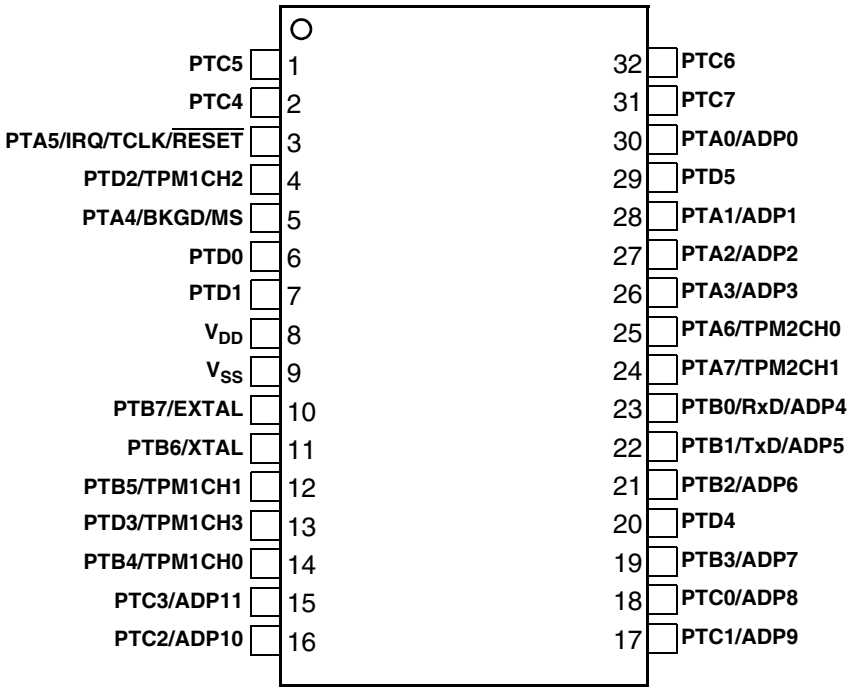



**Figure 3. MC9S08FL16 Series 32-Pin SDIP Package**

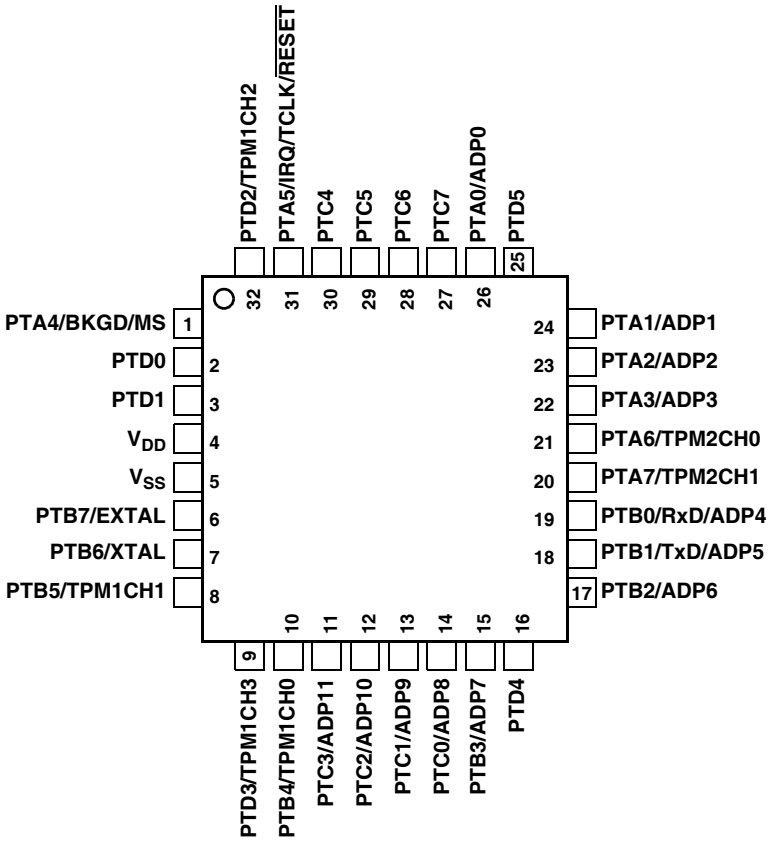



**Figure 4. MC9S08FL16 Series 32-Pin LQFP Package**

**Table 1. Pin Availability by Package Pin-Count**

| Pin Number | | <-- Lowest **Priority** --> Highest | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **32-SDIP** | **32-LQFP** | **Port Pin** | **I/O** | **Alt 1** | **I/O** | **Alt 2** | **I/O** | **Alt 3** | **I/O** |
| 1 | 29 | PTC5 | I/O | | | | | | |
| 2 | 30 | PTC4 | I/O | | | | | | |
| 3 | 31 | PTA5 | I | IRQ | I | TCLK | I | $\overline{\text{RESET}}$ | I |
| 4 | 32 | PTD2 | I/O | | | TPM1CH2 | I/O | | |
| 5 | 1 | PTA4 | O | | | BKGD | I | MS | I |
| 6 | 2 | PTD0 | I/O | | | | | | |
| 7 | 3 | PTD1 | I/O | | | | | | |
| 8 | 4 | | | | | | | $V_{DD}$ | I |
| 9 | 5 | | | | | | | $V_{SS}$ | I |
| 10 | 6 | PTB7 | I/O | EXTAL | I | | | | |
| 11 | 7 | PTB6 | I/O | XTAL | O | | | | |
| 12 | 8 | PTB5 | I/O | | | TPM1CH1 | I/O | | |
| 13 | 9 | PTD3 | I/O | | | TPM1CH3 | I/O | | |
| 14 | 10 | PTB4 | I/O | | | TPM1CH0 | I/O | | |
| 15 | 11 | PTC3 | I/O | | | ADP11 | I | | |

**Table 1. Pin Availability by Package Pin-Count (continued)**

| Pin Number | | <-- Lowest **Priority** --> Highest | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **32-SDIP** | **32-LQFP** | **Port Pin** | **I/O** | **Alt 1** | **I/O** | **Alt 2** | **I/O** | **Alt 3** | **I/O** |
| 16 | 12 | PTC2 | I/O | | | ADP10 | I | | |
| 17 | 13 | PTC1 | I/O | | | ADP9 | I | | |
| 18 | 14 | PTC0 | I/O | | | ADP8 | I | | |
| 19 | 15 | PTB3 | I/O | | | ADP7 | I | | |
| 20 | 16 | PTD4 | I/O | | | | | | |
| 21 | 17 | PTB2 | I/O | | | ADP6 | I | | |
| 22 | 18 | PTB1 | I/O | | | TxD | I/O | ADP5 | I |
| 23 | 19 | PTB0 | I/O | | | RxD | I | ADP4 | I |
| 24 | 20 | PTA7 | I/O | | | TPM2CH1 | I/O | | |
| 25 | 21 | PTA6 | I/O | | | TPM2CH0 | I/O | | |
| 26 | 22 | PTA3 | I/O | | | ADP3 | I | | |
| 27 | 23 | PTA2 | I/O | | | ADP2 | I | | |
| 28 | 24 | PTA1 | I/O | | | ADP1 | I | | |
| 29 | 25 | PTD5 | I/O | | | | | | |
| 30 | 26 | PTA0 | I/O | | | ADP0 | I | | |
| 31 | 27 | PTC7 | I/O | | | | | | |
| 32 | 28 | PTC6 | I/O | | | | | | |

## NOTE

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear out any associated flags before interrupts are enabled. Table 1 illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

# 4 Memory Map

Figure 5 shows the memory map for the MC9S08FL16 series. On-chip memory in the MC9S08FL16 series of MCUs consists of RAM, flash program memory for nonvolatile data storage, plus I/O and control/status registers. The registers are divided into two groups:

- Direct-page registers (0x0000 through 0x003F)
- High-page registers (0x1800 through 0x187F)

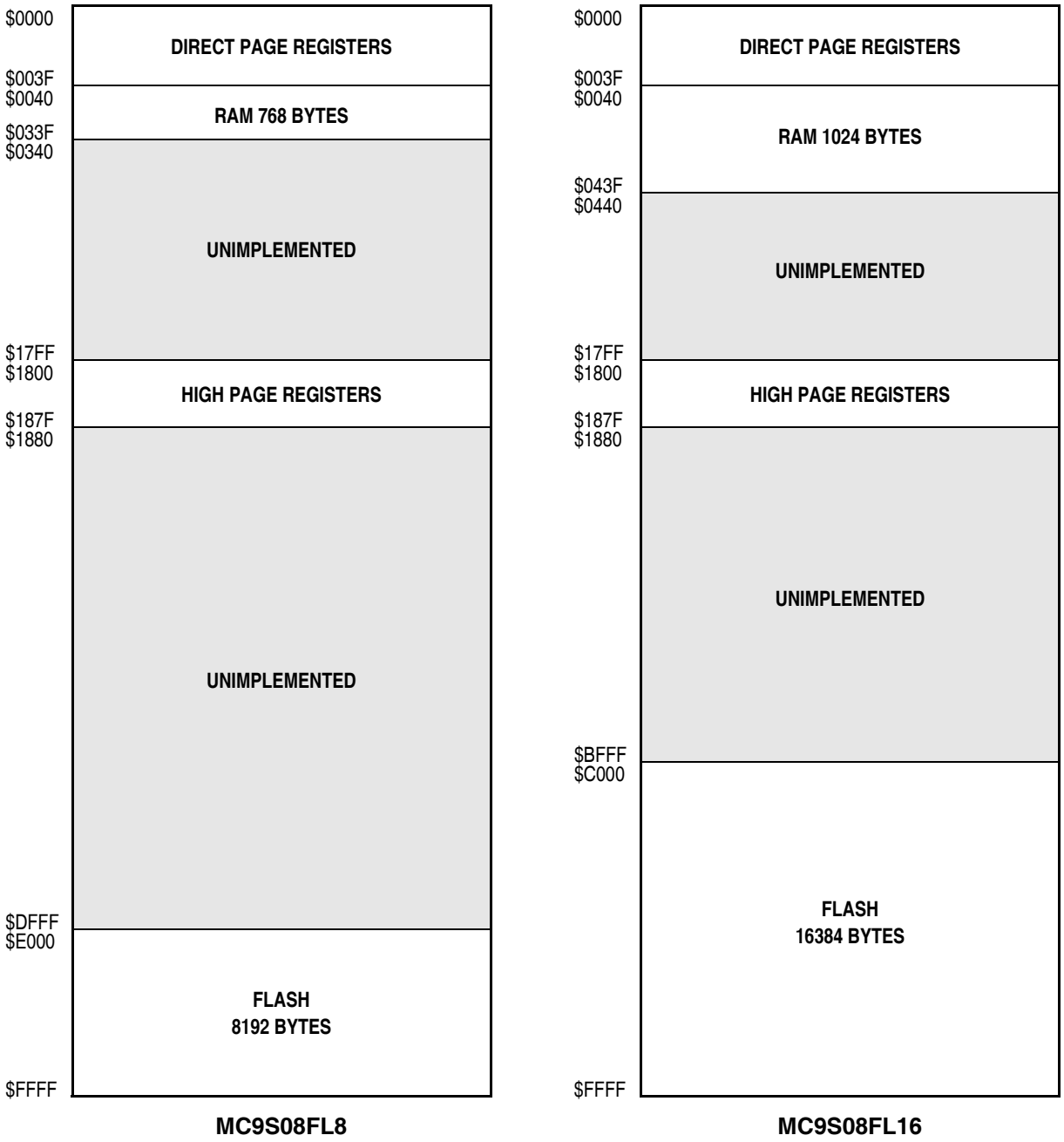



**Figure 5. MC9S08FL16 Series Memory Map**

# 5 Electrical Characteristics

## 5.1 Introduction

This section contains electrical and timing specifications for the MC9S08FL16 series of microcontrollers available at the time of publication.

## 5.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 2. Parameter Classifications**

| | |
|---|---|
| **P** | Those parameters are guaranteed during production testing on each individual device. |
| **C** | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| **T** | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| **D** | Those parameters are derived mainly from simulations. |

**NOTE**

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## 5.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either $V_{SS}$ or $V_{DD}$) or the programmable pullup resistor associated with the pin is enabled.

**Table 3. Absolute Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | –0.3 to 5.8 | V |
| Maximum current into $V_{DD}$ | $I_{DD}$ | 120 | mA |
| Digital input voltage | $V_{In}$ | –0.3 to $V_{DD}$ + 0.3 | V |
| Instantaneous maximum current<br>Single pin limit (applies to all port pins)[1, 2, 3] | $I_D$ | ±25 | mA |
| Storage temperature range | $T_{stg}$ | –55 to 150 | °C |

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ($V_{DD}$) and negative ($V_{SS}$) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTA5 are internally clamped to $V_{SS}$ and $V_{DD}$.

3 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

## 5.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and $V_{SS}$ or $V_{DD}$ and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and $V_{SS}$ or $V_{DD}$ will be very small.

**Table 4. Thermal Characteristics**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating temperature range (packaged) | $T_A$ | $T_L$ to $T_H$<br>–40 to 85 | °C |
| Thermal resistance<br>Single-layer board | | | |
| 32-pin SDIP | $\theta_{JA}$ | 60 | °C/W |
| 32-pin LQFP | | 85 | |
| Thermal resistance<br>Four-layer board | | | |
| 32-pin SDIP | $\theta_{JA}$ | 35 | °C/W |
| 32-pin LQFP | | 56 | |

The average chip-junction temperature ($T_J$) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

$T_A$ = Ambient temperature, °C
$\theta_{JA}$ = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O}$ far much smaller than $P_{int}$ and can be neglected. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring $P_D$ (at equilibrium) for an known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving Equation 1 and Equation 2 iteratively for any value of $T_A$.

## 5.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

During the device qualification, ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

**Table 5. ESD and Latch-Up Test Conditions**

| Model | Description | Symbol | Value | Unit |
|---|---|---|---|---|
| Human body | Series resistance | R1 | 1500 | Ω |
| | Storage capacitance | C | 100 | pF |
| | Number of pulses per pin | — | 3 | — |
| Latch-up | Minimum input voltage limit | — | –2.5 | V |
| | Maximum input voltage limit | — | 7.5 | V |

**Table 6. ESD and Latch-Up Protection Characteristics**

| No. | Rating[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | Human body model (HBM) | $V_{HBM}$ | ±2000 | — | V |
| 2 | Charge device model (CDM) | $V_{CDM}$ | ±500 | — | V |
| 3 | Latch-up current at $T_A$ = 85 °C | $I_{LAT}$ | ±100 | — | mA |

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## 5.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 7. DC Characteristics**

| Num | C | Characteristic | | Symbol | Condition | Min. | Typical[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| 1 | P | Operating voltage | | — | — | 4.5 | — | 5.5 | V |
| 2 | C | Output high voltage | All I/O pins, low-drive strength | $V_{OH}$ | $I_{Load}$ = –2 mA | $V_{DD}$ – 1.5 | — | — | V |
| | P | | All I/O pins, high-drive strength | | $I_{Load}$ = –10 mA | $V_{DD}$ – 1.5 | — | — | |
| 3 | D | Output high current | Max total $I_{OH}$ for all ports | $I_{OHT}$ | — | — | — | 100 | mA |
| 4 | C | Output low voltage | All I/O pins, low-drive strength | $V_{OL}$ | $I_{Load}$ = 2 mA | — | — | 1.5 | V |
| | P | | All I/O pins, high-drive strength | | $I_{Load}$ = 10 mA | — | — | 1.5 | |
| 5 | D | Output low current | Max total $I_{OL}$ for all ports | $I_{OLT}$ | — | — | — | 100 | mA |
| 6 | P | Input high voltage | All digital inputs | $V_{IH}$ | — | 0.65 × $V_{DD}$ | — | — | V |
| 7 | P | Input low voltage | All digital inputs | $V_{IL}$ | — | — | — | 0.35 × $V_{DD}$ | V |
| 8 | C | Input hysteresis | All digital inputs | $V_{hys}$ | — | 0.06 × $V_{DD}$ | — | — | mV |
| 9 | P | Input leakage current | All input only pins (per pin) | $\lvert I_{In} \rvert$ | $V_{In}$ = $V_{DD}$ or $V_{SS}$ | — | 0.1 | 1 | µA |
| 10 | P | Hi-Z (off-state) leakage current | All input/output (per pin) | $\lvert I_{OZ} \rvert$ | $V_{In}$ = $V_{DD}$ or $V_{SS}$ | — | 0.1 | 1 | µA |
| 11a | C | Pullup, pulldown resistors | All digital inputs, when enabled (all I/O pins other than PTA5/IRQ/TCLK/$\overline{\text{RESET}}$) | $R_{PU}$, $R_{PD}$ | — | 17.5 | 36.5 | 52.5 | kΩ |
| 11b | C | Pullup, pulldown resistors | (PTA5/IRQ/TCLK/$\overline{\text{RESET}}$) | $R_{PU}$, $R_{PD}$ (Note[2]) | — | 17.5 | 36.5 | 52.5 | kΩ |

**Table 7. DC Characteristics (continued)**

| Num | C | Characteristic | Symbol | Condition | Min. | Typical[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| 12 | C | DC injection current [3, 4, 5] — Single pin limit | $I_{IC}$ | $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ | –0.2 | — | 0.2 | mA |
| | | DC injection current [3, 4, 5] — Total MCU limit, includes sum of all stressed pins | | | –5 | — | 5 | mA |
| 13 | C | Input capacitance, all pins | $C_{In}$ | — | — | — | 8 | pF |
| 14 | C | RAM retention voltage | $V_{RAM}$ | — | — | 0.6 | 1.0 | V |
| 15 | C | POR re-arm voltage[6] | $V_{POR}$ | — | 0.9 | 1.4 | 2.0 | V |
| 16 | D | POR re-arm time | $t_{POR}$ | — | 10 | — | — | µs |
| 17 | P | Low-voltage detection threshold — high range<br>$V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVD1}$[7] | — | <br>3.9<br>4.0 | <br>4.0<br>4.1 | <br>4.1<br>4.2 | V |
| 18 | C | Low-voltage warning threshold — high range 1<br>$V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVW3}$ | — | <br>4.5<br>4.6 | <br>4.6<br>4.7 | <br>4.7<br>4.8 | V |
| | P | Low-voltage warning threshold — high range 0<br>$V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVW2}$[7] | — | <br>4.2<br>4.3 | <br>4.3<br>4.4 | <br>4.4<br>4.5 | V |
| 19 | C | Low-voltage inhibit reset/recover hysteresis | $V_{hys}$ | — | — | 100 | — | mV |
| 20 | C | Bandgap voltage reference[8] | $V_{BG}$ | — | — | 1.21 | — | V |

1 Typical values are measured at 25 °C. Characterized, not tested.

2 The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear higher when measured externally on the pin.

3 All functional non-supply pins, except for PTA5 are internally clamped to $V_{SS}$ and $V_{DD}$.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure that external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 When $V_{DD}$ is in between the minimun of this parameter and 4.5 V, the CPU, RAM, LVD and flash are full functional, but the performance of other modules may be reduced.

8 Factory trimmed at $V_{DD}$ = 5.0 V, Temp = 25 °C

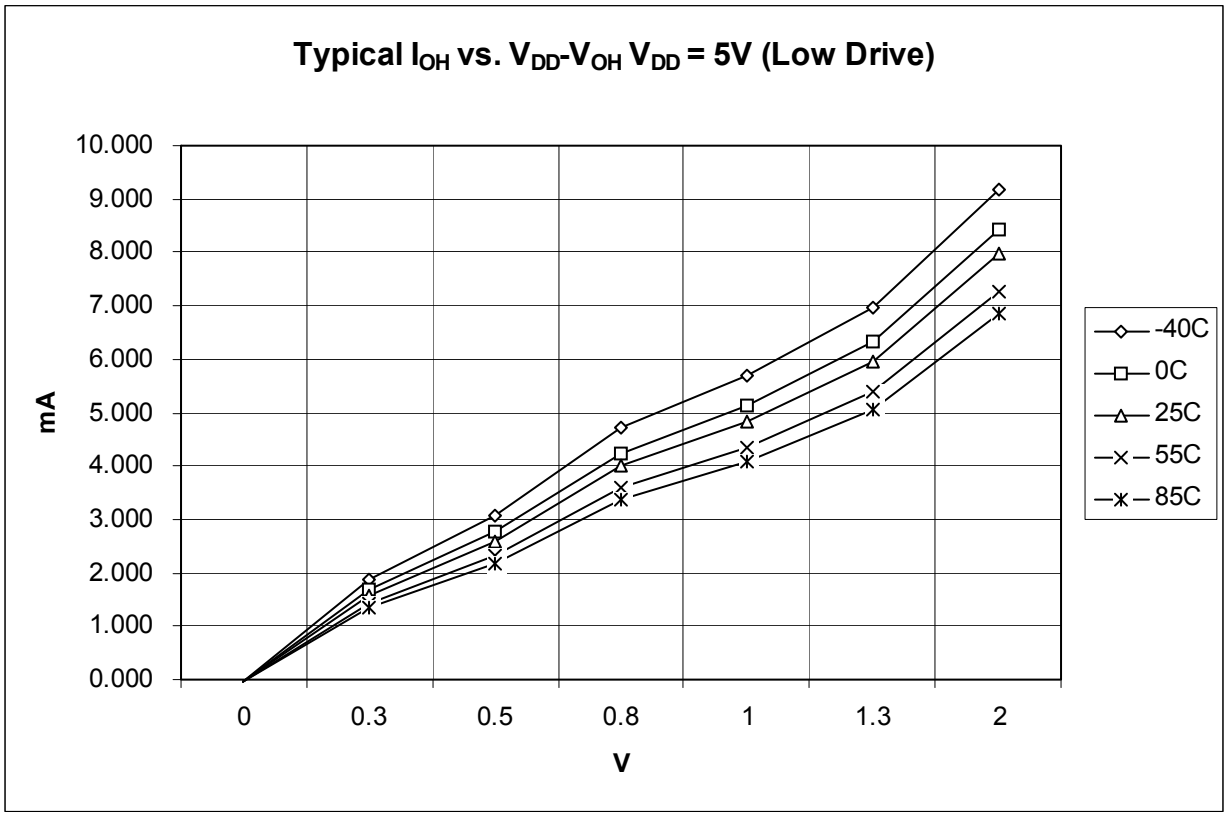



**Figure 7. Typical $I_{OH}$ Vs $V_{DD}$–$V_{OH}$ ($V_{DD}$ = 5.0 V) (Low Drive)**

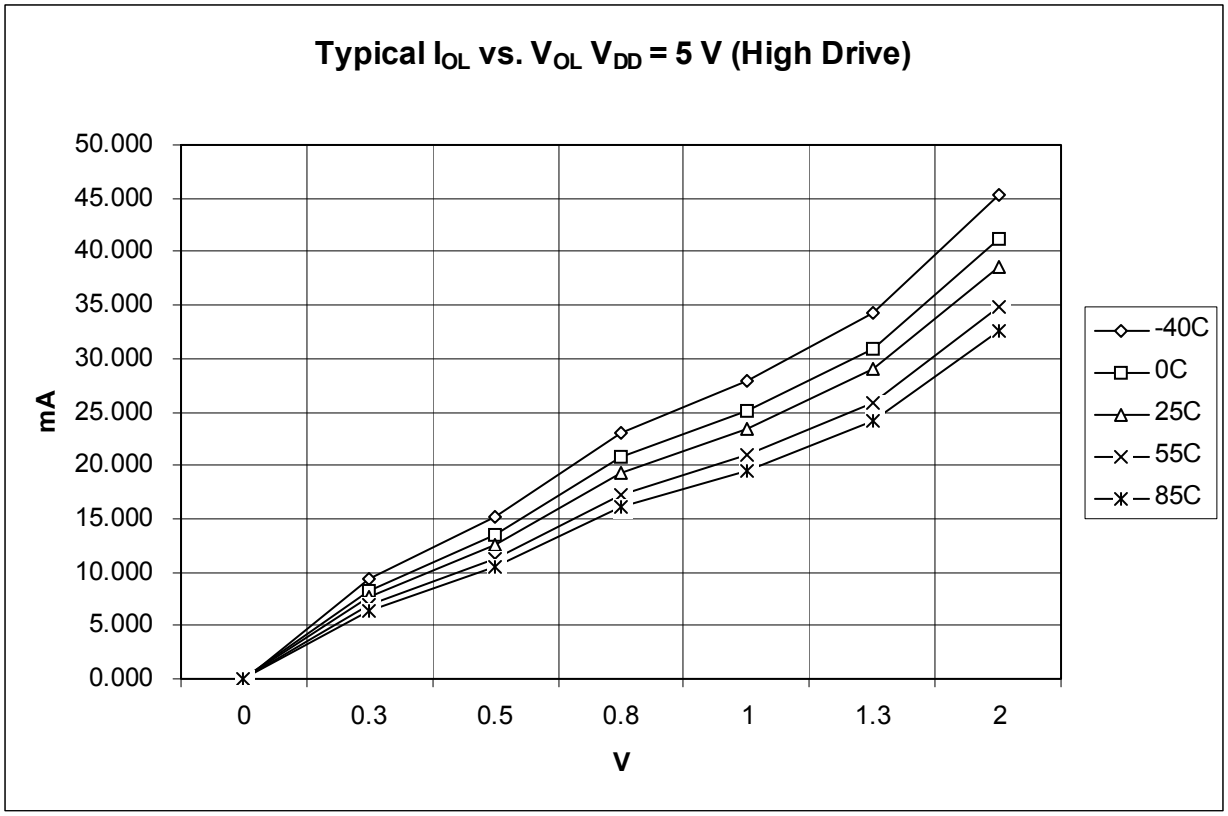



**Figure 8. Typical $I_{OH}$ Vs $V_{OL}$ ($V_{DD}$ = 5.0 V) (High Drive)**

**Table 9. XOSC and ICS Specifications (Temperature Range = –40 to 85 °C Ambient) (continued)**

| Num | C | Characteristic | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| 13 | C | Long term jitter of DCO output clock (averaged over 2 ms interval) [8] | $C_{Jitter}$ | — | 0.02 | 0.2 | $\%f_{dco}$ |

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 See crystal or resonator manufacturer's recommendation.

4 This parameter is characterized and not tested on each device.

5 Proper PC board layout procedures must be followed to achieve specifications.

6 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

7 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{Bus}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via $V_{DD}$ and $V_{SS}$ and variation in crystal oscillator frequency increase the $C_{Jitter}$ percentage for a given interval.

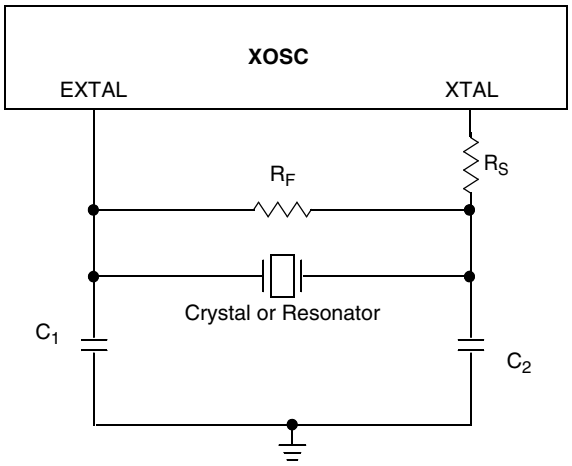



**Figure 10. Typical Crystal or Resonator Circuit**

## 5.9.1 Control Timing

**Table 10. Control Timing**

| Num | C | Rating | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | D | Bus frequency ($t_{cyc} = 1/f_{Bus}$) | $f_{Bus}$ | dc | — | 10 | MHz |
| 2 | D | Internal low power oscillator period | $t_{LPO}$ | 700 | — | 1300 | µs |
| 3 | D | External reset pulse width[2] | $t_{extrst}$ | 100 | — | — | ns |
| 4 | D | Reset low drive | $t_{rstdrv}$ | $34 \times t_{cyc}$ | — | — | ns |
| 5 | D | BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes | $t_{MSSU}$ | 500 | — | — | ns |
| 6 | D | BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[3] | $t_{MSH}$ | 100 | — | — | µs |
| 7 | D | IRQ pulse width<br>Asynchronous path[2]<br>Synchronous path[4] | $t_{ILIH}$, $t_{IHIL}$ | 100<br>$1.5 \times t_{cyc}$ | —<br>— | —<br>— | ns |
| 8 | D | Keyboard interrupt pulse width<br>Asynchronous path[2]<br>Synchronous path[4] | $t_{ILIH}$, $t_{IHIL}$ | 100<br>$1.5 \times t_{cyc}$ | —<br>— | —<br>— | ns |
| 9 | C | Port rise and fall time —<br>Low output drive (PTxDS = 0) (load = 50 pF)[5]<br>Slew rate control disabled (PTxSE = 0)<br>Slew rate control enabled (PTxSE = 1) | $t_{Rise}$, $t_{Fall}$ | <br><br>—<br>— | <br><br>16<br>23 | <br><br>—<br>— | ns |
| | | Port rise and fall time —<br>High output drive (PTxDS = 1) (load = 50 pF)[5]<br>Slew rate control disabled (PTxSE = 0)<br>Slew rate control enabled (PTxSE = 1) | $t_{Rise}$, $t_{Fall}$ | <br><br>—<br>— | <br><br>5<br>9 | <br><br>—<br>— | ns |

1 Typical values are based on characterization data at $V_{DD}$ = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS must be held low during the power-up and for a hold time of $t_{MSH}$ after $V_{DD}$ rises above $V_{LVD}$.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ levels. Temperature range –40 °C to 85 °C.

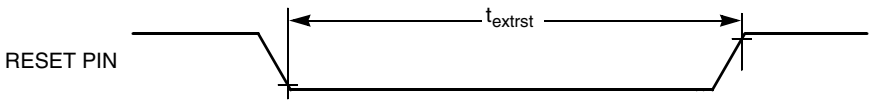



**Figure 12. Reset Timing**

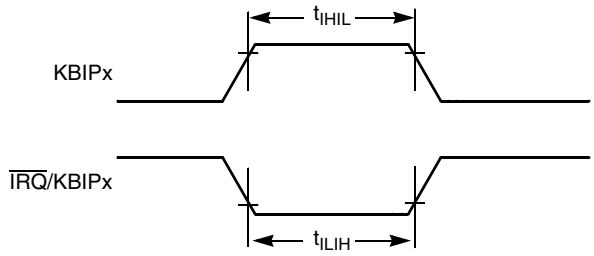



**Figure 13. IRQ/KBIPx Timing**

## 5.9.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table 11. TPM Input Timing**

| No. | C | Function | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | D | External clock frequency | $f_{TCLK}$ | 0 | $f_{Bus}/4$ | Hz |
| 2 | D | External clock period | $t_{TCLK}$ | 4 | — | $t_{cyc}$ |
| 3 | D | External clock high time | $t_{clkh}$ | 1.5 | — | $t_{cyc}$ |
| 4 | D | External clock low time | $t_{clkl}$ | 1.5 | — | $t_{cyc}$ |
| 5 | D | Input capture pulse width | $t_{ICPW}$ | 1.5 | — | $t_{cyc}$ |

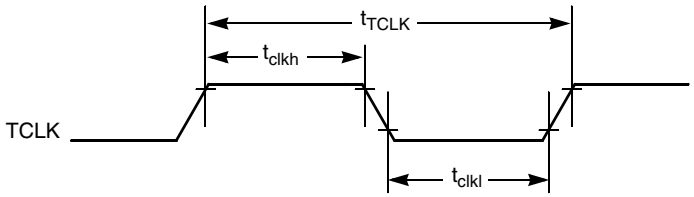



**Figure 14. Timer External Clock**

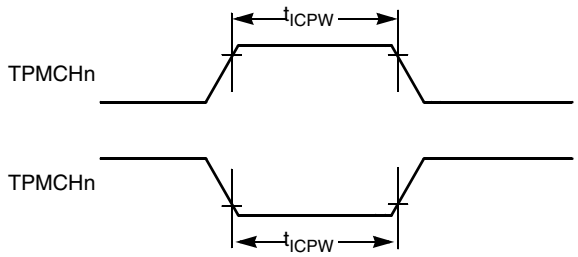



**Figure 15. Timer Input Capture Pulse**

## 5.10 ADC Characteristics

**Table 12. 8-Bit ADC Operating Conditions**

| Characteristic | Conditions | Symb | Min | Typical[1] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| Supply voltage | Absolute | $V_{DDA}$ | 4.5 | — | 5.5 | V | |
| | Delta to $V_{DD}$ ($V_{DD} - V_{DDA}$)[2] | $\Delta V_{DDA}$ | –100 | 0 | 100 | mV | |
| Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSA}$)[2] | $\Delta V_{SSA}$ | –100 | 0 | 100 | mV | |
| Input voltage | — | $V_{ADIN}$ | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| Input capacitance | — | $C_{ADIN}$ | — | 4.5 | 5.5 | pF | |
| Input resistance | — | $R_{ADIN}$ | — | 3 | 5 | kΩ | |
| Analog source resistance | 8-bit mode (all valid $f_{ADCK}$) | $R_{AS}$ | — | — | 10 | kΩ | External to MCU |
| ADC conversion clock frequency | High speed (ADLPC = 0) | $f_{ADCK}$ | 0.4 | — | 8.0 | MHz | |
| | Low power (ADLPC = 1) | | 0.4 | — | 4.0 | | |

1 Typical values assume $V_{DDA}$ = 5.0 V, Temp = 25 °C, $f_{ADCK}$= 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

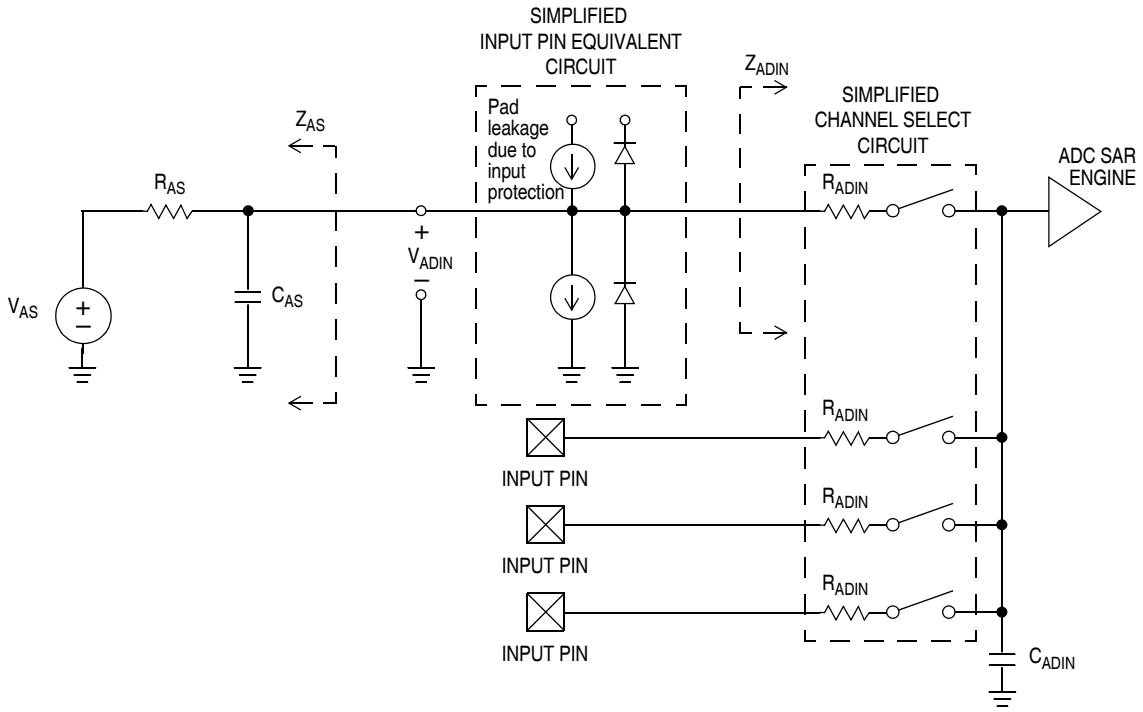



**Figure 16. ADC Input Impedance Equivalency Diagram**

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

## 5.12 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

### 5.12.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (the North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

**Table 15. Radiated Emissions, Electric Field**

| Parameter | Symbol | Conditions | Frequency | $f_{OSC}/f_{BUS}$ | Level[1] (Max) | Unit |
|---|---|---|---|---|---|---|
| Radiated emissions, electric field | $V_{RE\_TEM}$ | $V_{DD}$ = 5.0 V<br>$T_A$ = 25 °C<br>package type<br>32-pin LQFP | 0.15 – 50 MHz | 4 MHz crystal<br>19 MHz bus | 9 | dBµV |
| | | | 50 – 150 MHz | | 5 | |
| | | | 150 – 500 MHz | | 2 | |
| | | | 500 – 1000 MHz | | 1 | |
| | | | IEC Level | | N | — |
| | | | SAE Level | | 1 | — |

1 Data based on qualification test results.

# 6 Ordering Information

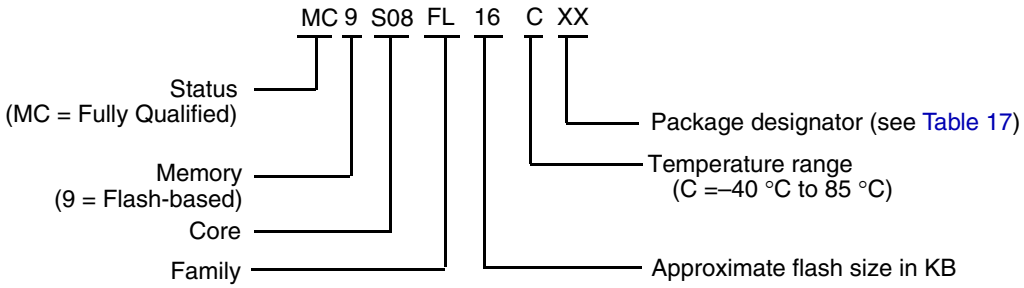
This section contains ordering information for MC9S08FL16 series devices. See below for an example of the device numbering system.

**Table 16. Device Numbering System**

| Device Number[1] | Memory | | Available Packages[2] |
|---|---|---|---|
| | FLASH | RAM | |
| MC9S08FL16 | 16 KB | 1024 | 32 SDIP<br>32 LQFP |
| MC9S08FL8 | 8 KB | 768 | |

1 See the reference manual, *MC9S08FL16 Series Reference Manual*, for a complete description of modules included on each device.
2 See Table 17 for package information.

Example of the device numbering system:




# 7 Package Information

**Table 17. Package Descriptions**

| Pin Count | Package Type | Abbreviation | Designator | Case No. | Document No. |
|---|---|---|---|---|---|
| 32 | Low Quad Flat Package | LQFP | LC | 873A-03 | 98ASH70029A |
| 32 | Shrink Dual In-line Package | SDIP | BM | 1376-02 | 98ASA99330D |

## 7.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 17.

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