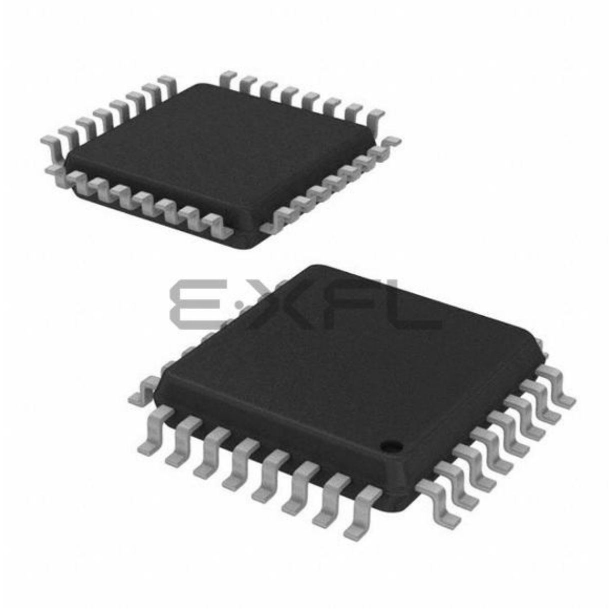
NXP USA Inc. - MC9S08FL8CLCR Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	SCI
Peripherals	LVD, PWM, WDT
Number of I/O	30
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08fl8clcr

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	March 18, 2009	Initial public release.
2	July 20, 2009	Updated Section 5.12, “EMC Performance.” and corrected Figure 1 and Table 1. Corrected default trim value to 31.25 kHz.
3	Nov. 29, 2010	Updated Table 7.
4	May, 2015	Corrected pin 12 of the Figure 3.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual **(MC9S08FL16RM)**

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of MC9S08FL16 series MCU.

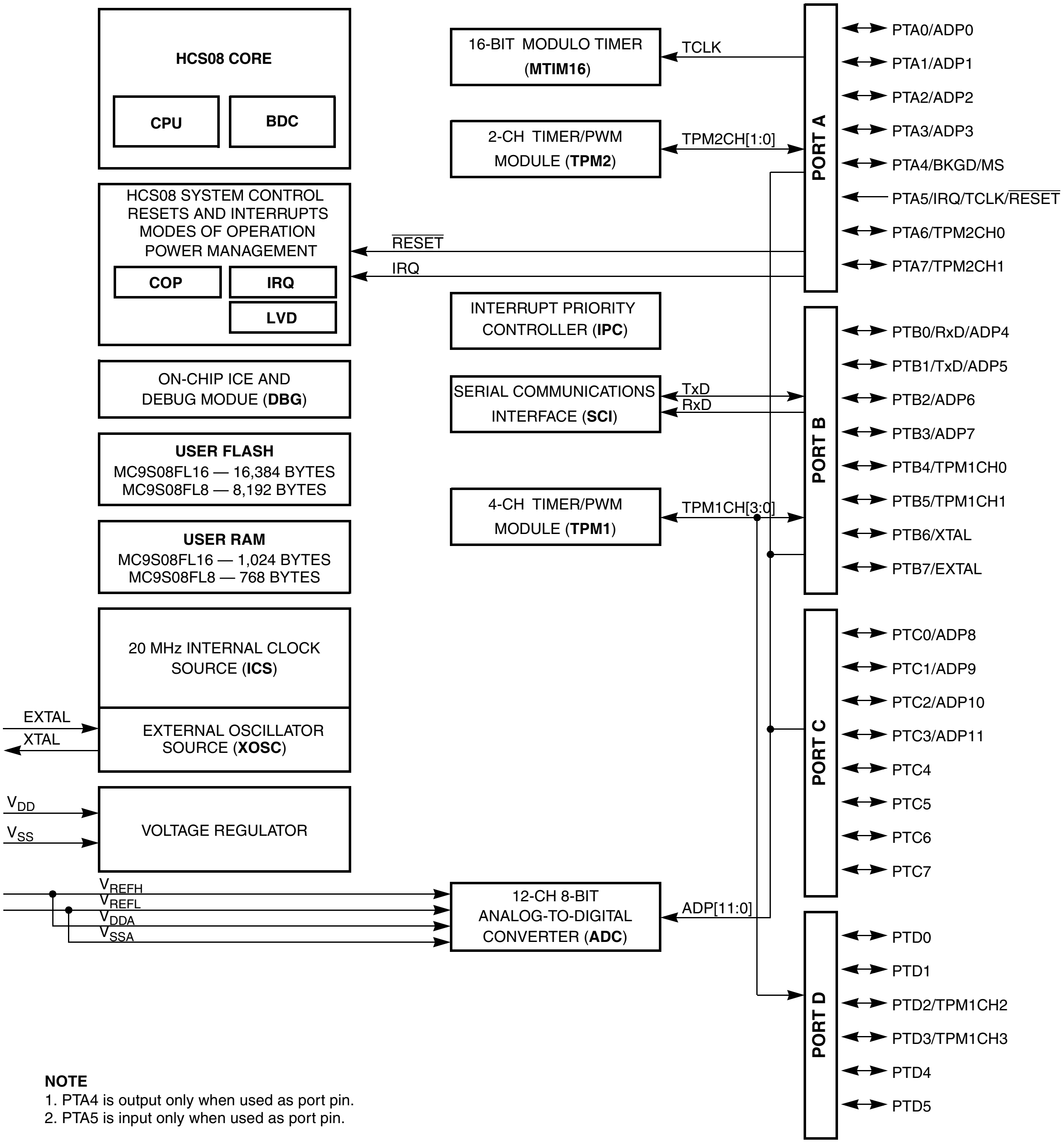


Figure 1. MC9S08FL16 Series Block Diagram

2 System Clock Distribution

MC9S08FL16 series use ICS module as clock sources. The ICS module can use internal or external clock source as reference to provide up to 20 MHz CPU clock. The output of ICS module includes,

- OSCOUT — XOSC output provides external reference clock to ADC.
- ICSFFCLK — ICS fixed frequency clock reference (around 32.768 kHz) provides double of the fixed lock signal to TPMs and MTIM16.
- ICSOUT — ICS CPU clock provides double of the bus clock which is basic clock reference of peripherals.
- ICSLCLK — Alternate BDC clock provides debug signal to BDC module.

The TCLK pin is an extra external clock source. When TCLK is enabled, it can provide alternate clock source to TPMs and MTIM16. The on-chip 1 kHz clock provides clock source of COP module.

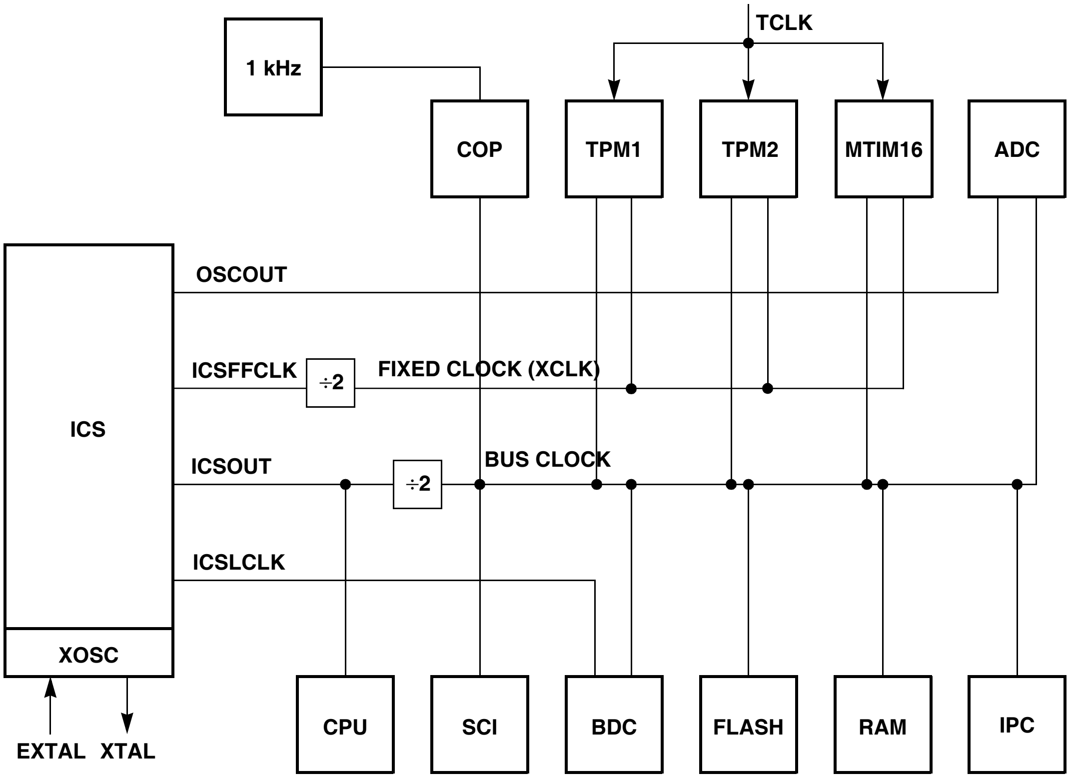


Figure 2. System Clock Distribution Diagram

3 Pin Assignments

This section shows the pin assignments for the MC9S08FL16 series devices.

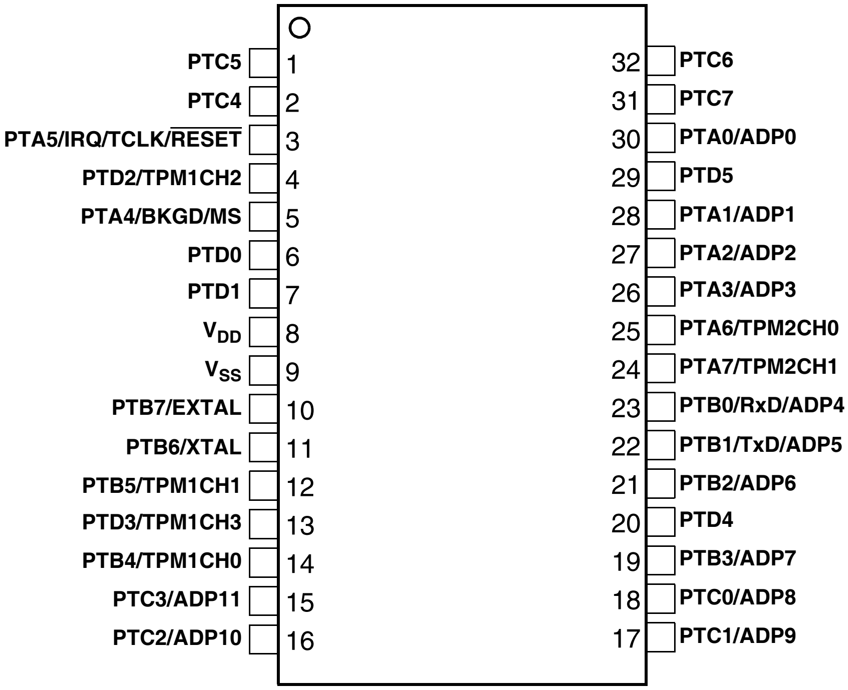


Figure 3. MC9S08FL16 Series 32-Pin SDIP Package

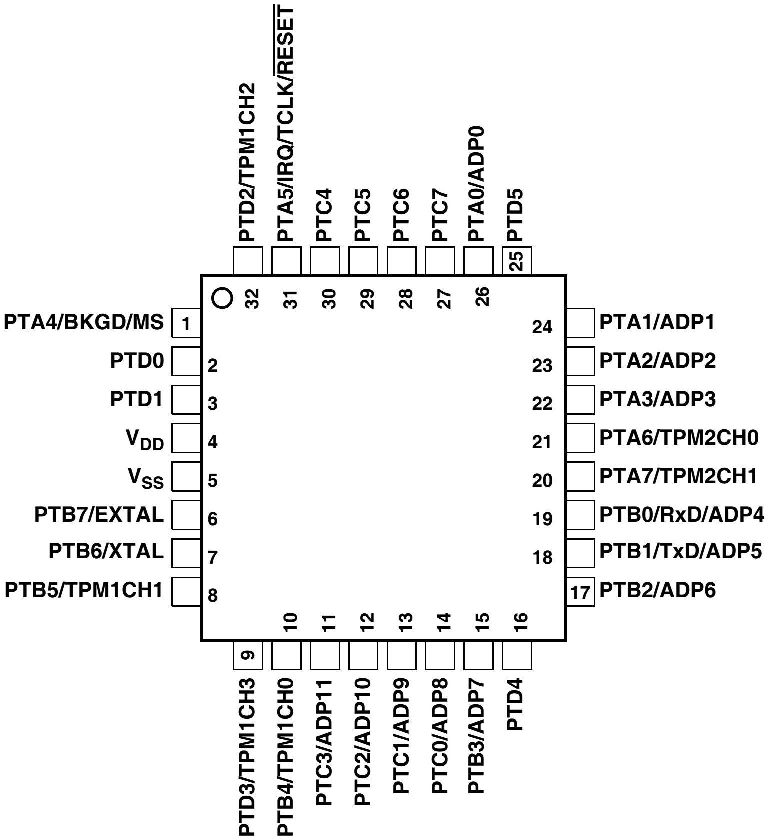


Figure 4. MC9S08FL16 Series 32-Pin LQFP Package

Table 1. Pin Availability by Package Pin-Count

Pin Number		<-- Lowest **Priority** --> Highest							
32-SDIP	**32-LQFP**	**Port Pin**	**I/O**	**Alt 1**	**I/O**	**Alt 2**	**I/O**	**Alt 3**	**I/O**
1	29	PTC5	I/O						
2	30	PTC4	I/O						
3	31	PTA5	I	IRQ	I	TCLK	I	$\overline{\text{RESET}}$	I
4	32	PTD2	I/O			TPM1CH2	I/O		
5	1	PTA4	O			BKGD	I	MS	I
6	2	PTD0	I/O						
7	3	PTD1	I/O						
8	4							V_{DD}	I
9	5							V_{SS}	I
10	6	PTB7	I/O	EXTAL	I				
11	7	PTB6	I/O	XTAL	O				
12	8	PTB5	I/O			TPM1CH1	I/O		
13	9	PTD3	I/O			TPM1CH3	I/O		
14	10	PTB4	I/O			TPM1CH0	I/O		
15	11	PTC3	I/O			ADP11	I		

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number		<-- Lowest **Priority** --> Highest							
32-SDIP	**32-LQFP**	**Port Pin**	**I/O**	**Alt 1**	**I/O**	**Alt 2**	**I/O**	**Alt 3**	**I/O**
16	12	PTC2	I/O			ADP10	I		
17	13	PTC1	I/O			ADP9	I		
18	14	PTC0	I/O			ADP8	I		
19	15	PTB3	I/O			ADP7	I		
20	16	PTD4	I/O						
21	17	PTB2	I/O			ADP6	I		
22	18	PTB1	I/O			TxD	I/O	ADP5	I
23	19	PTB0	I/O			RxD	I	ADP4	I
24	20	PTA7	I/O			TPM2CH1	I/O		
25	21	PTA6	I/O			TPM2CH0	I/O		
26	22	PTA3	I/O			ADP3	I		
27	23	PTA2	I/O			ADP2	I		
28	24	PTA1	I/O			ADP1	I		
29	25	PTD5	I/O						
30	26	PTA0	I/O			ADP0	I		
31	27	PTC7	I/O						
32	28	PTC6	I/O						

NOTE

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear out any associated flags before interrupts are enabled. Table 1 illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

4 Memory Map

Figure 5 shows the memory map for the MC9S08FL16 series. On-chip memory in the MC9S08FL16 series of MCUs consists of RAM, flash program memory for nonvolatile data storage, plus I/O and control/status registers. The registers are divided into two groups:

- Direct-page registers (0x0000 through 0x003F)
- High-page registers (0x1800 through 0x187F)

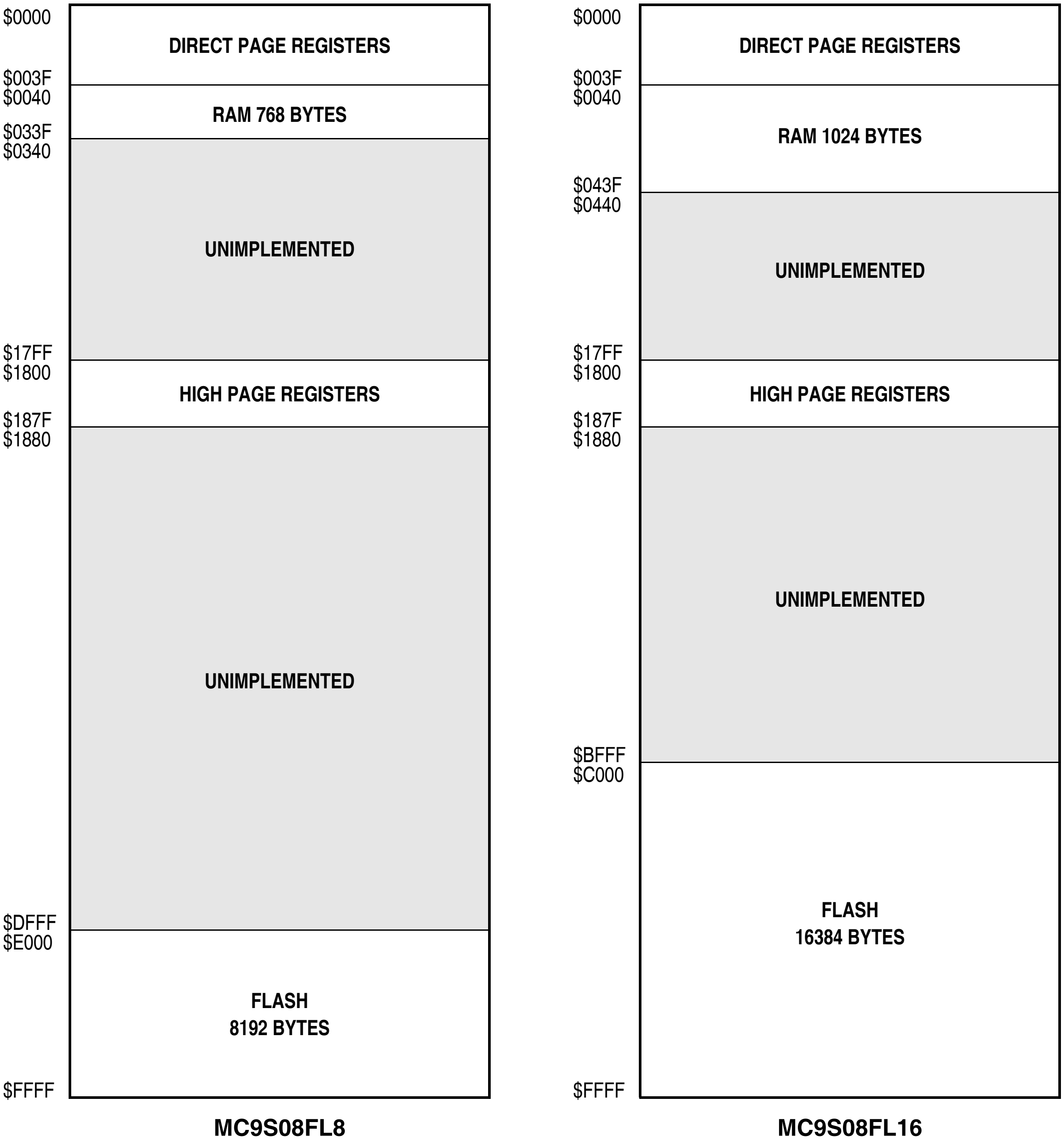


Figure 5. MC9S08FL16 Series Memory Map

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

5.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Thermal resistance Single-layer board			
32-pin SDIP	θ_{JA}	60	°C/W
32-pin LQFP		85	
Thermal resistance Four-layer board			
32-pin SDIP	θ_{JA}	35	°C/W
32-pin LQFP		56	

The average chip-junction temperature (T_J) in °C can be obtained from:

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

5.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min.	Typical[1]	Max.	Unit
1	P	Operating voltage		—	—	4.5	—	5.5	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	I_{Load} = –2 mA	V_{DD} – 1.5	—	—	V
	P		All I/O pins, high-drive strength		I_{Load} = –10 mA	V_{DD} – 1.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	I_{Load} = 2 mA	—	—	1.5	V
	P		All I/O pins, high-drive strength		I_{Load} = 10 mA	—	—	1.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	—	100	mA
6	P	Input high voltage	All digital inputs	V_{IH}	—	0.65 × V_{DD}	—	—	V
7	P	Input low voltage	All digital inputs	V_{IL}	—	—	—	0.35 × V_{DD}	V
8	C	Input hysteresis	All digital inputs	V_{hys}	—	0.06 × V_{DD}	—	—	mV
9	P	Input leakage current	All input only pins (per pin)	$\|I_{In}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	0.1	1	µA
10	P	Hi-Z (off-state) leakage current	All input/output (per pin)	$\|I_{OZ}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	0.1	1	µA
11a	C	Pullup, pulldown resistors	All digital inputs, when enabled (all I/O pins other than PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD}	—	17.5	36.5	52.5	kΩ
11b	C	Pullup, pulldown resistors	(PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD} (Note[2])	—	17.5	36.5	52.5	kΩ

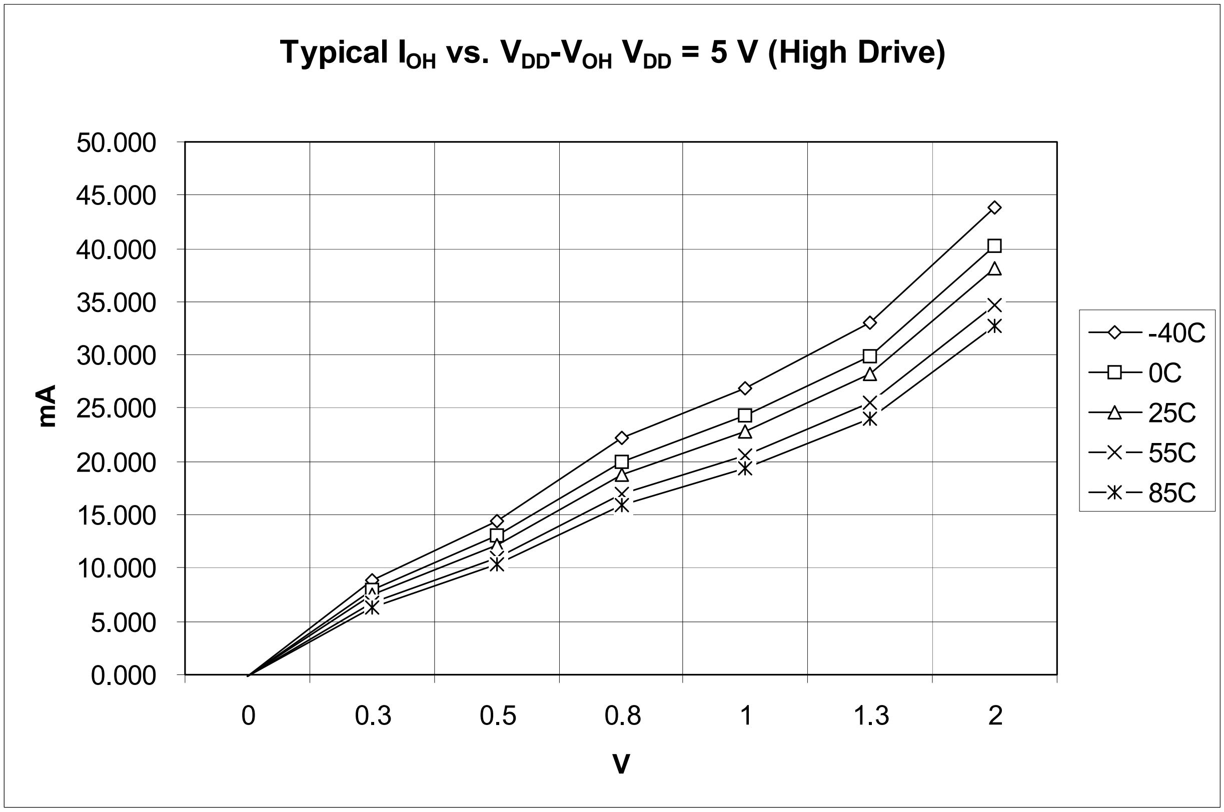


Figure 6. Typical I_{OH} Vs V_{DD}–V_{OH} (V_{DD} = 5.0 V) (High Drive)

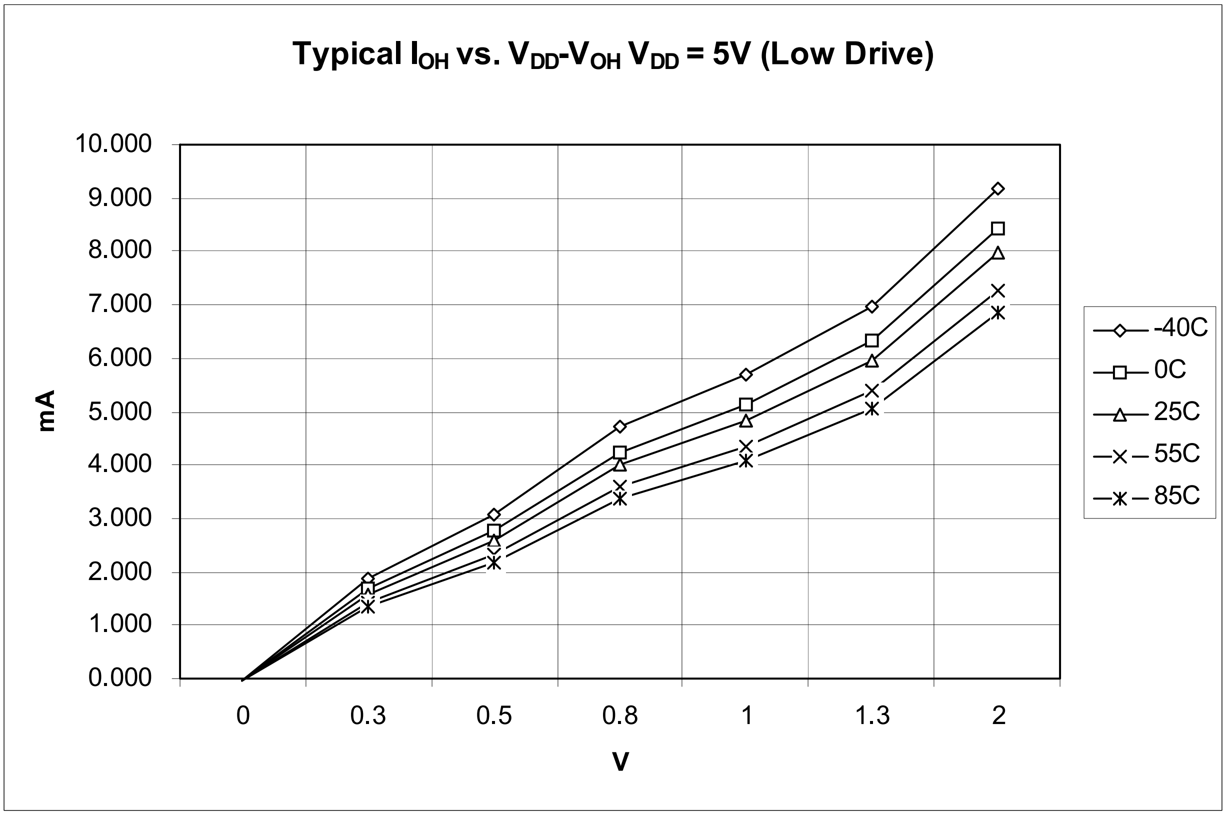


Figure 7. Typical I_{OH} Vs V_{DD}–V_{OH} (V_{DD} = 5.0 V) (Low Drive)

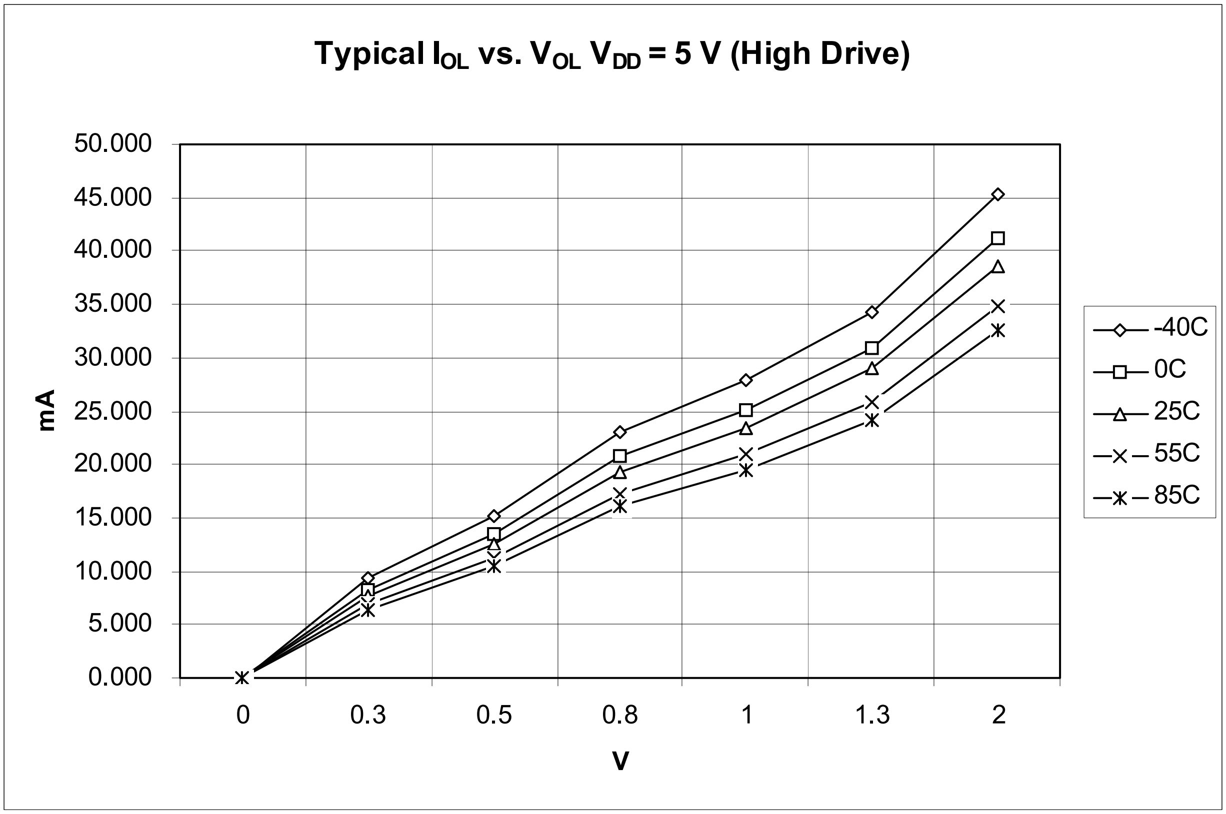


Figure 8. Typical I_{OH} Vs V_{OL} (V_{DD} = 5.0 V) (High Drive)

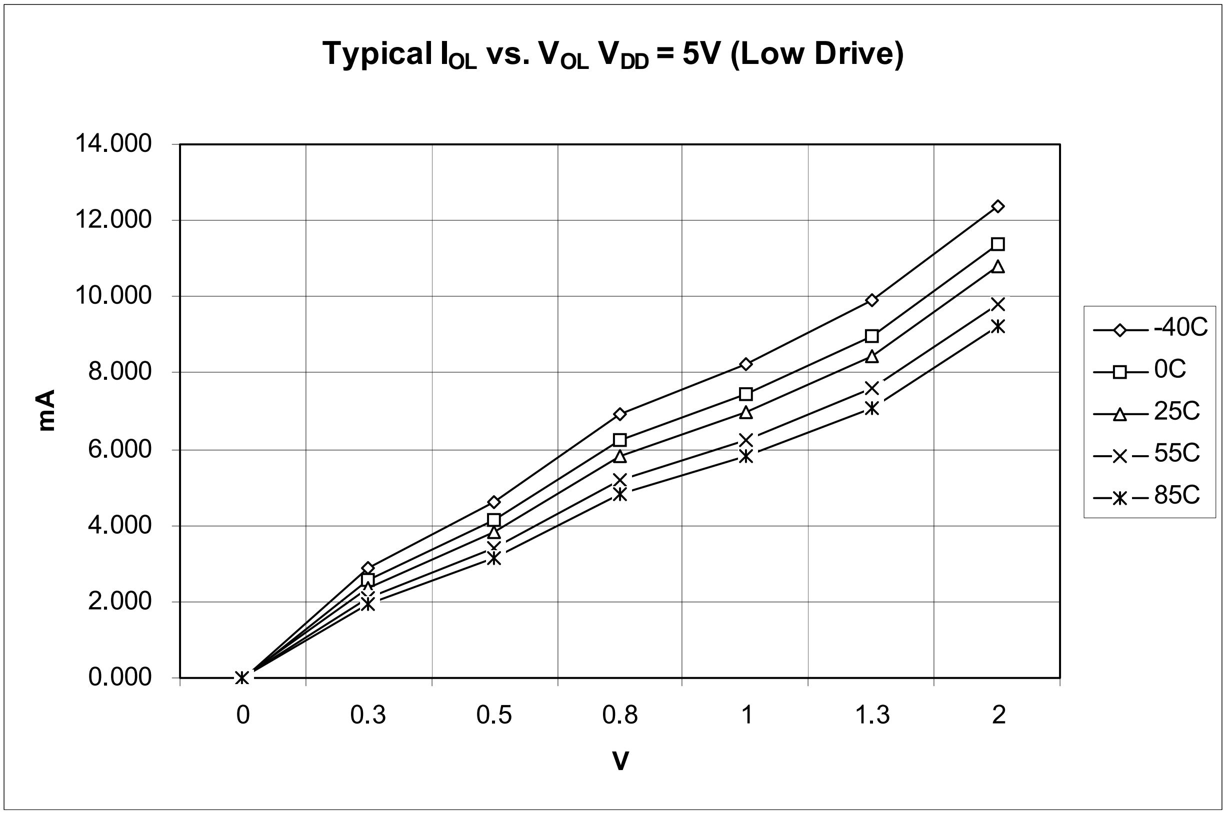


Figure 9. Typical I_{OH} Vs V_{OL} (V_{DD} = 5.0 V) (Low Drive)

5.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	P	Run supply current FEI mode, all modules off	RI_{DD}	10 MHz	5	5.66 5.75 5.80	—	mA	–40 °C 25 °C 85 °C
	P			1 MHz		1.61 1.65 1.78	—		–40 °C 25 °C 85 °C
2	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	10 MHz	5	2.79 2.86 2.88	—	µA	–40 °C 25 °C 85 °C
	C			1 MHz		1.05 1.06 1.06	—		–40 °C 25 °C 85 °C
3	C	Stop2 mode supply current	$S2I_{DD}$	—	5	1.06	—	µA	–40 to 85 °C
	C	Stop3 mode supply current no clocks active	$S3I_{DD}$	—	5	1.17	—	µA	–40 to 85 °C
4	C	ADC adder to stop3	—	—	5	163.88	—	µA	25 °C
5	C	ICS adder to stop3 EREFSTEN = 1	—	—	5	1.25	—	µA	25 °C
6	C	LVD adder to stop3	—	—	5	161.3	—	µA	25 °C

[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

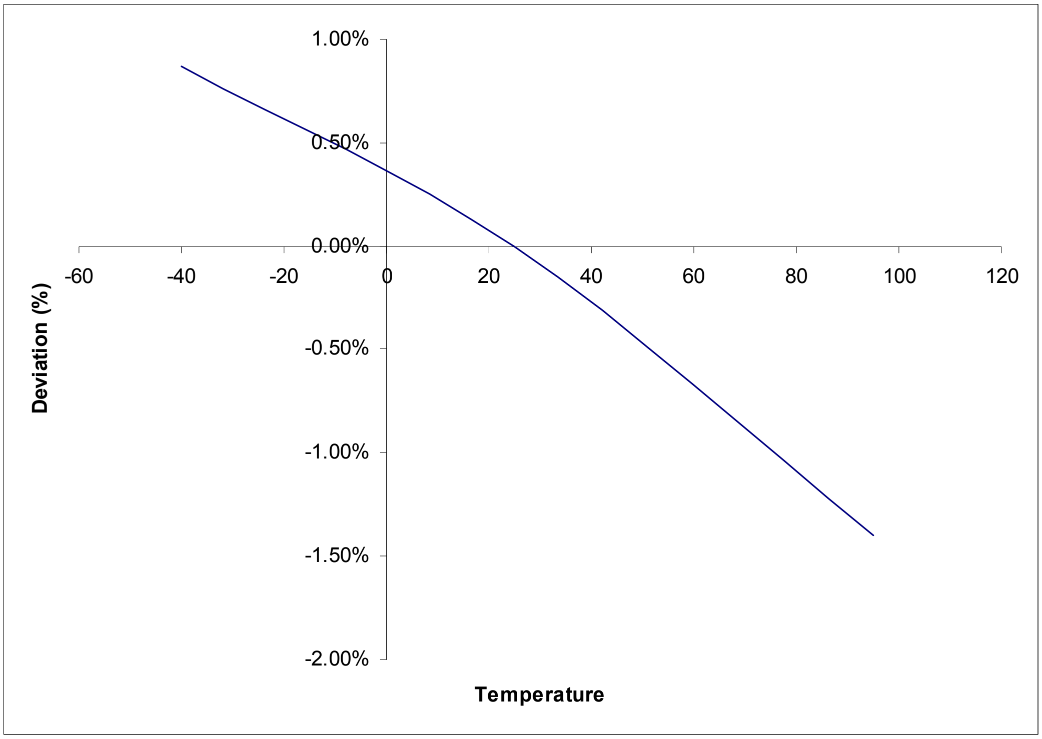


Figure 11. Deviation of DCO Output from Trimmed Frequency (20 MHz, 5.0 V)

5.9 AC Characteristics

This section describes timing characteristics for each peripheral system.

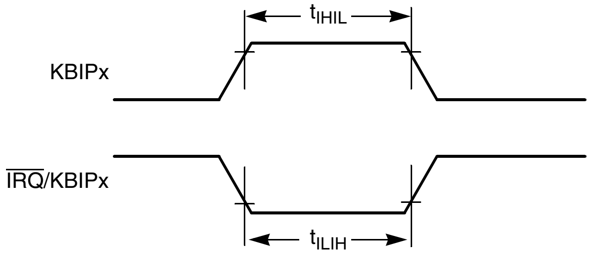


Figure 13. $\overline{\text{IRQ}}$/KBIPx Timing

5.9.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

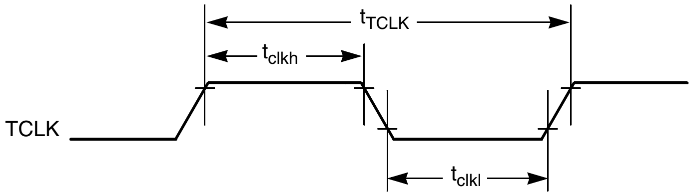


Figure 14. Timer External Clock

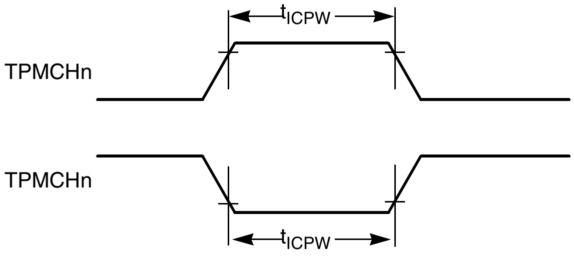


Figure 15. Timer Input Capture Pulse

5.10 ADC Characteristics

Table 12. 8-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	4.5	—	5.5	V	
	Delta to V_{DD} ($V_{DD} – V_{DDA}$)[2]	ΔV_{DDA}	–100	0	100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS} – V_{SSA}$)[2]	ΔV_{SSA}	–100	0	100	mV	
Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF	
Input resistance	—	R_{ADIN}	—	3	5	kΩ	
Analog source resistance	8-bit mode (all valid f_{ADCK})	R_{AS}	—	—	10	kΩ	External to MCU
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

[1] Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK}= 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

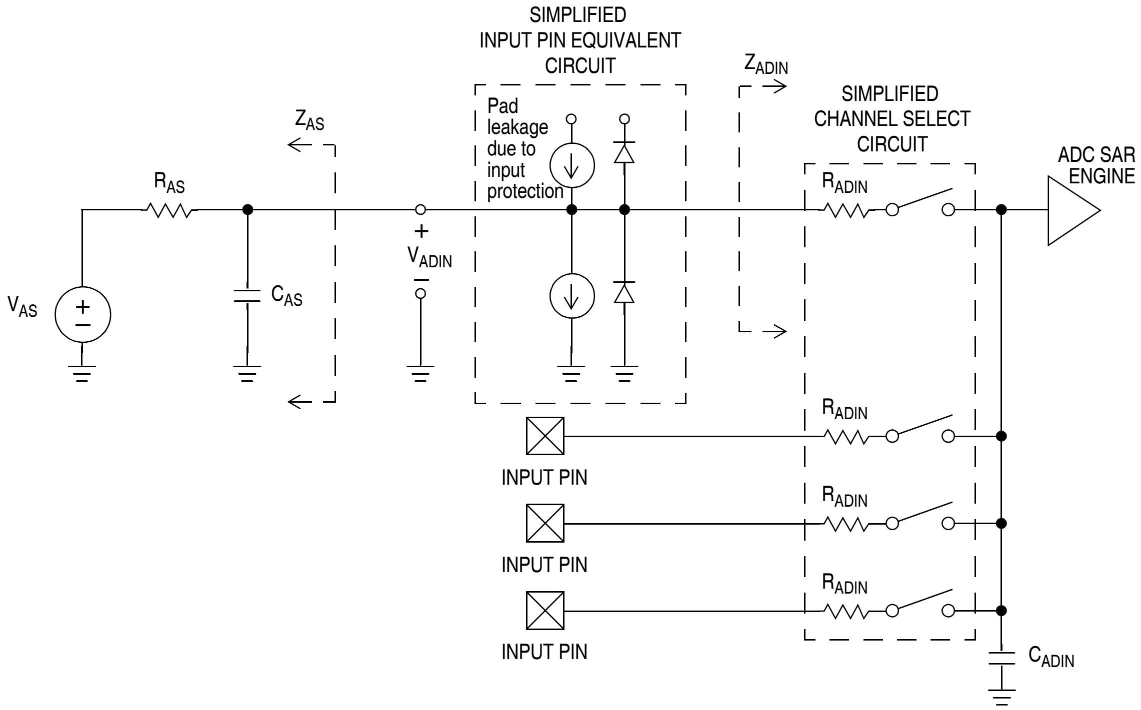


Figure 16. ADC Input Impedance Equivalency Diagram

Table 13. 8-Bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Quantization Error	8-bit mode	E_Q	—	—	±0.5	LSB[2]	
D	Input Leakage Error	8-bit mode	E_{IL}	—	±0.1	±1	LSB[2]	Pad leakage[2] * R_{AS}

[1] Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] Based on input pad leakage current. Refer to pad electricals.

5.11 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 14. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	4.5	—	5.5	V
D	Supply voltage for read operation	V_{Read}	4.5	—	5.5	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
P	Byte program time (random location)[2]	t_{prog}		9		t_{Fcyc}
P	Byte program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}
P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
P	Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}
	Byte program current[3]	RI_{DDBP}	—	4	—	mA
	Page erase current[3]	RI_{DDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40 °C to 85 °C T = 25 °C		—	10,000	—	cycles
C	Data retention[5]	t_{D_ret}	5	100	—	years

[1] The frequency of this clock is controlled by a software setting.

[2] These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

[3] The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 5.0 V, bus frequency = 4.0 MHz.

[4] **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

[5] **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

5.12 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

5.12.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (the North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 15. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5.0 V T_A = 25 °C package type 32-pin LQFP	0.15 – 50 MHz	4 MHz crystal 19 MHz bus	9	dBμV
			50 – 150 MHz		5	
			150 – 500 MHz		2	
			500 – 1000 MHz		1	
			IEC Level		N	—
			SAE Level		1	—

[1] Data based on qualification test results.

6 Ordering Information

This section contains ordering information for MC9S08FL16 series devices. See below for an example of the device numbering system.

Table 16. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	FLASH	RAM	
MC9S08FL16	16 KB	1024	32 SDIP 32 LQFP
MC9S08FL8	8 KB	768	