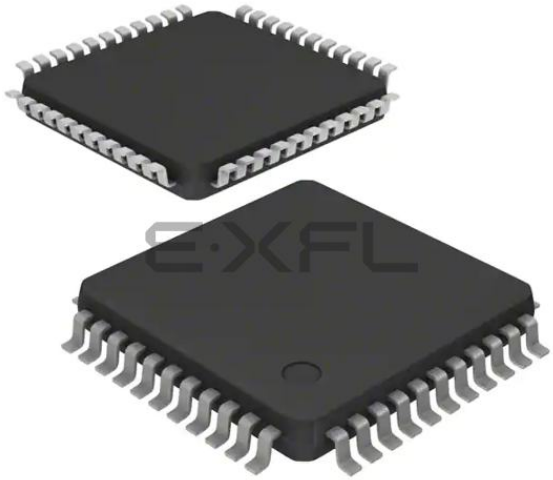

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9116aeg

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ZiLOG Worldwide Headquarters
532 Race Street
Campbell, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
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- Six Vectored, Prioritized Interrupts from Eight Different Sources
- Two Programmable 8-Bit Counter/Timers, each with two 6-Bit Programmable Prescalers
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock
- Two Standby Modes: STOP and HALT
- Auto Latches

Table 12. 40-Pin DIP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
11	GND	Ground, V_{SS}	Output
12	P32	Port 3, Pin 2	Input
13-20	P00-P07	Port 0, Pins 0-7	Input/Output
21-28	P10-P17	Port 3, Pins 0-7	Input/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P20-P27	Port 2, Pins 0-7	Input/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

Pin Functions

The following paragraphs describe the function of each available Z86C91 pin.

$\overline{\text{DS}}$ (output, active Low). The Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). The Address Strobe is pulsed one time at the beginning of each machine cycle for external memory transfer. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and READ/WRITE.

XTAL1 (Crystal 1)Time-Based Oscillator Input. This pin connects a parallel-resonant crystal, ceramic resonator, LC network, or an external single-phase clock to the on-chip oscillatorand buffer.

XTAL2 (Crystal 2) Time-Based Oscillator Output. This pin connects a parallel-resonant crystal, ceramic resonant, LC network to the on-chip oscillator and buffer.

R/$\overline{\text{W}}$ (output, WRITE Low). The READ/WRITE signal is Low when the Z8 writes to external data memory.

$\overline{\text{RESET}}$ (input, Low). To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external XTAL clocks (4TpC). If the external $\overline{\text{RESET}}$ signal is less than 4TpC in duration, reset does not occur.

On the fifth clock after $\overline{\text{RESET}}$ is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external $\overline{\text{RESET}}$, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. When $\overline{\text{RESET}}$ is deactivated, program execution begins at location 000Ch. Power-Up reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P00–P07). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03–P00 input/output and P07–P04 input/output), or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control $\overline{\text{DAV0}}$ and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04–P07. The lower nibble must indicate the same direction as the upper nibble.

For external memory references, Port 1 provides address bits A7–A0 (lower nibble) and Port 0 provides address bits A15–A8 (upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 is programmed independently as I/O while the lower nibble is used for addressing. If one or

Port 1 (P17–P10). Port 1 is an 8-bit, TTL- compatible port (Figure 6), with multiplexed Address (A7–A0) and Data (D7–D0) ports for interfacing external memory. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 6). A hardware RESET is required to exit this high-impedance state.

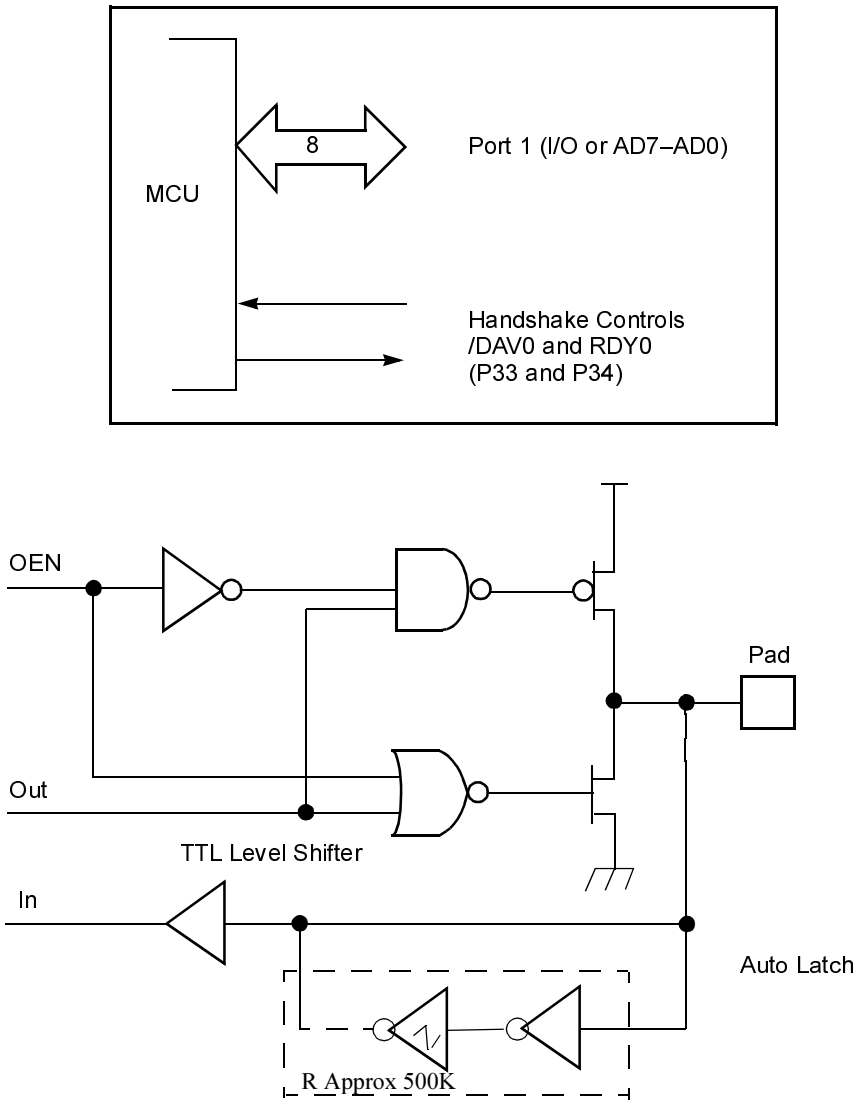


Figure 6. Port 1 Configuration

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

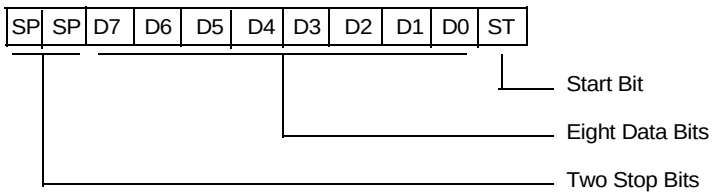


Figure 9. Transmitted Data (No Parity)

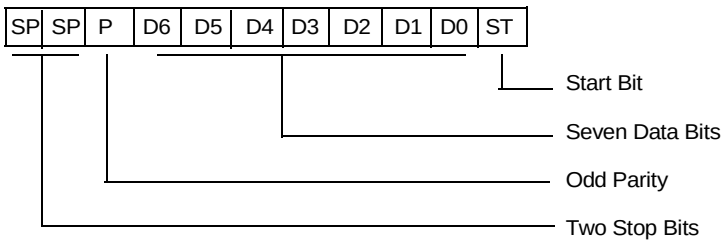


Figure 10. Transmitted Data (With Parity)

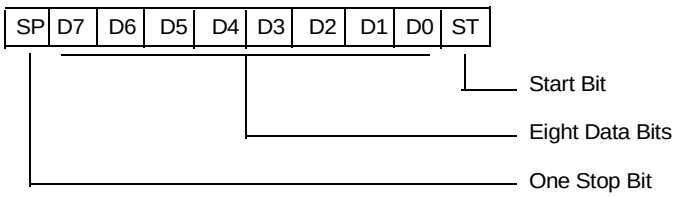


Figure 11. Received Data (No Parity)

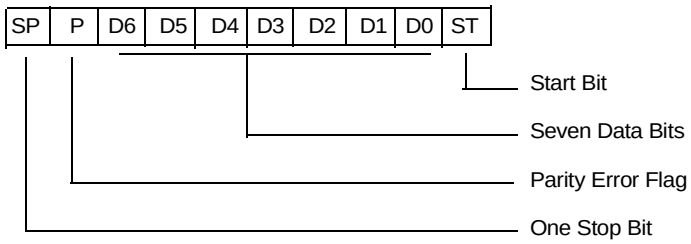


Figure 12. Received Data (With Parity)

Functional Description

The Z8 MCU incorporates the following functions that enhance the standard Z8® architecture and provide the user with increased design flexibility:

- Reset
- Program Memory
- Data Memory
- Working Register
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- HALT and STOP Modes
- Port Configuration Register

RESET. The device is reset in the following condition:

- External Reset

Automatic Power-On Reset circuitry is not built into this Z8. This Z8 requires an external reset circuit to reset upon power-up. The internal pull-up resistor is on the $\overline{\text{RESET}}$ pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a low-value pull-up resistor be used.

Program Memory. The Z86C91 can address up to 64 KB of external program memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location `000Ch` after reset. See Figure 13.

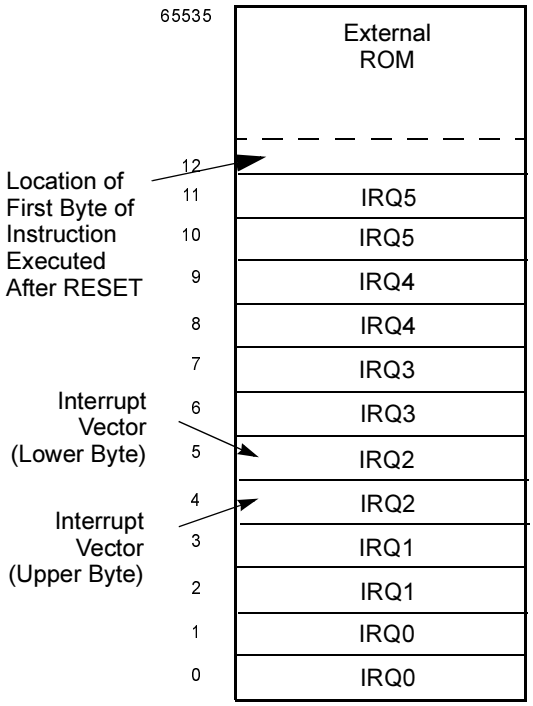


Figure 13. Program Memory Map

Data Memory ($\overline{DM}$). The Z86C91addresses up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that is programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode.

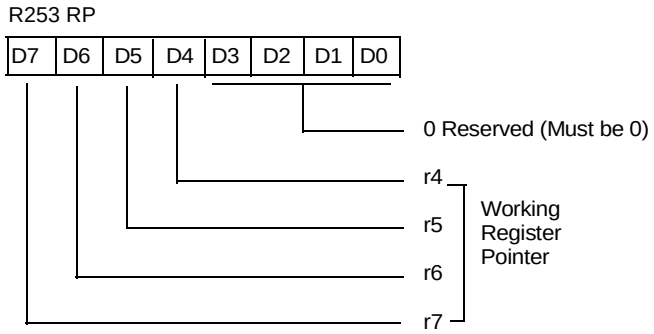


Figure 16. Register Pointer Register

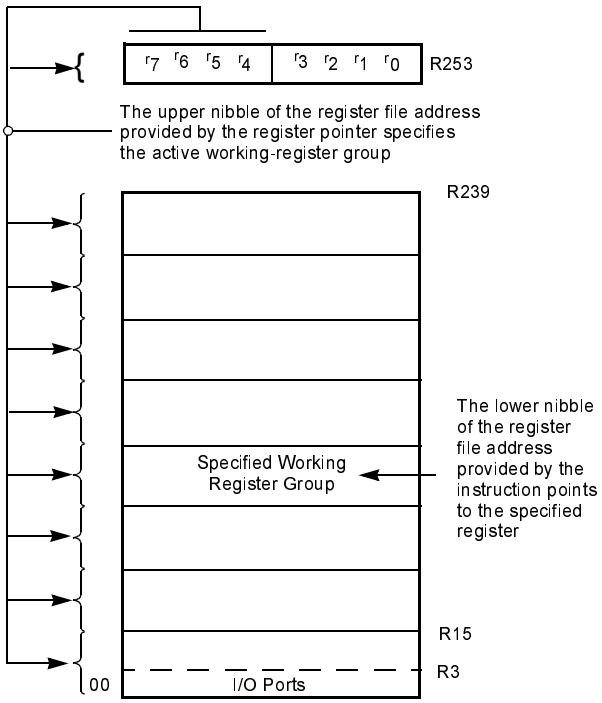


Figure 17. Register Pointer—Detail

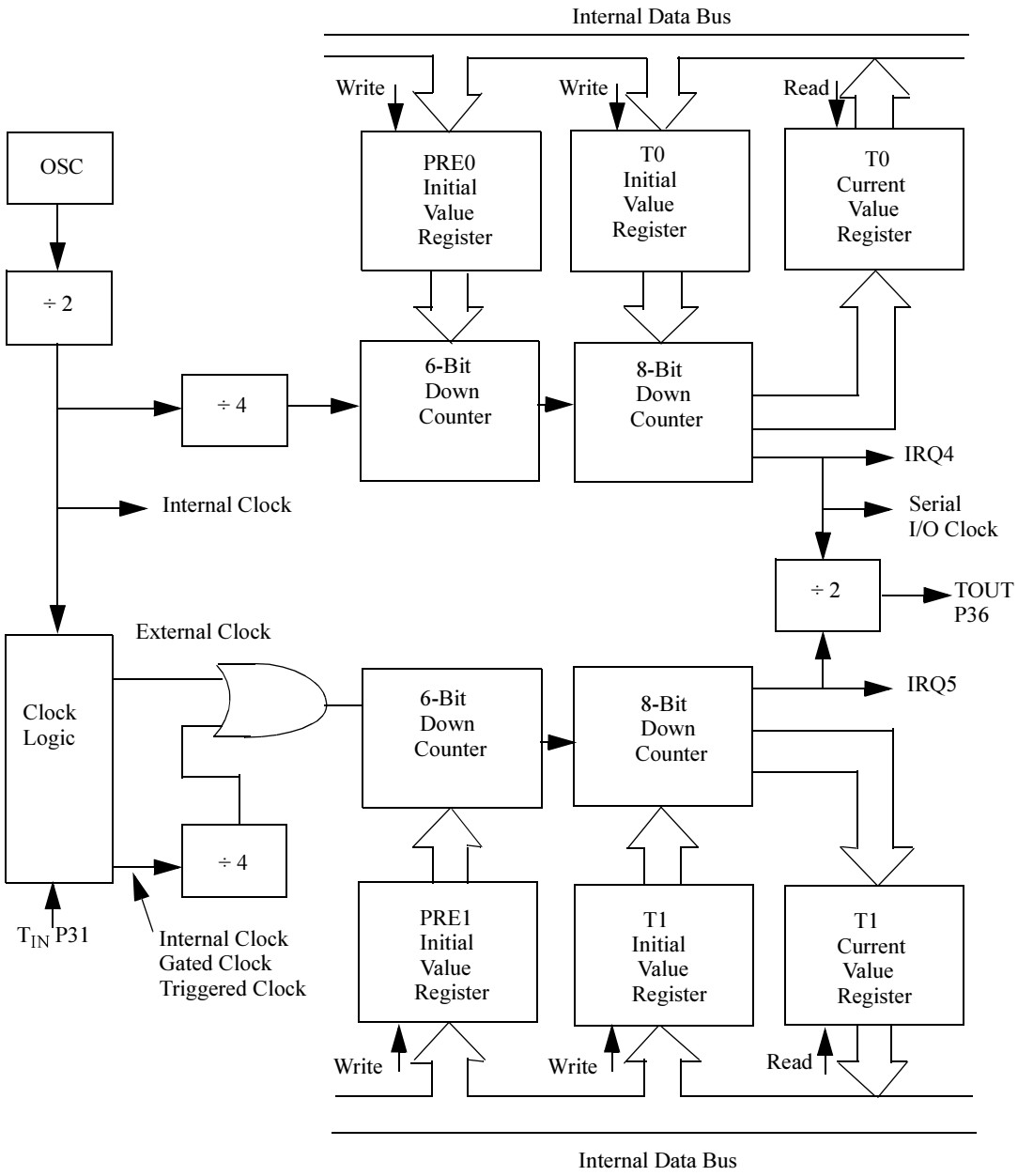


Figure 18. Counter/Timer Block Diagram

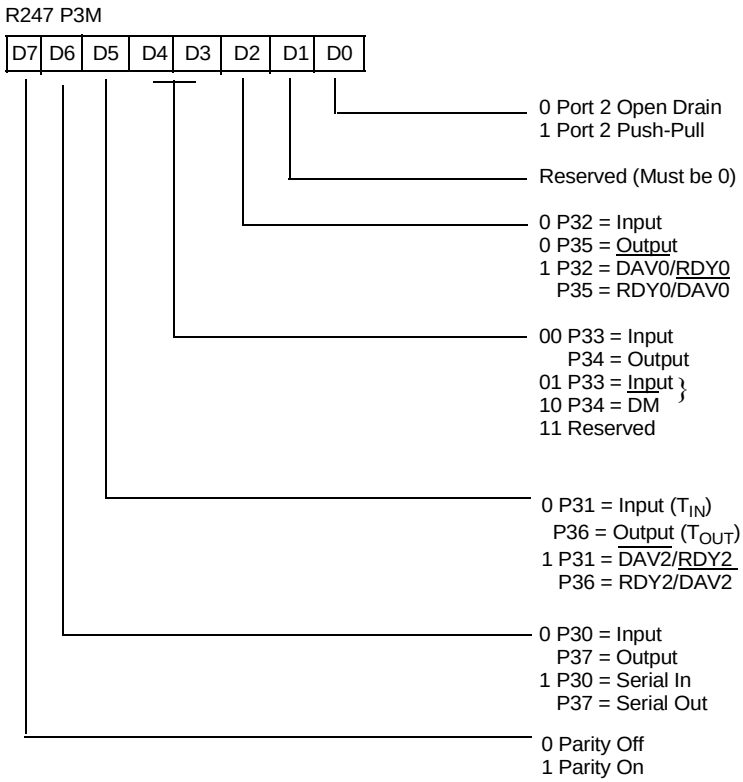


Figure 28. Port 3 Mode Register (F7h: Write Only)

Ports 0 and 1 Mode Register

The Ports 0 and 1 Mode Register, P01M, controls port and timing functions for Ports 0 and 1 and is shown in Figure 29.

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than the Absolute Maximum Ratings listed in Table 16 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STO}	Storage Temperature	–65	+150	C
T_A	Operating Ambient Temperature		[2]	C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 37).

Table 17. DC Electrical Characteristics at Standard and External Temperatures (Continued)

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical[2]		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@25°C**	**Units**	**Conditions**
V_{CL}	Clock Input Low Voltage	-0.3	0.8	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = -2.0 mA
V_{OH}	Output High Voltage	V_{CC}–100mV		V_{CC}–100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OH} = +2 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8	-0.3	0.8		V	
I_{IL}	Input Leakage	–2	2	-2	2		µA	Test at 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	-2	2		µA	Test at 0 V, V_{CC}
I_{IR}	Reset Input Current		–80		-80		µA	V_{RL}=0V
I_{CC}	Supply Current		35		35	24	mA	@ 16 MHz([1])
I_{CC1}	Standby Current		7		7	4.5	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		10	1	µA	STOP Mode V_{IN} = 0 V, V_{CC} ([1])
I_{ALL}	Autolatch Low Current	-10	10	-14	14		µA	

Note:
1. All inputs driven to 0V, V_{CC} and outputs floating.
2. V_{CC} = 5.0V

AC Electrical Characteristics

Figure 38 illustrates the timing characteristics of the Z86C91MCU with respect to external input/output sources. See Table 18 for descriptions of the numbered timing parameters in the figure.

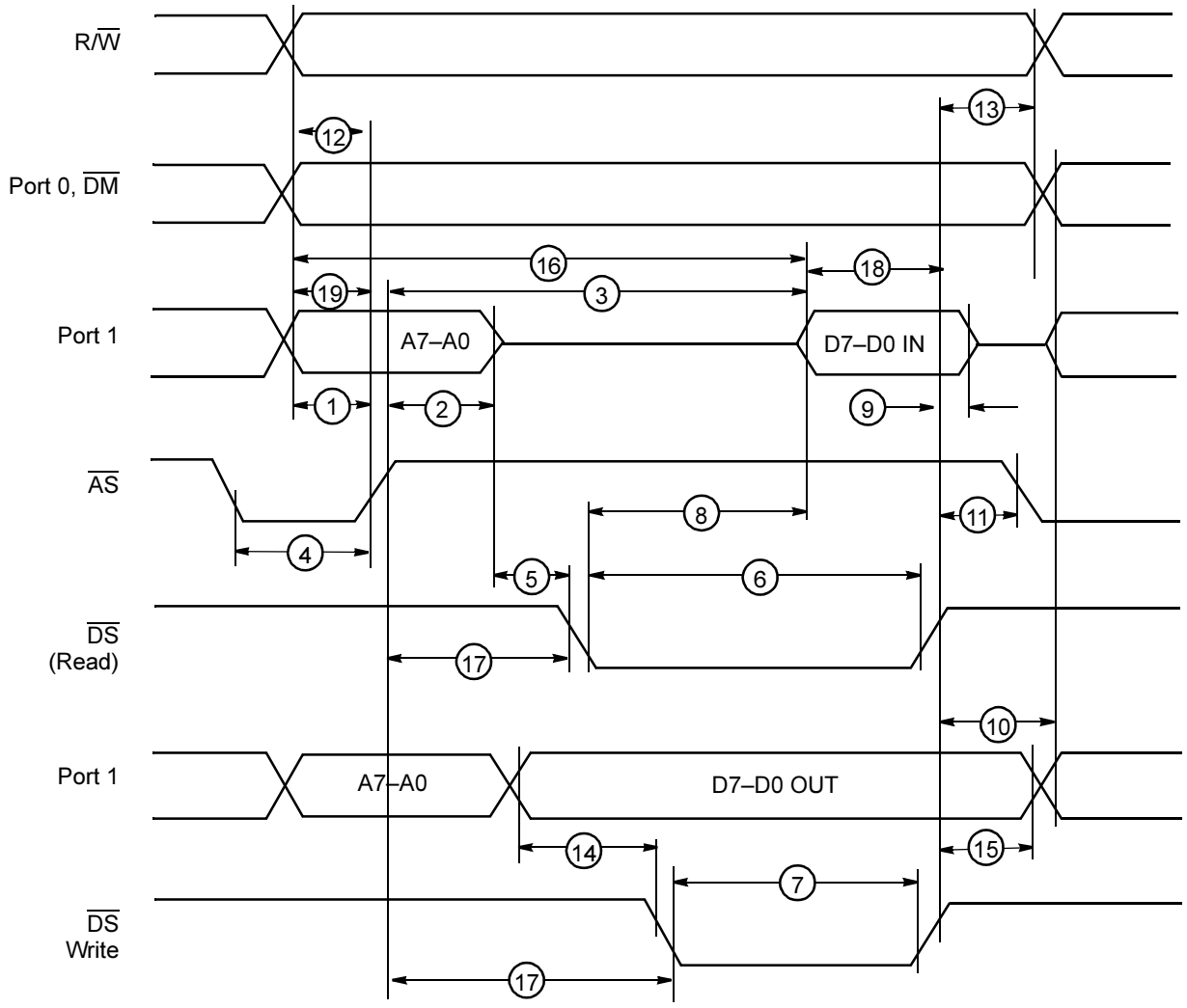
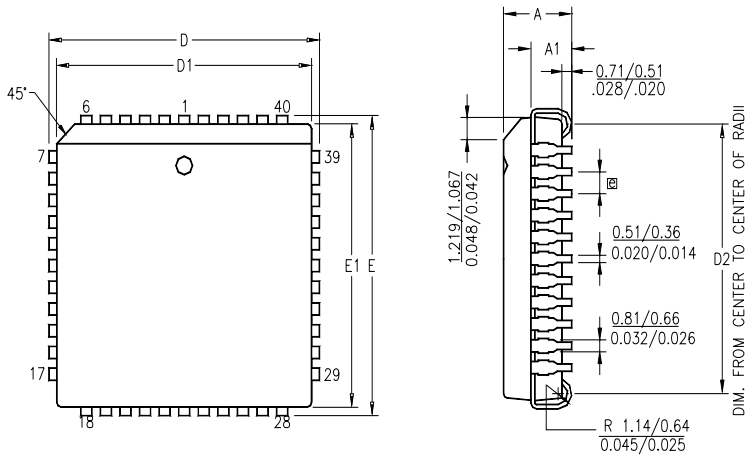


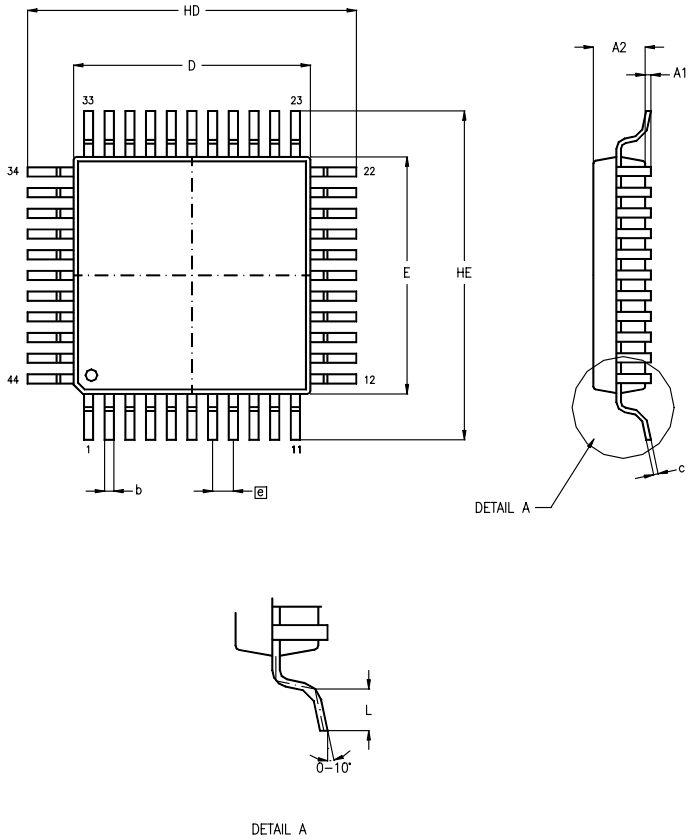
Figure 38. External I/O or Memory READ and WRITE Timing



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
   INCH

Figure 43. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 44. 44-Pin PQFP Package Diagram

Ordering Information

Table 22. Ordering Information

Pin Count	Package	Order Number
40	DIP	Z86C9116PSC
40	DIP	Z86C9116PEC
44	PLCC	Z86C9116VSC
44	PLCC	Z86C9116VEC
44	QFP	Z86C9116FEC
44	QFP	Z86C9116FSC

Part Number Description

ZiLOG part numbers consist of a number of components. For example, part number Z86C9116PSC is a 16-MHz 40-pin DIP that operates in the –0ºC to +70ºC temperature range, with Plastic Standard Flow. The Z86C9116PSC part number corresponds to the code segments indicated in the following table.

Z	ZiLOG Prefix
86	Z8 Product
C	OTP Product
91	Product Number
16	Speed (MHz)
P	Package
S	Temperature
C	Environmental Flow

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

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PS	Product Specification
0185	Unique Document Number
01	Revision Number
0802	Month and Year Published