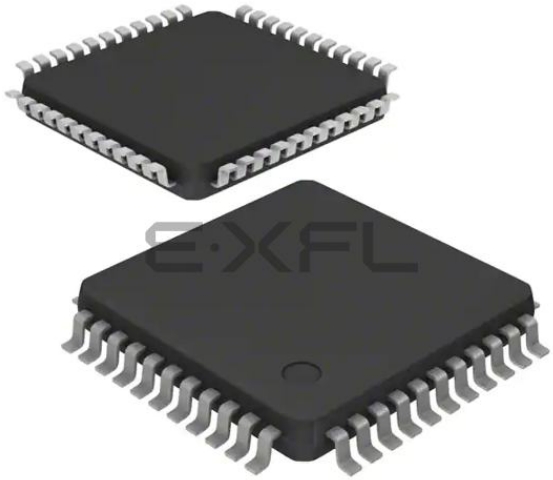

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | UART/USART |
| Peripherals | - |
| Number of I/O | 24 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 236 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86c9116asg |

# Table of Contents

- Six Vectored, Prioritized Interrupts from Eight Different Sources
- Two Programmable 8-Bit Counter/Timers, each with two 6-Bit Programmable Prescalers
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock
- Two Standby Modes: STOP and HALT
- Auto Latches

# Pin Description

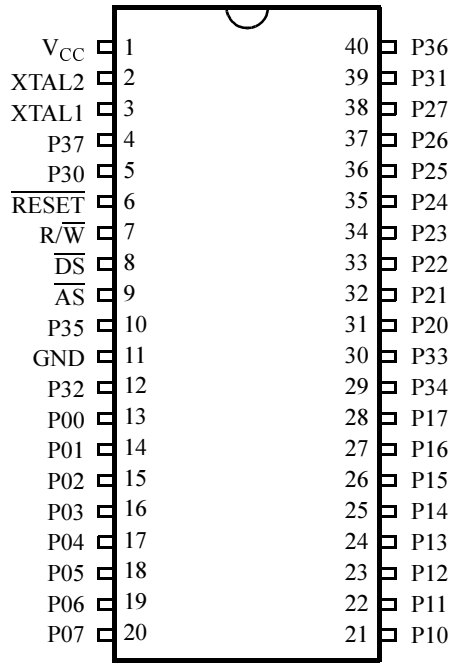



**Figure 2. 40-Pin DIP Pin Configuration**

**Table 12. 40-Pin DIP Pin Identification**

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1 | $V_{CC}$ | Power Supply | Input |
| 2 | XTAL2 | Crystal, Oscillator Clock | Output |
| 3 | XTAL1 | Crystal, Oscillator Clock | Input |
| 4 | P37 | Port 3, Pin 7 | Output |
| 5 | P30 | Port 3, Pin 0 | Input |
| 6 | $\overline{RESET}$ | Reset | Input |
| 7 | R/$\overline{W}$ | Read/Write | Output |
| 8 | $\overline{DS}$ | Data Strobe | Output |
| 9 | $\overline{AS}$ | Address Strobe | Output |
| 10 | P35 | Port 3, Pin 5 | Output |

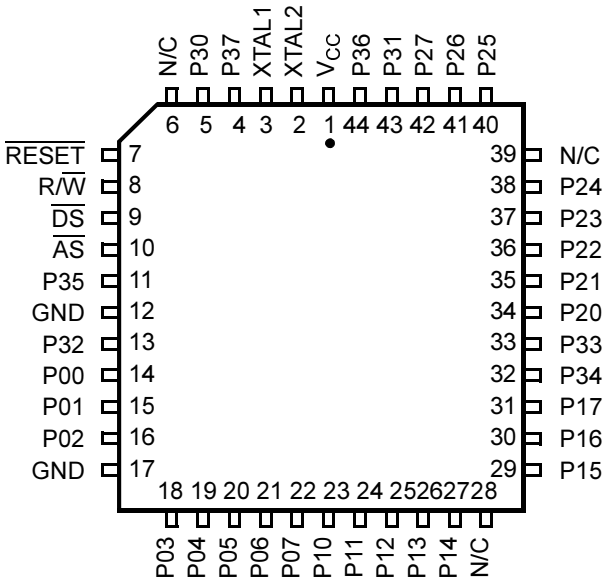



**Figure 4. 44-Pin PLCC Configuration**

**Table 14. 44-Pin PLCC Configuration**

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1 | $V_{CC}$ | Power Supply | Input |
| 2 | XTAL2 | Crystal, Oscillator Clock | Output |
| 3 | XTAL1 | Crystal, Oscillator Clock | Input |
| 4 | P37 | Port 3, Pin 7 | Output |
| 5 | P30 | Port 3, Pin 0 | Input |
| 6 | N/C | Not Connected | |
| 7 | $\overline{RESET}$ | Reset | Input |
| 8 | R/$\overline{W}$ | Read/Write | Output |
| 9 | $\overline{DS}$ | Data Strobe | Output |
| 10 | $\overline{AS}$ | Address Strobe | Output |
| 11 | P35 | Port 3, Pin 5 | Output |
| 12 | GND | Ground $V_{SS}$ | Output |

**Port 1 (P17–P10).** Port 1 is an 8-bit, TTL- compatible port (Figure 6), with multiplexed Address (A7–A0) and Data (D7–D0) ports for interfacing external memory. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 6). A hardware RESET is required to exit this high-impedance state.

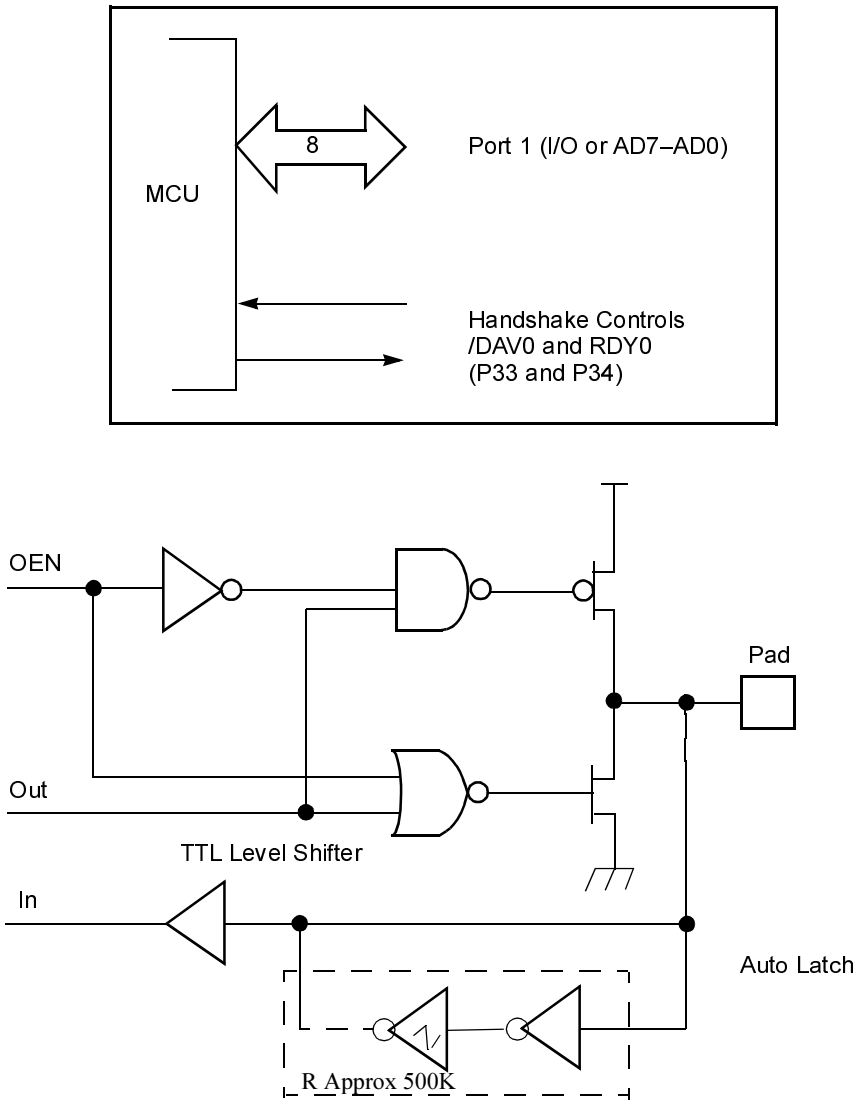



**Figure 6. Port 1 Configuration**

**Table 15. Port 3 Pin Assignments**

| Pin | I/O | Control Timer | Interrupt | P0 HS | P2 HS | Ext | UART |
|---|---|---|---|---|---|---|---|
| P30 | IN | | IRQ3 | | | | Serial In |
| P31 | IN | $T_{IN}$ | IRQ2 | | D/R | | |
| P32 | IN | | IRQ0 | D/R | | | |
| P33 | IN | | IRQ1 | | | | |
| P34 | OUT | | | | | $\overline{DM}$ | |
| P35 | OUT | | | R/D | | | |
| P36 | OUT | $T_{OUT}$ | | | R/D | | |
| P37 | OUT | | | | | | Serial Out |

Notes:
HS = Handshake Signals
D = $\overline{DAV}$ (Data Available)
R = RDY (Ready)

**Autolatch.** The autolatch places valid CMOS levels on all inputs that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Autolatches are available on Port 0, Port 1, Port 2, and P3 inputs.

**$\overline{RESET}$ (input, Low).** Initializes the MCU. RESET occurs through external reset only. During Power-On Reset, the externally-generated reset drives the $\overline{RESET}$ pin Low for the POR time. Pull-up is provided internally.

**Caution:** $\overline{RESET}$ depends on oscillator operation to achieve full reset conditions.

$\overline{RESET}$ is a Schmitt-triggered input. During the RESET cycle, $\overline{DS}$ is held active Low while $\overline{AS}$ cycles at a rate of $T_PC \div 2$. Program execution begins at location `000Ch`, after the $\overline{RESET}$ is released.

When program execution begins, $\overline{AS}$ and $\overline{DS}$ toggles only for external memory accesses. The Z8 can only exit Stop Mode by using the $\overline{RESET}$ pin.The Z8 does reset all registers on a Stop-Mode Recovery operation out of STOP mode.

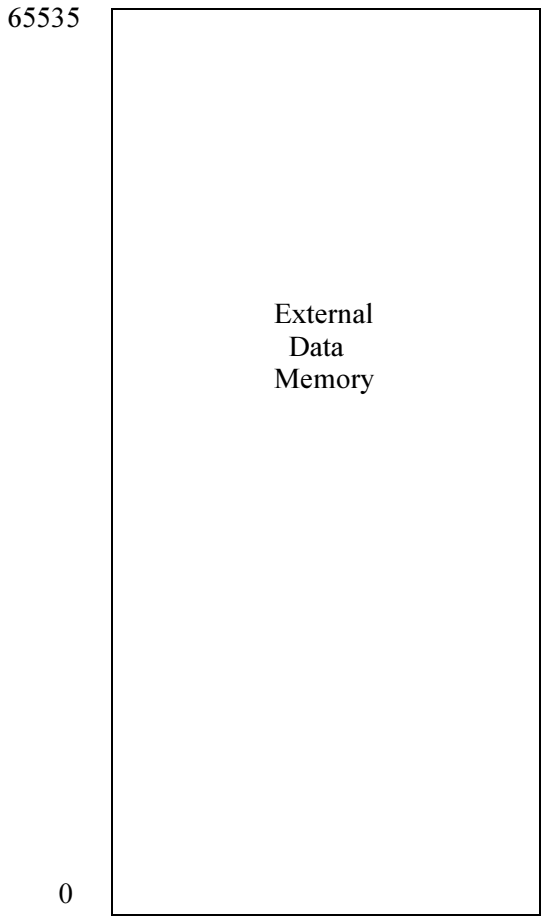



**Figure 14. Data Memory Map**

**Register File.** The register file contains three I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

| Location | | Identifiers |
|---|---|---|
| 255 | Stack Pointer (Bits 7-0) | SPL |
| 254 | Stack Pointer (Bits 15-8) | SPH |
| 253 | Register Pointer | RP |
| 252 | Program Control Flags | FLAGS |
| 251 | Interrupt Mask Register | IMR |
| 250 | Interrupt Request Register | IRQ |
| 249 | Interrupt Priority Register | IPR |
| 248 | Ports 0-1 Mode | P01M |
| 247 | Port 3 Mode | P3M |
| 246 | Port 2 Mode | P2M |
| 245 | T0 Prescaler | PRE0 |
| 244 | Timer/Counter 0 | T0 |
| 243 | T1 Prescaler | PRE1 |
| 242 | Timer/Counter 1 | T1 |
| 241 | Timer Mode | TMR |
| 240 | Serial I/O | SIO |
| 239 | General Purpose Registers | |
| 4 | | |
| 3 | Port 3 | P3 |
| 2 | Port 2 | P2 |
| 1 | Reserved | Reserved |
| 0 | Port 0 | P0 |

**Figure 15. Register File**

**Note:** Register Bank E0-EF is only accessed through working register and indirect addressing modes.

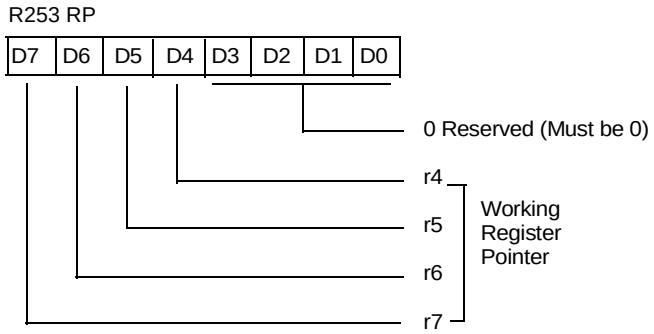



**Figure 16. Register Pointer Register**

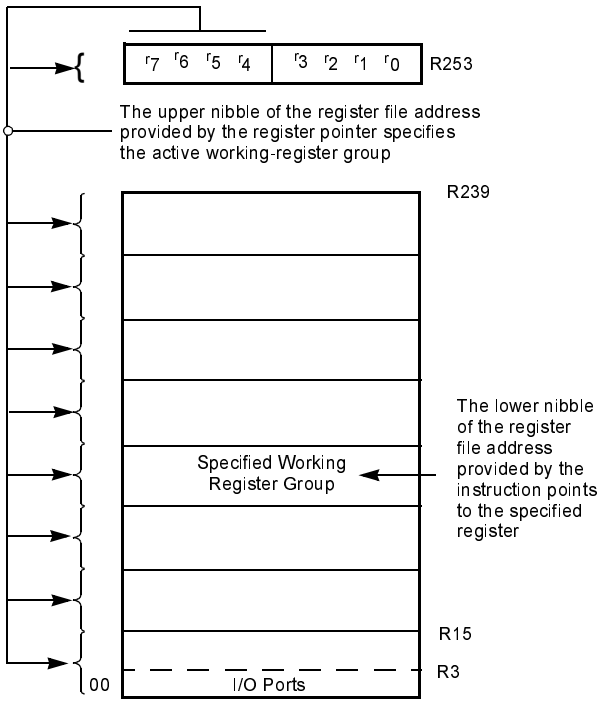



**Figure 17. Register Pointer—Detail**

### Timer Mode Register

The Timer Mode Register, TMR, controls timing and counter functions and shown.in Figure 22.

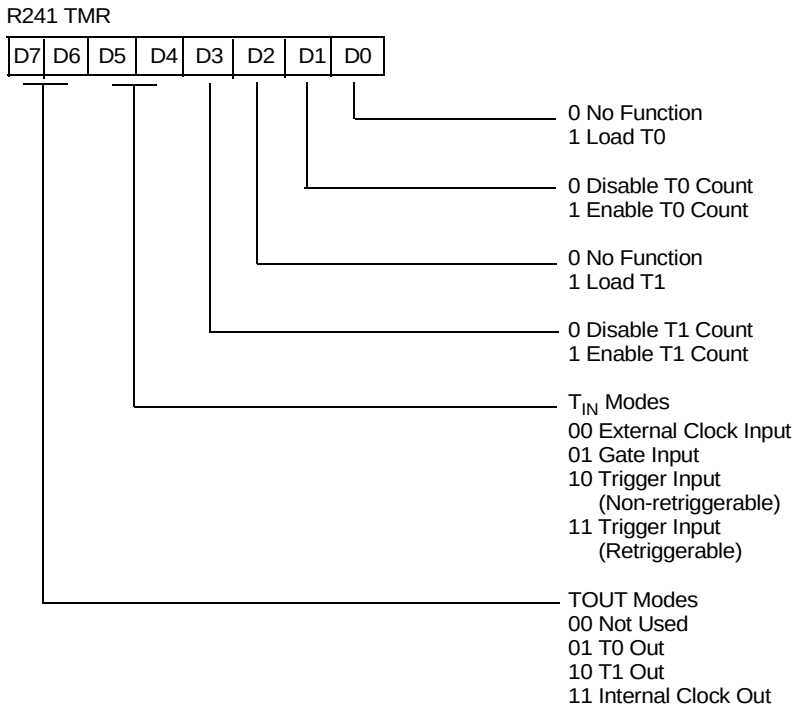



**Figure 22. Timer Mode Register (F1h: Read/Write)**

### Counter/Timer 1 Register

The Counter/Timer 1 Register, T1 is shown in Figure 23.

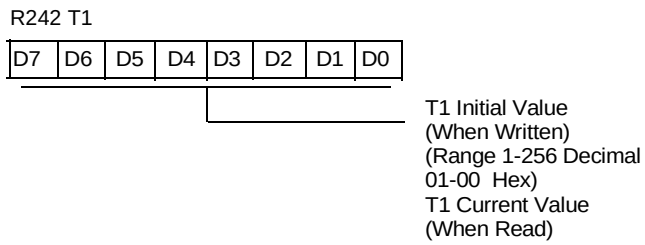



**Figure 23. Counter Timer 1 Register (F2h: Read/Write)**

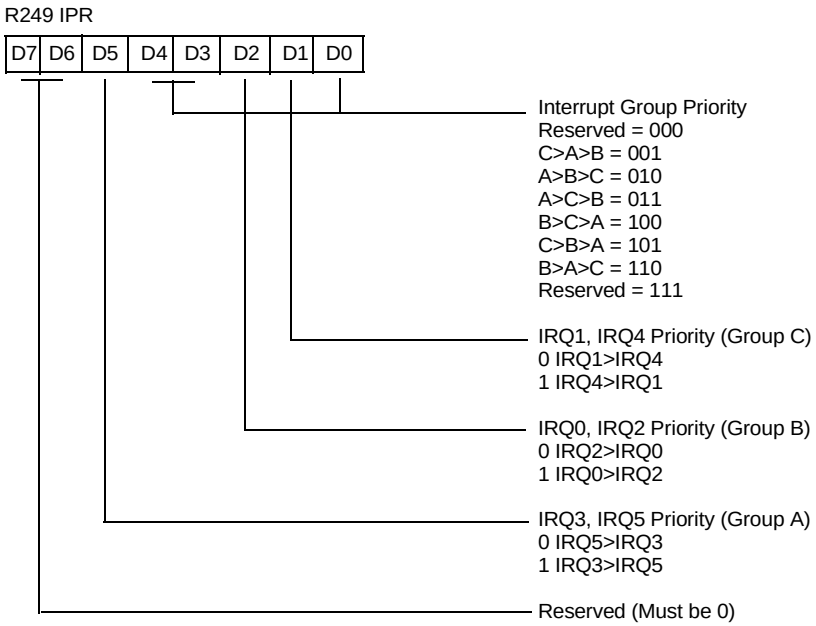



**Figure 30. Interrupt Priority Register (F9h: Write Only)**

### Interrupt Request Register

The Interrupt Request Register, IRQ, controls interrupt functions and is shown in Figure 31.

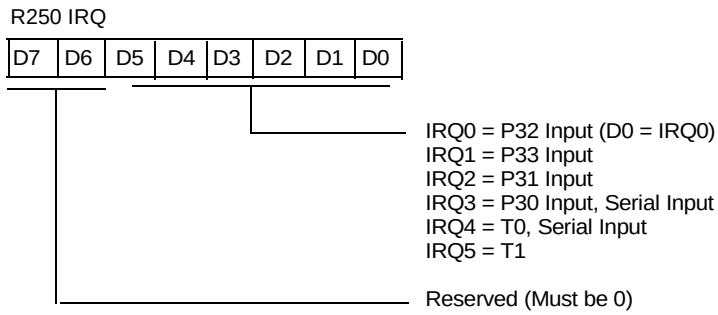



**Figure 31. Interrupt Request Register (FAh: Read/Write)**

### Interrupt Mask Register

The Interrupt Mask Register, IMR, controls interrupt functions and is shown in Figure 32.

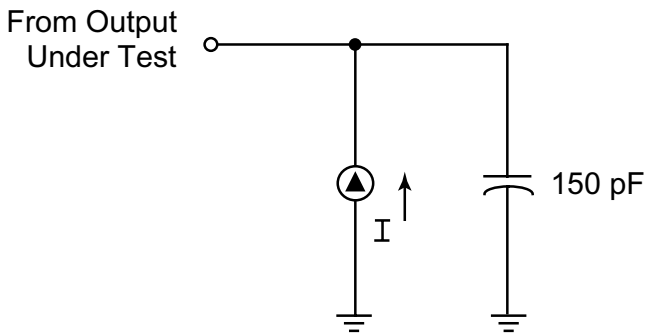



**Figure 37. Test Load Diagram**

## Capacitance

$T_A$ = 25°C, $V_{CC}$ = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

| Parameter | Min | Max |
|---|---|---|
| Input capacitance | 0 | 12 pF |
| Output capacitance | 0 | 12 pF |
| I/O capacitance | 0 | 12 pF |

## DC Electrical Characteristics

**Table 17. DC Electrical Characteristics at Standard and External Temperatures**

| | | $T_A$ = 0°C to +70°C | | $T_A$ = -40°C to +105°C | | Typical[2] | | |
|---|---|---|---|---|---|---|---|---|
| **Sym** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **@25°C** | **Units** | **Conditions** |
| | Max Input Voltage | | 7 | | 7 | | V | $I_{IH}$ <200µA |
| $V_{CH}$ | Clock Input High Voltage | 3.8 | $V_{CC}$ | 3.8 | $V_{CC}$ | | V | Driven by External Clock Generator |

Note:
1. All inputs driven to 0V, $V_{CC}$ and outputs floating.
2. $V_{CC}$ = 5.0V

**Table 17. DC Electrical Characteristics at Standard and External Temperatures (Continued)**

| | | $T_A$ = 0°C to +70°C | | $T_A$ = -40°C to +105°C | | Typical[2] | | |
|---|---|---|---|---|---|---|---|---|
| **Sym** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **@25°C** | **Units** | **Conditions** |
| $V_{CL}$ | Clock Input Low Voltage | -0.3 | 0.8 | -0.3 | 0.8 | | V | Driven by External Clock Generator |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | | V | |
| $V_{IL}$ | Input Low Voltage | –0.3 | 0.8 | -0.3 | 0.8 | | V | |
| $V_{OH}$ | Output High Voltage | 2.4 | | 2.4 | | | V | $I_{OH}$ = -2.0 mA |
| $V_{OH}$ | Output High Voltage | $V_{CC}$–100mV | | $V_{CC}$–100mV | | | V | $I_{OH}$ = -100 µA |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | 0.4 | | V | $I_{OH}$ = +2 mA |
| $V_{RH}$ | Reset Input High Voltage | 3.8 | $V_{CC}$ | 3.8 | $V_{CC}$ | | V | |
| $V_{RL}$ | Reset Input Low Voltage | –0.3 | 0.8 | -0.3 | 0.8 | | V | |
| $I_{IL}$ | Input Leakage | –2 | 2 | -2 | 2 | | µA | Test at 0 V, $V_{CC}$ |
| $I_{OL}$ | Output Leakage | –2 | 2 | -2 | 2 | | µA | Test at 0 V, $V_{CC}$ |
| $I_{IR}$ | Reset Input Current | | –80 | | -80 | | µA | $V_{RL}$=0V |
| $I_{CC}$ | Supply Current | | 35 | | 35 | 24 | mA | @ 16 MHz([1]) |
| $I_{CC1}$ | Standby Current | | 7 | | 7 | 4.5 | mA | HALT Mode $V_{IN}$ = 0 V, $V_{CC}$ @ 16 MHz |
| $I_{CC2}$ | Standby Current | | 10 | | 10 | 1 | µA | STOP Mode $V_{IN}$ = 0 V, $V_{CC}$ ([1]) |
| $I_{ALL}$ | Autolatch Low Current | -10 | 10 | -14 | 14 | | µA | |

Note:
1. All inputs driven to 0V, $V_{CC}$ and outputs floating.
2. $V_{CC}$ = 5.0V

## AC Electrical Characteristics

Figure 38 illustrates the timing characteristics of the Z86C91MCU with respect to external input/output sources. See Table 18 for descriptions of the numbered timing parameters in the figure.

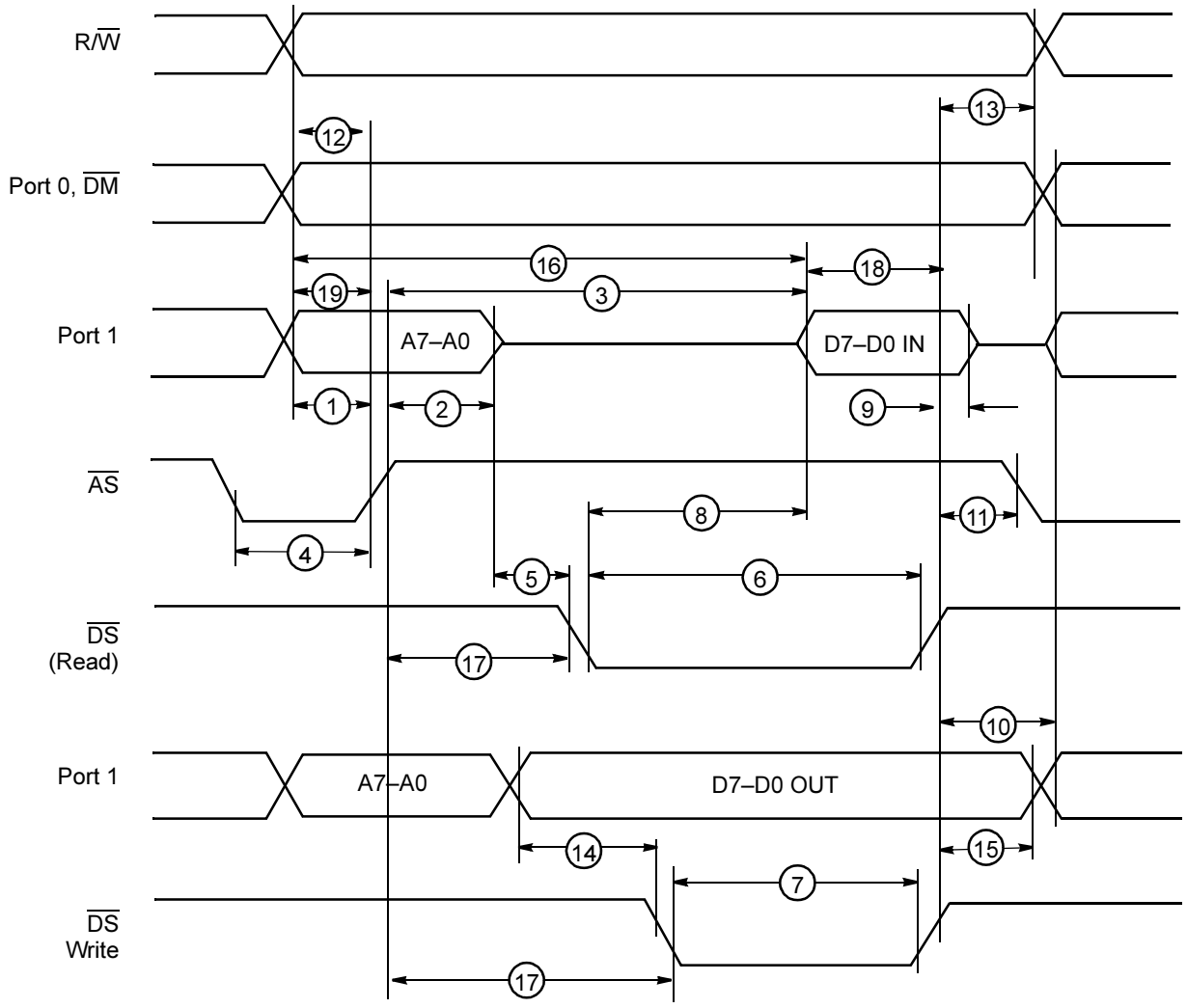



**Figure 38. External I/O or Memory READ and WRITE Timing**

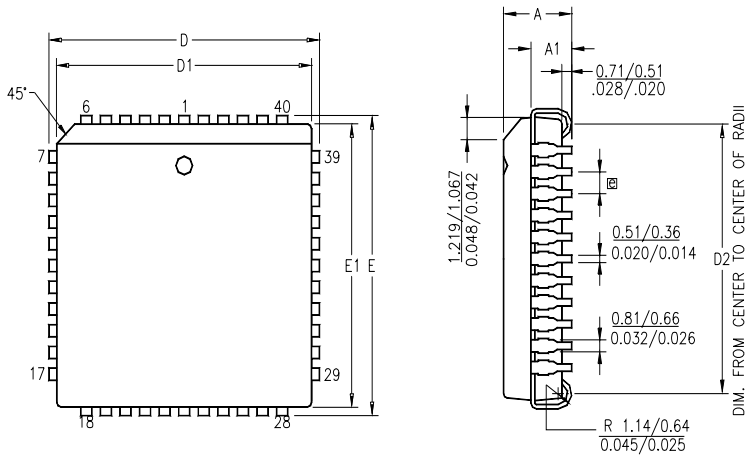
**Table 18. External I/O or Memory READ/WRITE Timing—Standard/Extended Temperature**

| | | | $T_A$ = –0°C to 70°C @ 16 MHz | | $T_A$ = –40°C to 105°C @ 16 MHz | | | |
|---|---|---|---|---|---|---|---|---|
| **No** | **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| 1 | $T_D$A(AS) | Address Valid to $\overline{AS}$ Rise Delay | 25 | | 25 | | ns | 2,3 |
| 2 | $T_D$AS(A) | $\overline{AS}$ Rise to Address Float Delay | 35 | | 35 | | ns | 2,3 |
| 3 | $T_D$AS(DR) | $\overline{AS}$ Rise to Read Data Req'd Valid | | 180 | | 180 | ns | 1,2,3 |
| 4 | $T_W$AS | $\overline{AS}$ Low Width | 40 | | 40 | | ns | 2,3 |
| 5 | $T_D$AS(DS) | Address Float to $\overline{DS}$ Fall | 0 | | 0 | | ns | |
| 6 | $T_W$DSR | $\overline{DS}$ (Read) Low Width | 135 | | 135 | | ns | 1,2,3 |
| 7 | $T_W$DSW | $\overline{DS}$ (WRITE) Low Width | 80 | | 80 | | ns | 1,2,3 |
| 8 | $T_D$DSR(DR) | $\overline{DS}$ Fall to Read Data Req'd Valid | | 75 | | 75 | ns | 1,2,3 |
| 9 | $T_H$DR(DS) | Read Data to $\overline{DS}$ Rise Hold Time | 0 | | 0 | | ns | 2,3 |
| 10 | $T_D$DS(A) | $\overline{DS}$ Rise to Address Active Delay | 50 | | 50 | | ns | 2,3 |
| 11 | $T_D$DS(AS) | $\overline{DS}$ Rise to $\overline{AS}$ Fall Delay | 35 | | 35 | | ns | 2,3 |
| 12 | $T_D$R/W(AS) | R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay | 25 | | 25 | | ns | 2,3 |
| 13 | $T_D$DS(R/W) | $\overline{DS}$ Rise to R/$\overline{W}$ Not Valid | 35 | | 35 | | ns | 2,3 |
| 14 | $T_D$DW(DSW) | WRITE Data Valid to $\overline{DS}$ Fall (WRITE) Delay | 25 | | 25 | | ns | 2,3 |
| 15 | $T_D$DS(DW) | $\overline{DS}$ Rise to WRITE Data Not Valid Delay | 35 | | 35 | | ns | 2,3 |
| 16 | $T_D$A(DR) | Address Valid to Read Data Req'd Valid | | 230 | | 230 | ns | 1,2,3 |
| 17 | $T_D$AS(DS) | $\overline{AS}$ Rise to $\overline{DS}$ Fall Delay | 45 | | 45 | | ns | 2,3 |
| 18 | $T_D$DI(DS) | Data Input Setup to $\overline{DS}$ Rise | 60 | | 60 | | ns | 1,2,3 |
| 19 | $T_D$DM(AS) | $\overline{DM}$ Valid to $\overline{AS}$ Rise Delay | 30 | | 30 | | ns | 2,3 |

Notes:
1. When using extended memory timing add 2 TpC.
2. Timing numbers provided are for minimum $T_P$C.
3. See Clock Cycle Dependent Characteristics table

**Table 19. Clock Dependent Formulas**

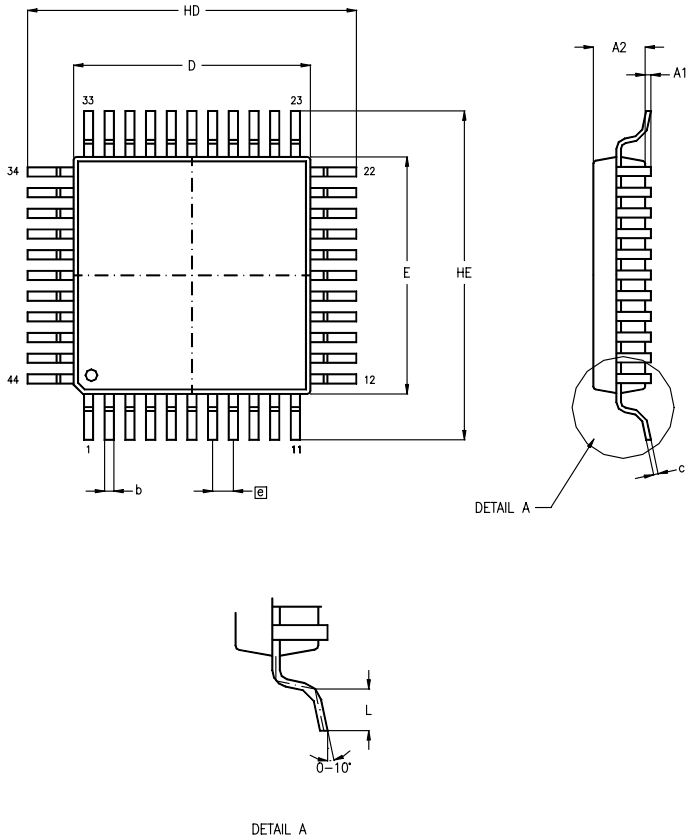
| Number | Symbol | Equation |
|---|---|---|
| 1 | $T_D$A(AS) | 0.40 TpC + 0.32 |
| 2 | $T_D$AS(A) | 0.59 TpC - 3.25 |
| 3 | $T_D$AS(DR) | 2.38 TpC + 6.14 |
| 4 | $T_W$AS | 0.66 TpC -1.65 |
| 6 | $T_W$DSR | 2.33TpC - 10.56 |
| 7 | $T_W$DSW | 1.27 TpC + 1.67 |
| 8 | $T_D$DSR(DR) | 1.97 TpC - 42.5 |
| 10 | $T_D$DS(A) | 0.8 TpC |
| 11 | $T_D$DS(AS) | 0.59 TpC - 3.14 |
| 12 | $T_D$R$\overline{W}$(AS) | 0.4 TpC |
| 13 | $T_D$DS(R$\overline{W}$) | 0.8 TpC - 15 |
| 14 | $T_D$DW(DSW) | 0.4 TpC |
| 15 | $T_D$DS(DW) | 0.88 TpC - 19 |
| 16 | $T_D$A(DR) | 4 TpC - 20 |
| 17 | $T_D$AS(DS) | 0.91 TpC - 10.7 |
| 18 | $T_S$DI(DS) | 0.8 TpC - 10 |
| 19 | $T_D$DM(AS) | 0.9 TpC - 26.3 |




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.27 | 4.57 | 0.168 | 0.180 |
| A1 | 2.41 | 2.92 | 0.095 | 0.115 |
| D/E | 17.40 | 17.65 | 0.685 | 0.695 |
| D1/E1 | 16.51 | 16.66 | 0.650 | 0.656 |
| D2 | 15.24 | 16.00 | 0.600 | 0.630 |
| e | 1.27 BSC | | 0.050 BSC | |

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
   INCH

**Figure 43. 44-Pin PLCC Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.05 | 0.25 | .002 | .010 |
| A2 | 2.00 | 2.25 | .078 | .089 |
| b | 0.25 | 0.45 | .010 | .018 |
| c | 0.13 | 0.20 | .005 | .008 |
| HD | 13.70 | 14.15 | .539 | .557 |
| D | 9.90 | 10.10 | .390 | .398 |
| HE | 13.70 | 14.15 | .539 | .557 |
| E | 9.90 | 10.10 | .390 | .398 |
| e | 0.80 BSC | | .0315 BSC | |
| L | 0.60 | 1.20 | .024 | .047 |

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

**Figure 44. 44-Pin PQFP Package Diagram**

# Ordering Information

**Table 22. Ordering Information**

| Pin Count | Package | Order Number |
|---|---|---|
| 40 | DIP | Z86C9116PSC |
| 40 | DIP | Z86C9116PEC |
| 44 | PLCC | Z86C9116VSC |
| 44 | PLCC | Z86C9116VEC |
| 44 | QFP | Z86C9116FEC |
| 44 | QFP | Z86C9116FSC |

## Part Number Description

ZiLOG part numbers consist of a number of components. For example, part number Z86C9116PSC is a 16-MHz 40-pin DIP that operates in the –0ºC to +70ºC temperature range, with Plastic Standard Flow. The Z86C9116PSC part number corresponds to the code segments indicated in the following table.

| | |
|---|---|
| Z | ZiLOG Prefix |
| 86 | Z8 Product |
| C | OTP Product |
| 91 | Product Number |
| 16 | Speed (MHz) |
| P | Package |
| S | Temperature |
| C | Environmental Flow |

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

ZiLOG, Inc.
532 Race Street
San Jose, CA 95126-3432
Telephone (408) 558-8500
FAX 408 558-8300
Internet: www.ZiLOG.com