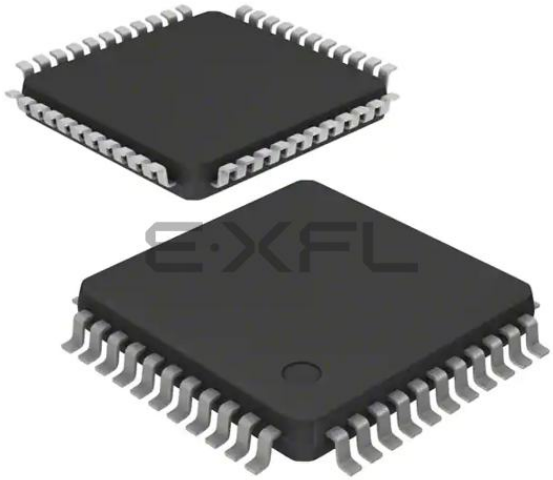

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
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- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock
- Two Standby Modes: STOP and HALT
- Auto Latches

Functional Block Diagrams

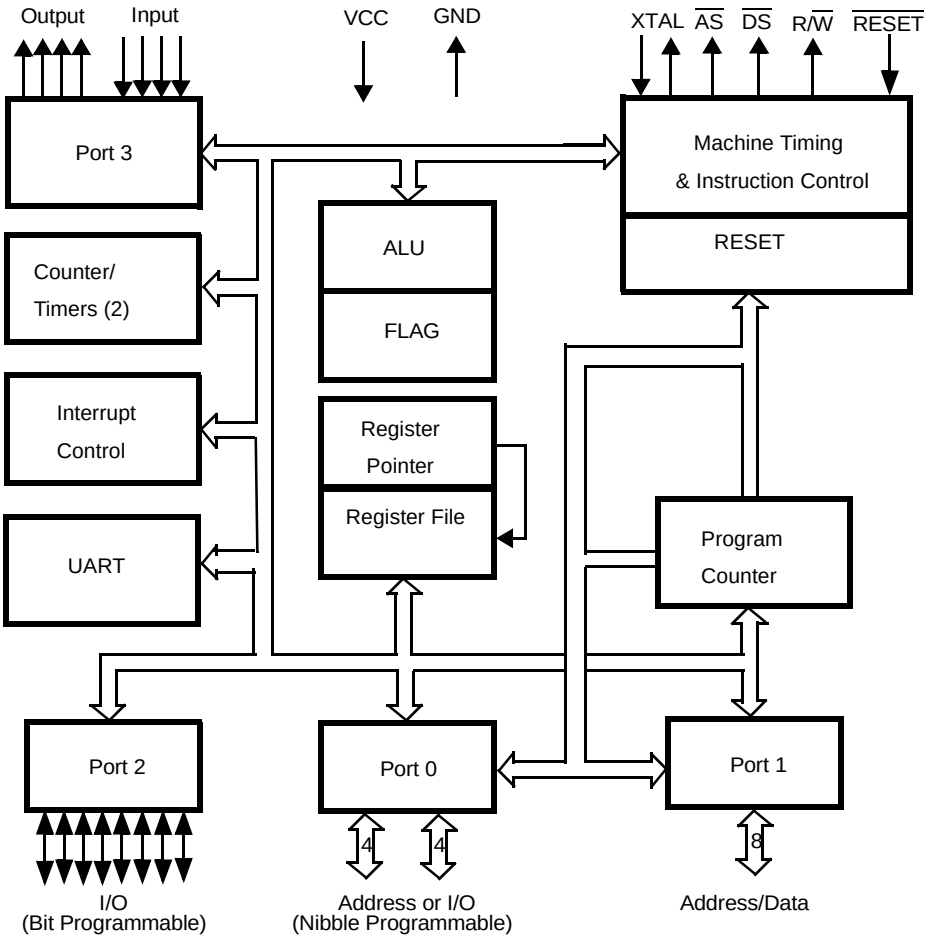


Figure 1. Z86C91 Functional Block Diagram

Table 13. 44-Pin PQFP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3, Bit 7	Output
33	P30	Port 3, Bit 0	Intput
34	$\overline{\text{RESET}}$	Reset	Input
35	R/$\overline{\text{W}}$	Read/Write	Output
36	$\overline{\text{DS}}$	Data Strobe	Output
37	$\overline{\text{AS}}$	Address Strobe	Output
38	P35	Port 3, Bit 5	Output
39	GND	Ground	Output
40	P32	Port 3, Bit 2	Input
41-43	P00-P02	Port 0, Bits 0-2	Input/Output
44	GND	Ground	Output

Pin Functions

The following paragraphs describe the function of each available Z86C91 pin.

$\overline{\text{DS}}$ (output, active Low). The Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). The Address Strobe is pulsed one time at the beginning of each machine cycle for external memory transfer. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and READ/WRITE.

XTAL1 (Crystal 1)Time-Based Oscillator Input. This pin connects a parallel-resonant crystal, ceramic resonator, LC network, or an external single-phase clock to the on-chip oscillatorand buffer.

XTAL2 (Crystal 2) Time-Based Oscillator Output. This pin connects a parallel-resonant crystal, ceramic resonant, LC network to the on-chip oscillator and buffer.

R/$\overline{\text{W}}$ (output, WRITE Low). The READ/WRITE signal is Low when the Z8 writes to external data memory.

$\overline{\text{RESET}}$ (input, Low). To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external XTAL clocks (4TpC). If the external $\overline{\text{RESET}}$ signal is less than 4TpC in duration, reset does not occur.

On the fifth clock after $\overline{\text{RESET}}$ is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external $\overline{\text{RESET}}$, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. When $\overline{\text{RESET}}$ is deactivated, program execution begins at location 000Ch. Power-Up reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P00–P07). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03–P00 input/output and P07–P04 input/output), or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control $\overline{\text{DAV0}}$ and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04–P07. The lower nibble must indicate the same direction as the upper nibble.

For external memory references, Port 1 provides address bits A7–A0 (lower nibble) and Port 0 provides address bits A15–A8 (upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 is programmed independently as I/O while the lower nibble is used for addressing. If one or

both nibbles are required for I/O operation, they are configured by writing to the Port 01 mode register (P01M).

After a hardware RESET, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode.

Port 0 can be placed in a high-impedance state along with Port 1, $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 5). A hardware RESET is required to exit this high-impedance state.

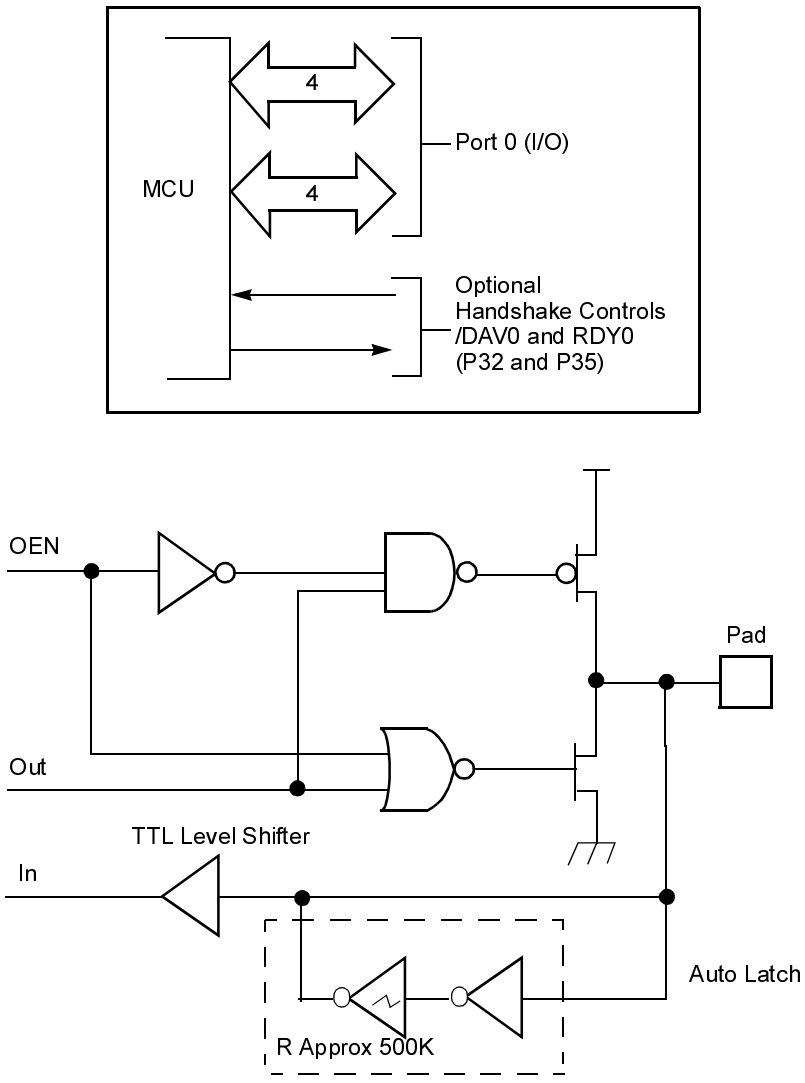


Figure 5. Port 0 Configuration

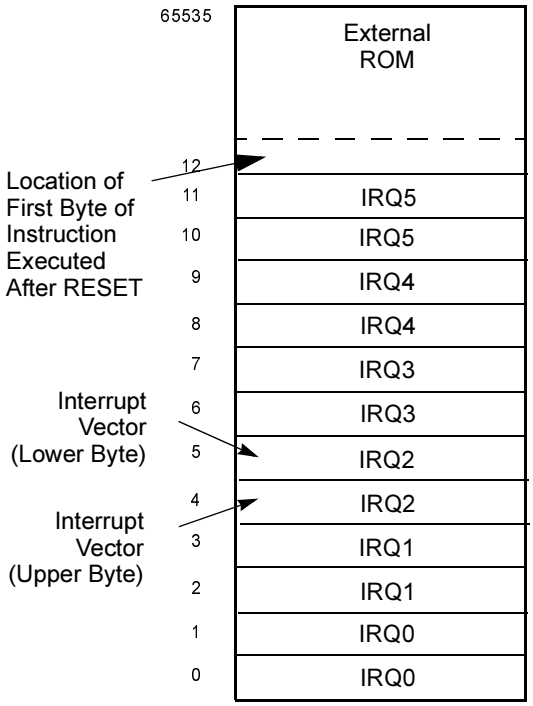


Figure 13. Program Memory Map

Data Memory ($\overline{DM}$). The Z86C91addresses up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that is programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode.

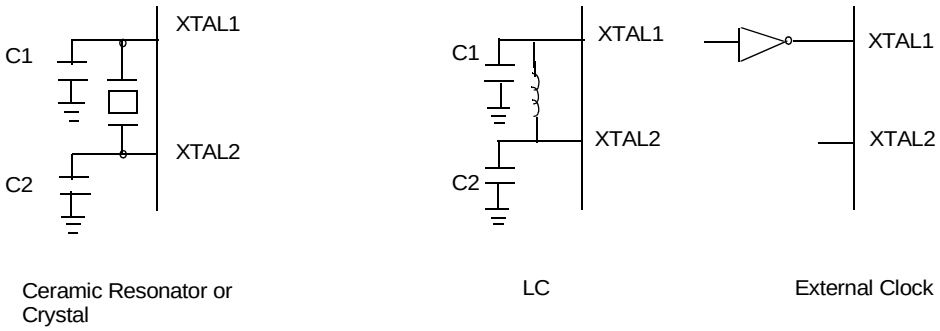


Figure 20. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation or the peripheral clock. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at location `000Ch`.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. Therefore, the user must execute a NOP (Op Code = `FFh`) immediately before the appropriate sleep instruction. For example:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

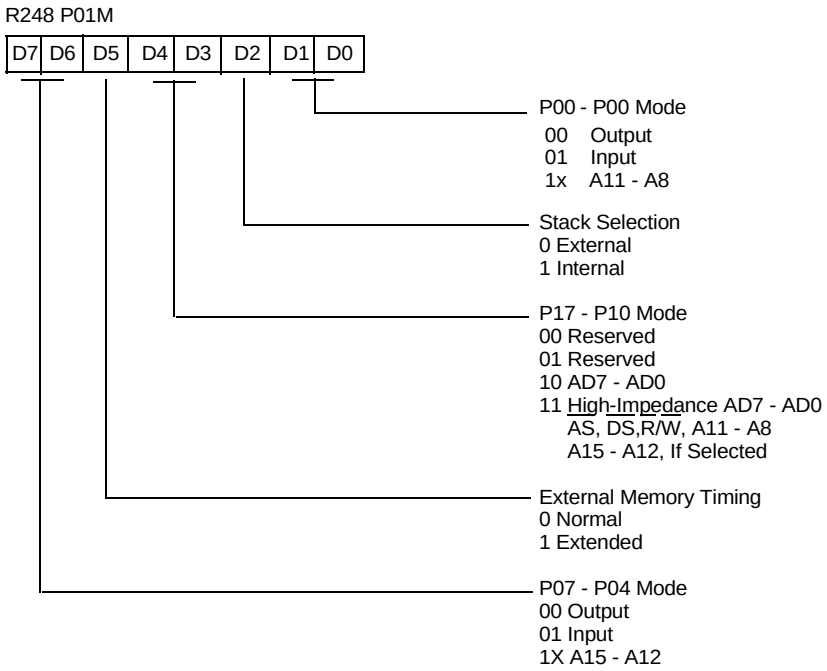


Figure 29. Port 0 and 1 Mode Register (F8h: Write Only)

Interrupt Priority Register. The Interrupt Priority Register, IPR, prioritizes interrupt functions and is shown in Figure 30.

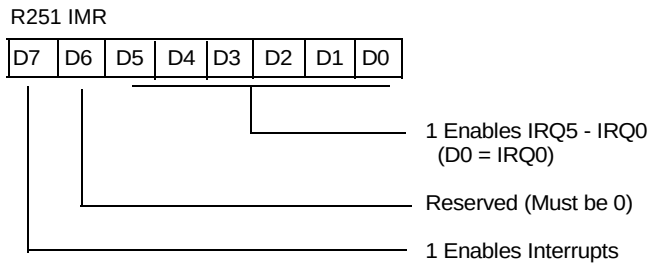


Figure 32. Interrupt Mask Register (FBh: Read/Write)

Flags Register

The CPU sets flags in the Flags Register, FLAGS, to allow the user to perform tests based on differing logical states. The FLAGS Register is shown in Figure 33 .

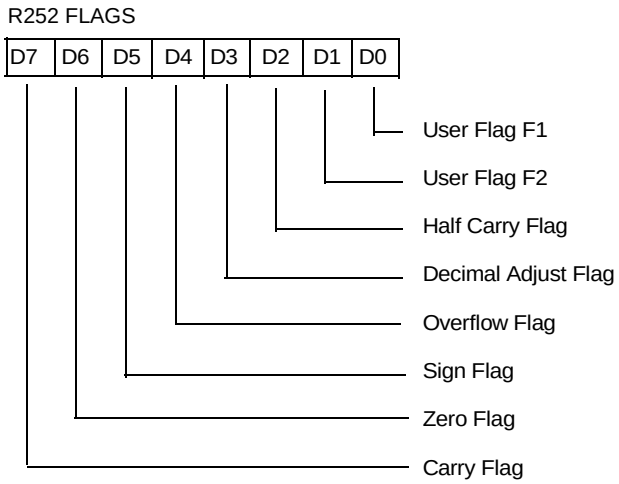


Figure 33. Flags Register (FCh: Read/Write)

Register Pointer Register

The Register Pointer Register, RP, controls pointer functions in the working registers and is shown in Figure 34.

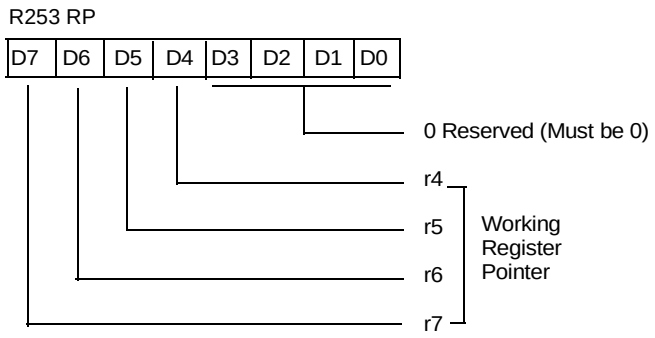


Figure 34. Register Pointer Register (FDh: Read/Write)

Stack Pointer High Register

The Stack Pointer High Register, SPH, controls pointer functions in the upper byte when the external stack is used and is shown in Figure 35.

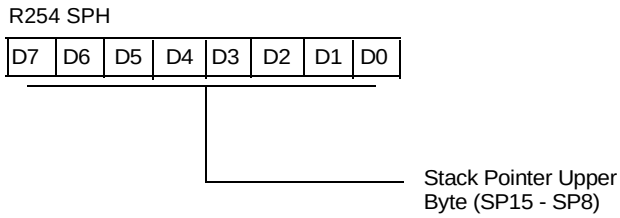


Figure 35. Stack Pointer Register (FEh: Read/Write)

Stack Pointer Low Register

The Stack Pointer Low Register, SPL, controls pointer functions in the lower byte and is shown in Figure 36.

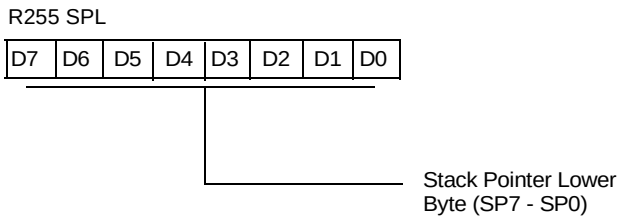


Figure 36. Stack Pointer Register (FFh: Read/Write)

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than the Absolute Maximum Ratings listed in Table 16 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STO}	Storage Temperature	–65	+150	C
T_A	Operating Ambient Temperature		[2]	C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 37).

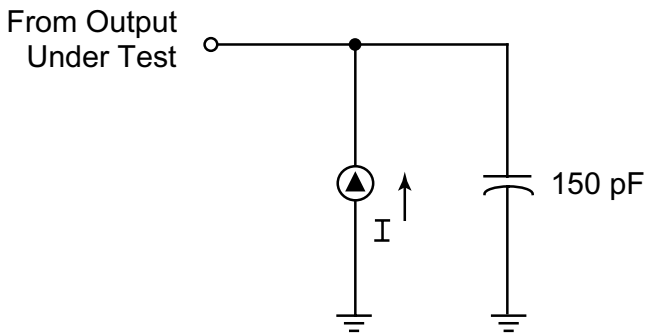


Figure 37. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC Electrical Characteristics

Table 17. DC Electrical Characteristics at Standard and External Temperatures

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical[2]		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@25°C**	**Units**	**Conditions**
	Max Input Voltage		7		7		V	I_{IH} <200µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	Driven by External Clock Generator

Note:
1. All inputs driven to 0V, V_{CC} and outputs floating.
2. V_{CC} = 5.0V

Table 18. External I/O or Memory READ/WRITE Timing—Standard/Extended Temperature

			T_A = –0°C to 70°C @ 16 MHz		T_A = –40°C to 105°C @ 16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	T_DA(AS)	Address Valid to $\overline{AS}$ Rise Delay	25		25		ns	2,3
2	T_DAS(A)	$\overline{AS}$ Rise to Address Float Delay	35		35		ns	2,3
3	T_DAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid		180		180	ns	1,2,3
4	T_WAS	$\overline{AS}$ Low Width	40		40		ns	2,3
5	T_DAS(DS)	Address Float to $\overline{DS}$ Fall	0		0		ns	
6	T_WDSR	$\overline{DS}$ (Read) Low Width	135		135		ns	1,2,3
7	T_WDSW	$\overline{DS}$ (WRITE) Low Width	80		80		ns	1,2,3
8	T_DDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid		75		75	ns	1,2,3
9	T_HDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	0		0		ns	2,3
10	T_DDS(A)	$\overline{DS}$ Rise to Address Active Delay	50		50		ns	2,3
11	T_DDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	35		35		ns	2,3
12	T_DR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	25		25		ns	2,3
13	T_DDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	35		35		ns	2,3
14	T_DDW(DSW)	WRITE Data Valid to $\overline{DS}$ Fall (WRITE) Delay	25		25		ns	2,3
15	T_DDS(DW)	$\overline{DS}$ Rise to WRITE Data Not Valid Delay	35		35		ns	2,3
16	T_DA(DR)	Address Valid to Read Data Req'd Valid		230		230	ns	1,2,3
17	T_DAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	45		45		ns	2,3
18	T_DDI(DS)	Data Input Setup to $\overline{DS}$ Rise	60		60		ns	1,2,3
19	T_DDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	30		30		ns	2,3

Notes:
1. When using extended memory timing add 2 TpC.
2. Timing numbers provided are for minimum T_PC.
3. See Clock Cycle Dependent Characteristics table

Table 19. Clock Dependent Formulas

Number	Symbol	Equation
1	T_DA(AS)	0.40 TpC + 0.32
2	T_DAS(A)	0.59 TpC - 3.25
3	T_DAS(DR)	2.38 TpC + 6.14
4	T_WAS	0.66 TpC -1.65
6	T_WDSR	2.33TpC - 10.56
7	T_WDSW	1.27 TpC + 1.67
8	T_DDSR(DR)	1.97 TpC - 42.5
10	T_DDS(A)	0.8 TpC
11	T_DDS(AS)	0.59 TpC - 3.14
12	T_DR$\overline{W}$(AS)	0.4 TpC
13	T_DDS(R$\overline{W}$)	0.8 TpC - 15
14	T_DDW(DSW)	0.4 TpC
15	T_DDS(DW)	0.88 TpC - 19
16	T_DA(DR)	4 TpC - 20
17	T_DAS(DS)	0.91 TpC - 10.7
18	T_SDI(DS)	0.8 TpC - 10
19	T_DDM(AS)	0.9 TpC - 26.3

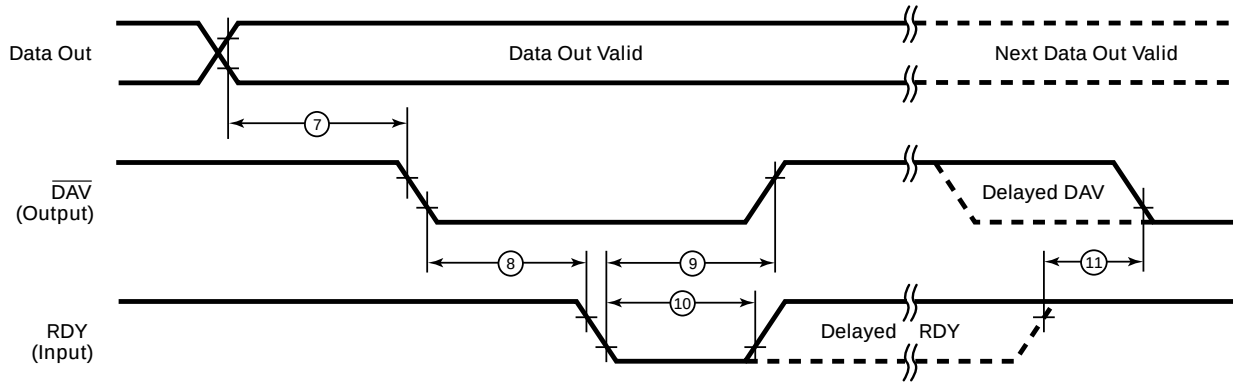


Figure 41. Output Handshake Timing

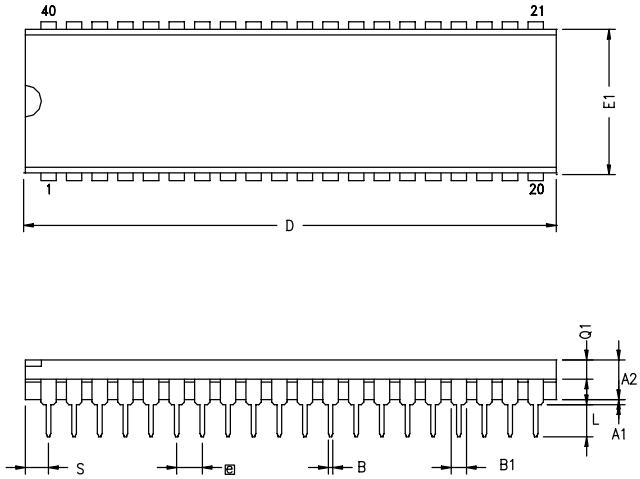
Table 21. Handshake Timing (Standard and Extended Temperatures)

No	Symbol	Parameter	T_A = 0ºC to +70ºC Min	T_A = 0ºC to +70ºC Max	T_A = -40ºC to +105ºC Min	T_A = -40ºC to +105ºC Max	Data Direction
1	T_SDI(DAV)	Data In Setup Time	0		0		Input
2	T_HDI(RDY)	Data In Hold Time	145		145		Input
3	T_WDAV	Data Available Width	110		110		Input
4	T_DDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	Input
5	T_DDAVId(RDY)	DAV Out to DAV Fall Delay		115		115	Input
6	RDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	0		0		Input
7	T_DD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	Output
8	T_DDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		Output
9	T_DRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	Output
10	T_WRDY	RDY Width	110		110		Output
11	T_DRDY0$_D$(DAV)	RDY Rise to DAV Fall Delay		115		115	Output

Note: All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Packaging

Figure 42 illustrates the 40-pin DIP package for the microcontroller devices.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 42. 40-Pin DIP Package Diagram