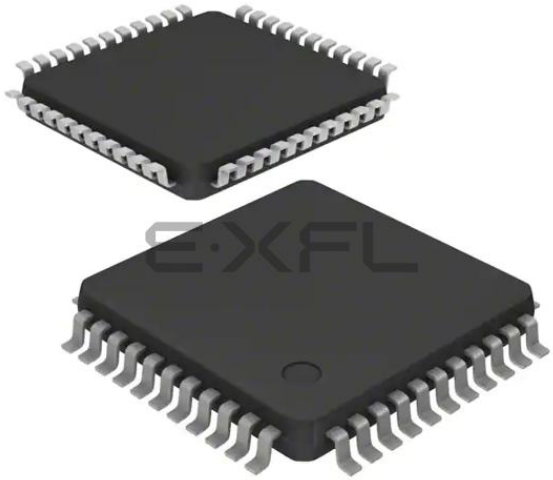

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9116fsc

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
532 Race Street
Campbell, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

Table of Contents

List of Figures

Architectural Overview

ZiLOG's large Z8® family of 8-bit ROMless microcontrollers includes the Z86C91 product with 236 bytes of RAM. Each of these devices offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

For applications demanding powerful I/O capabilities, the Z86C91 offers 24 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines and is configurable under software control to proviide timing, status signals, serial or parallel I/O with or without handshake and an address/data bus for interfacing external memory. The Z86C91 MCU features three basic address spaces to support this wide range of configurations: Program Memory, Data Memory, and 236 General Purposes Registers.

The Z86C91 operates at 16 MHz with a voltage range of 4.5 to 5.5 VDC.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86C91 offers two on-chip counter/timers with a large number of user-selectable modes and a full-duplex hardware UART.

The Z86C91 is a ROMless part and offers the use of external memory, which enables this Z8® MCU to be used in high-volume applications, or where code flexibility is required.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Z86C91 Features

- Asynchronous receiver/transmitter UART
- 40-Pin DIP and 44-Pin PLCC and QFP Packages
- 4.5- to 5.5-Volt Operating Range
- Operating Temperature Ranges:
  - Standard: 0ºC to 70ºC
  - Extended: -40ºC to 105ºC
- 24 Input/Output Lines

Table 13. 44-Pin PQFP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3, Bit 7	Output
33	P30	Port 3, Bit 0	Intput
34	$\overline{\text{RESET}}$	Reset	Input
35	R/$\overline{\text{W}}$	Read/Write	Output
36	$\overline{\text{DS}}$	Data Strobe	Output
37	$\overline{\text{AS}}$	Address Strobe	Output
38	P35	Port 3, Bit 5	Output
39	GND	Ground	Output
40	P32	Port 3, Bit 2	Input
41-43	P00-P02	Port 0, Bits 0-2	Input/Output
44	GND	Ground	Output

Port 1 (P17–P10). Port 1 is an 8-bit, TTL- compatible port (Figure 6), with multiplexed Address (A7–A0) and Data (D7–D0) ports for interfacing external memory. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 6). A hardware RESET is required to exit this high-impedance state.

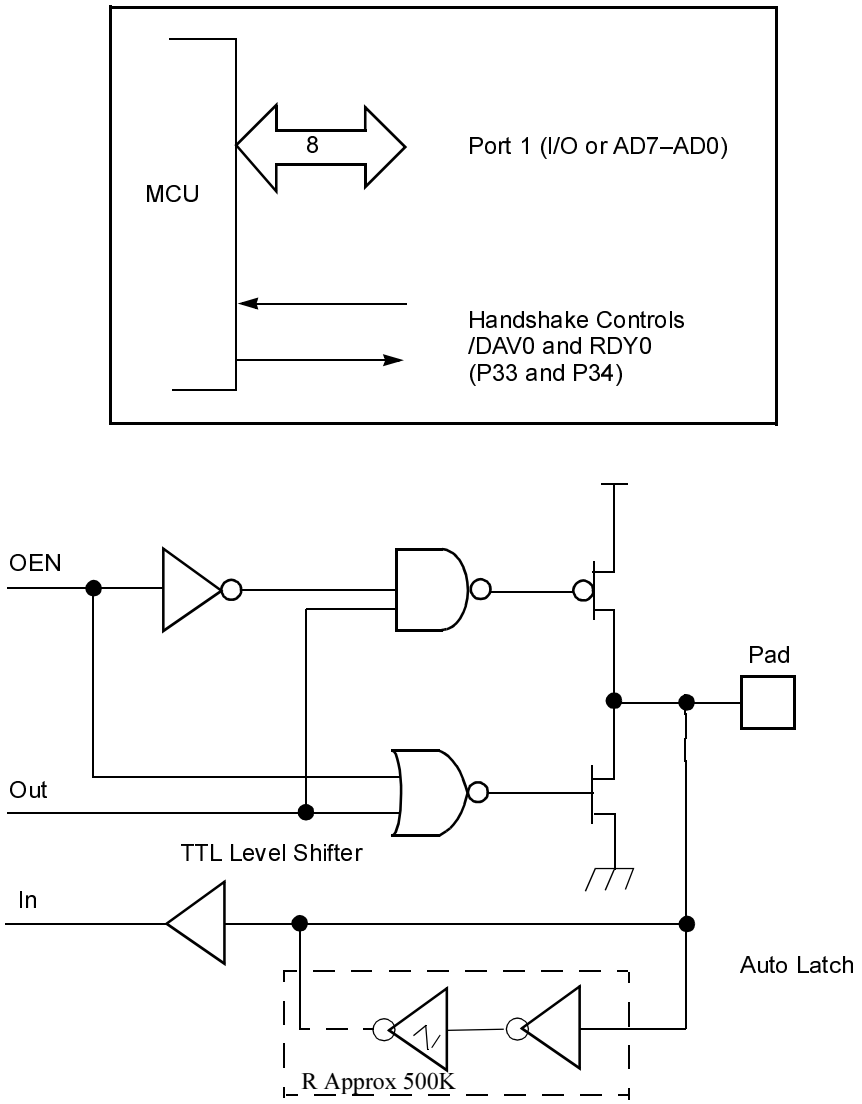

Figure 6. Port 1 Configuration

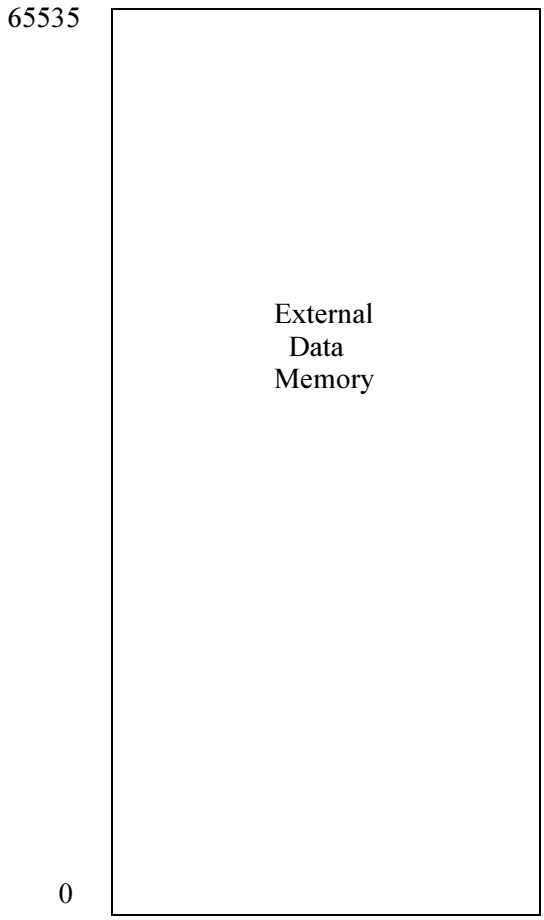

Figure 14. Data Memory Map

Register File. The register file contains three I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

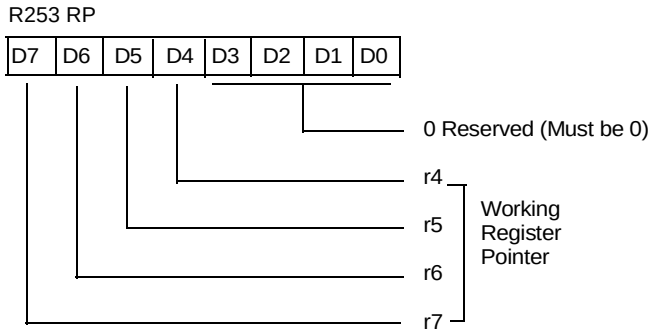

Figure 16. Register Pointer Register

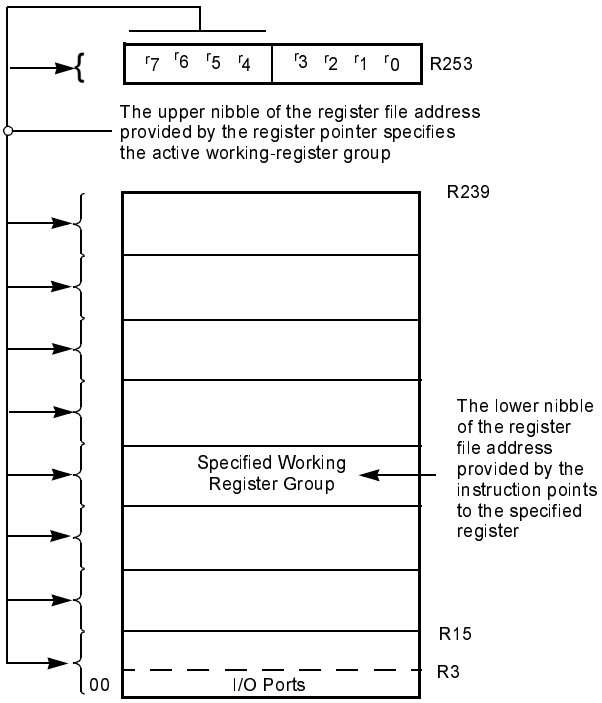

Figure 17. Register Pointer—Detail

Interrupts. The Z8 has six different interrupts from eight different sources. These interrupts are maskable and prioritized. The 8 sources are divided as follows: 4 sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and 2 are claimed by counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register

All interrupts are vectored through locations in Program Memory. When an interrupt request is granted, the interrupt machine cycle is activated. This resets the interrupt request flag and disables all of the subsequent interrupts, except Program Counter and Status Flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16 bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Nested interrupts are supported by enabling interrupts in the interrupt service routine.

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48TpC (external XTAL clock cycles) are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

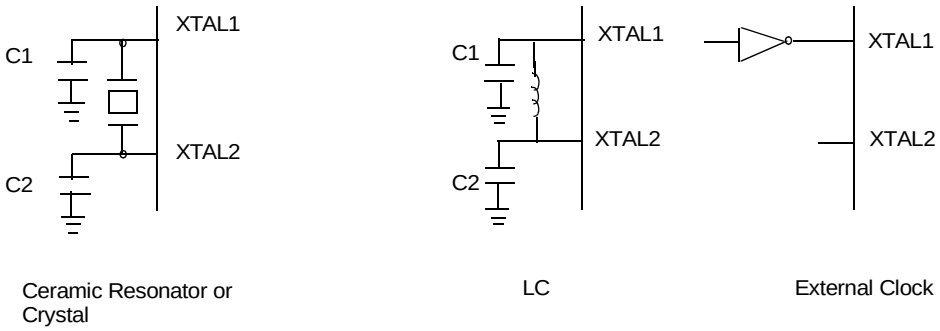

Figure 20. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation or the peripheral clock. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at location `000Ch`.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. Therefore, the user must execute a NOP (Op Code = `FFh`) immediately before the appropriate sleep instruction. For example:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

Control Registers

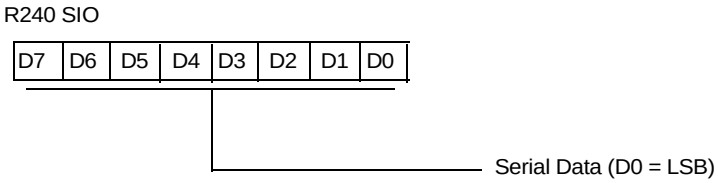

Figure 21. Serial I/O Register (F0h: Read/Write)

Caution: The majority of the control registers are read/write. The rest of the control are write only. The write-only registers are not readable. Attempting to read write-only registers will result in reading non-valid data. Any attempt to use logical or boolean types of instructions on these registers may corrupt the contents in the registers involved. Emulator operations on these write-only registers also reflect what is found on the Z8 device.

Timer Mode Register

The Timer Mode Register, TMR, controls timing and counter functions and shown.in Figure 22.

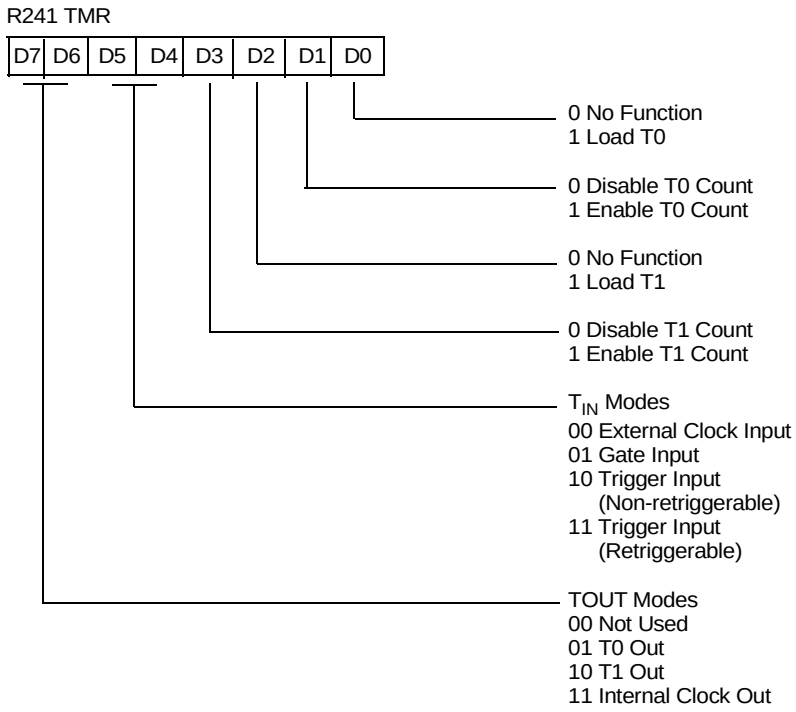

Figure 22. Timer Mode Register (F1h: Read/Write)

Counter/Timer 1 Register

The Counter/Timer 1 Register, T1 is shown in Figure 23.

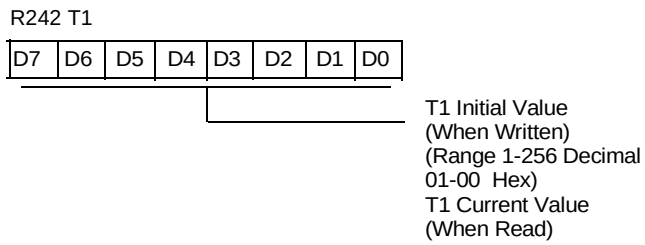

Figure 23. Counter Timer 1 Register (F2h: Read/Write)

Prescaler 1 Register

The Prescaler 1 Register, PRE1, controls clocking functions and is shown in Figure 24.

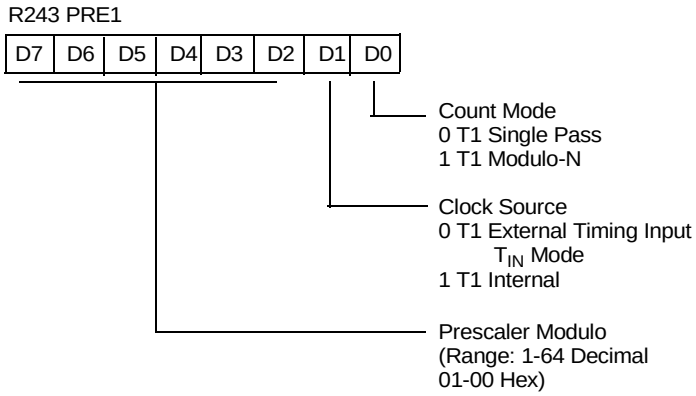

Figure 24. Prescaler 1 Register (F3h: Write Only)

Counter/Timer 0 Register

The Counter/Timer 0 Register, T0 is shown in Figure 25.

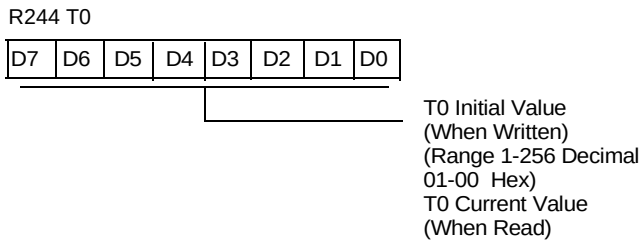

Figure 25. Counter/Timer 0 Register (F4h: Read/Write)

Prescaler 0 Register

The Prescaler 0 Register PRE0 controls clocking functions and is shown in Figure 26.

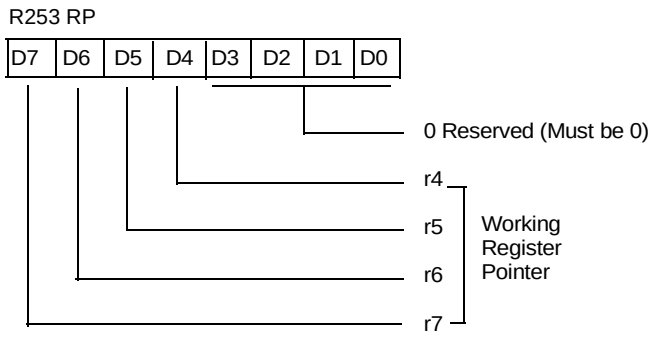

Figure 34. Register Pointer Register (FDh: Read/Write)

Stack Pointer High Register

The Stack Pointer High Register, SPH, controls pointer functions in the upper byte when the external stack is used and is shown in Figure 35.

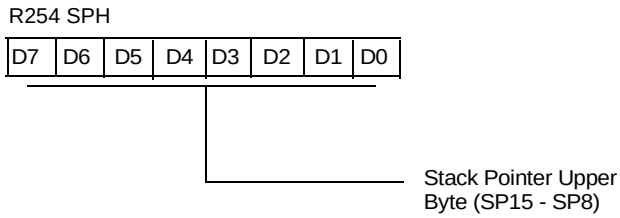

Figure 35. Stack Pointer Register (FEh: Read/Write)

Stack Pointer Low Register

The Stack Pointer Low Register, SPL, controls pointer functions in the lower byte and is shown in Figure 36.

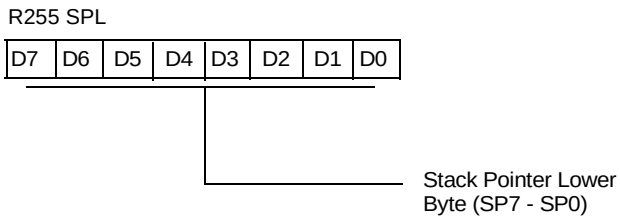

Figure 36. Stack Pointer Register (FFh: Read/Write)

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than the Absolute Maximum Ratings listed in Table 16 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STO}	Storage Temperature	–65	+150	C
T_A	Operating Ambient Temperature		[2]	C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 37).

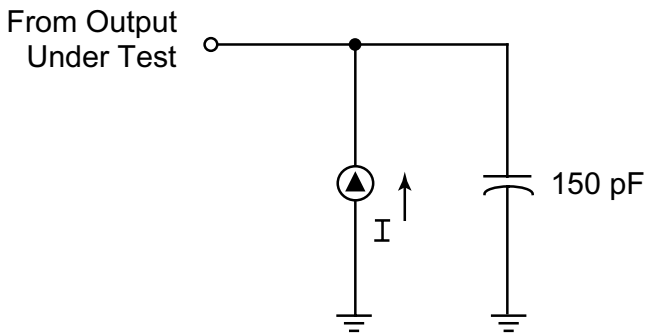

Figure 37. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC Electrical Characteristics

Table 17. DC Electrical Characteristics at Standard and External Temperatures

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical[2]		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@25°C**	**Units**	**Conditions**
	Max Input Voltage		7		7		V	I_{IH} <200µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	Driven by External Clock Generator

Note:
1. All inputs driven to 0V, V_{CC} and outputs floating.
2. V_{CC} = 5.0V

Table 17. DC Electrical Characteristics at Standard and External Temperatures (Continued)

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical[2]		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@25°C**	**Units**	**Conditions**
V_{CL}	Clock Input Low Voltage	-0.3	0.8	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = -2.0 mA
V_{OH}	Output High Voltage	V_{CC}–100mV		V_{CC}–100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OH} = +2 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8	-0.3	0.8		V	
I_{IL}	Input Leakage	–2	2	-2	2		µA	Test at 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	-2	2		µA	Test at 0 V, V_{CC}
I_{IR}	Reset Input Current		–80		-80		µA	V_{RL}=0V
I_{CC}	Supply Current		35		35	24	mA	@ 16 MHz([1])
I_{CC1}	Standby Current		7		7	4.5	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		10	1	µA	STOP Mode V_{IN} = 0 V, V_{CC} ([1])
I_{ALL}	Autolatch Low Current	-10	10	-14	14		µA	

Note:
1. All inputs driven to 0V, V_{CC} and outputs floating.
2. V_{CC} = 5.0V

Table 18. External I/O or Memory READ/WRITE Timing—Standard/Extended Temperature

			T_A = –0°C to 70°C @ 16 MHz		T_A = –40°C to 105°C @ 16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	T_DA(AS)	Address Valid to $\overline{AS}$ Rise Delay	25		25		ns	2,3
2	T_DAS(A)	$\overline{AS}$ Rise to Address Float Delay	35		35		ns	2,3
3	T_DAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid		180		180	ns	1,2,3
4	T_WAS	$\overline{AS}$ Low Width	40		40		ns	2,3
5	T_DAS(DS)	Address Float to $\overline{DS}$ Fall	0		0		ns	
6	T_WDSR	$\overline{DS}$ (Read) Low Width	135		135		ns	1,2,3
7	T_WDSW	$\overline{DS}$ (WRITE) Low Width	80		80		ns	1,2,3
8	T_DDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid		75		75	ns	1,2,3
9	T_HDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	0		0		ns	2,3
10	T_DDS(A)	$\overline{DS}$ Rise to Address Active Delay	50		50		ns	2,3
11	T_DDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	35		35		ns	2,3
12	T_DR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	25		25		ns	2,3
13	T_DDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	35		35		ns	2,3
14	T_DDW(DSW)	WRITE Data Valid to $\overline{DS}$ Fall (WRITE) Delay	25		25		ns	2,3
15	T_DDS(DW)	$\overline{DS}$ Rise to WRITE Data Not Valid Delay	35		35		ns	2,3
16	T_DA(DR)	Address Valid to Read Data Req'd Valid		230		230	ns	1,2,3
17	T_DAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	45		45		ns	2,3
18	T_DDI(DS)	Data Input Setup to $\overline{DS}$ Rise	60		60		ns	1,2,3
19	T_DDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	30		30		ns	2,3

Notes:
1. When using extended memory timing add 2 TpC.
2. Timing numbers provided are for minimum T_PC.
3. See Clock Cycle Dependent Characteristics table

Additional Timing

Figure 39 illustrates the timing characteristics of the Z86C91 MCU with respect to system clock functions. See Table 20 for descriptions of the numbered timing parameters in the figure.

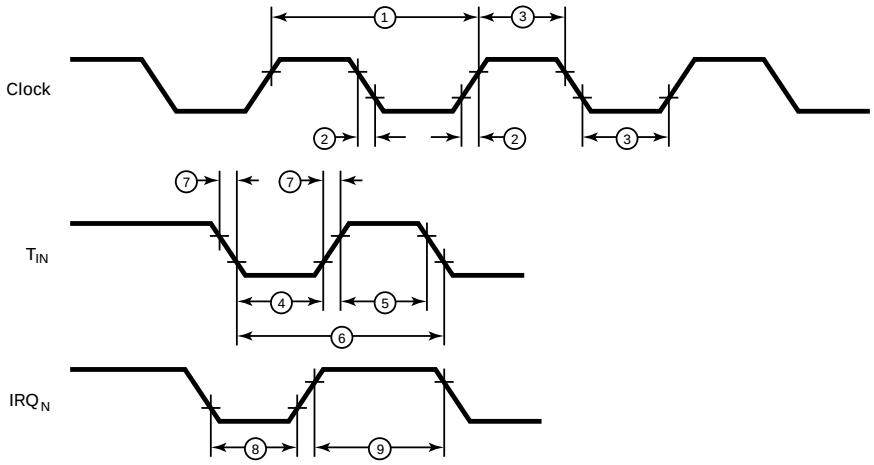

Figure 39. Additional Timing

Table 20. Additional Timing (Standard and Extended Temperature)

			T_A = 0ºC to +70ºC 16 MHz		T_A =-4 0ºC to +105ºC 16 MHz			
No	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	T_PC	Input Clock Period	62.5	1000	62.5	1000	ns	1
2	T_RC,T_FC	Clock Input Rise & Fall Times		10		10	ns	1
3	T_WC	Input Clock Width	25		25		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	75		75		ns	2
5	$T_WT_{IN}H$	Timer Input High Width	$3T_PC$		$3T_PC$			2

Notes:
1. Clock timing references use 3.8V for a logic one and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request via Port 3.
4. The interrupt request via Port 3 (P31–P33).
5. The interrupt request via Port 3 (P30).

Table 20. Additional Timing (Standard and Extended Temperature) (Continued)

			T_A = 0°C to +70°C 16 MHz		T_A =-4 0°C to +105°C 16 MHz			
No	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
6	T_PT_{IN}	Timer Input Period	$8T_PC$		$8T_PC$			2
7	T_RT_{IN},T_FT_{IN}	Timer Input Rise & Fall Timer	100		100		ns	2
8A	T_WIL	Interrupt Request Low Time	70		70		ns	2,4
8B	T_WIL	Interrupt Request Low Time	$3T_PC$		$3T_PC$			2,5
9	T_WIH	Interrupt Request Input High Time	$3T_PC$		$3T_PC$			2,3

Notes:
1. Clock timing references use 3.8V for a logic one and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request via Port 3.
4. The interrupt request via Port 3 (P31–P33).
5. The interrupt request via Port 3 (P30).

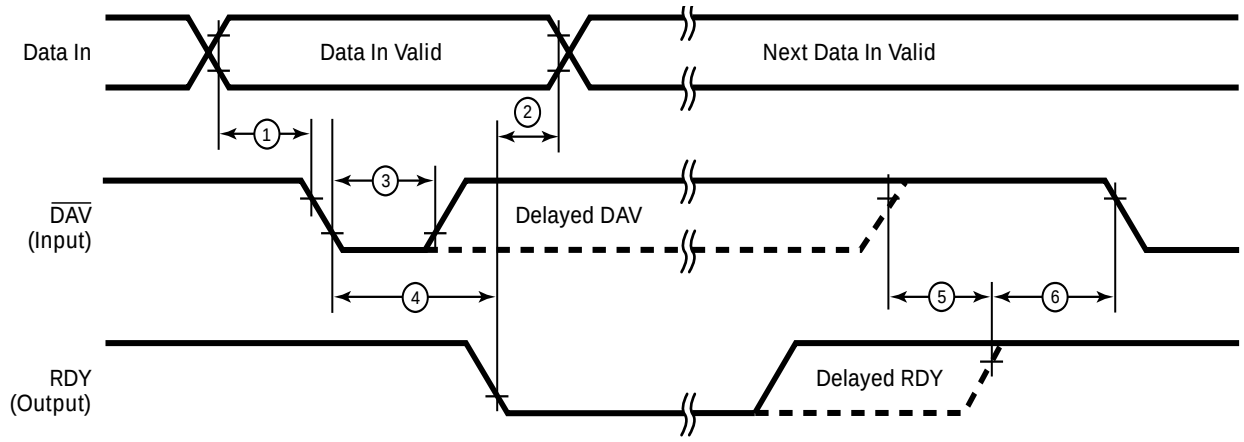

Figure 40. Input Handshake Timing