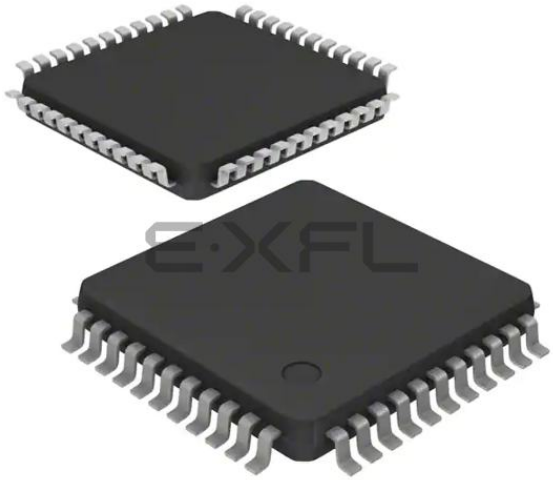

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9116fsc00tr

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Document Disclaimer

List of Tables

Functional Block Diagrams

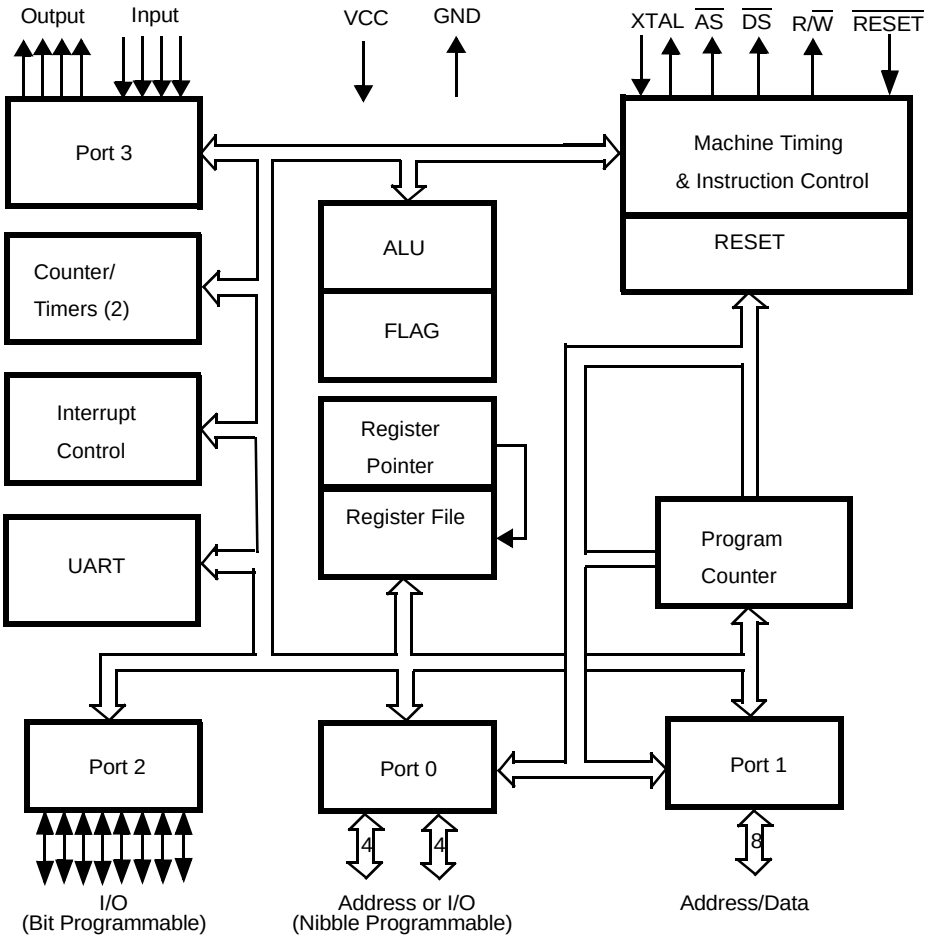


Figure 1. Z86C91 Functional Block Diagram

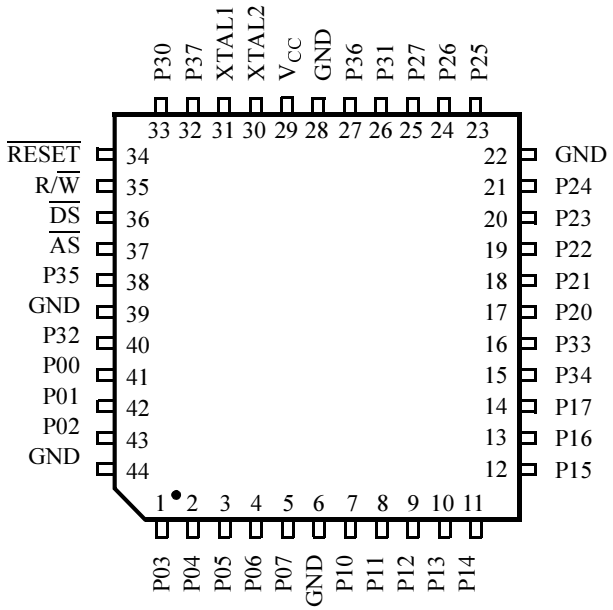


Figure 3. 44-Pin PQFP Pin Configuration

Table 13. 44-Pin PQFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0, Bits 3-7	Input/Output
6	GND	Ground	Output
7-14	P10-P17	Port 1, Bits 0-7	Input/Output
15	P34	Port 3, Bit 4	Output
16	P33	Port 3, Bit 3	Intput
17-21	P20-P24	Port 2, Bits 0-4	Input/Output
22	GND	Ground	Output
23-25	P25-P27	Port 2, Bits 5-7	Input/Output
26	P31	Port 3, Bit 1	Input
27	P36	Port 3, Bit 6	Output
28	GND	Ground	Output

Table 13. 44-Pin PQFP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3, Bit 7	Output
33	P30	Port 3, Bit 0	Intput
34	$\overline{\text{RESET}}$	Reset	Input
35	R/$\overline{\text{W}}$	Read/Write	Output
36	$\overline{\text{DS}}$	Data Strobe	Output
37	$\overline{\text{AS}}$	Address Strobe	Output
38	P35	Port 3, Bit 5	Output
39	GND	Ground	Output
40	P32	Port 3, Bit 2	Input
41-43	P00-P02	Port 0, Bits 0-2	Input/Output
44	GND	Ground	Output

Port 1 (P17–P10). Port 1 is an 8-bit, TTL- compatible port (Figure 6), with multiplexed Address (A7–A0) and Data (D7–D0) ports for interfacing external memory. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 6). A hardware RESET is required to exit this high-impedance state.

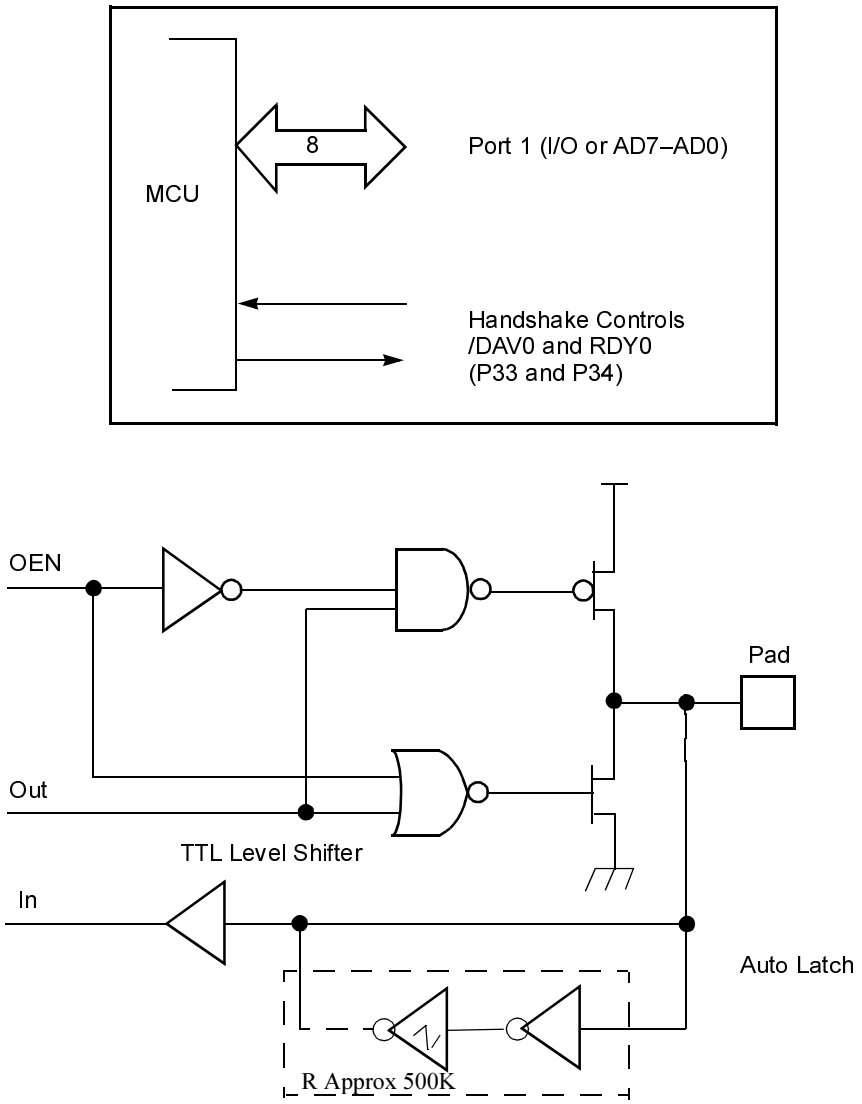


Figure 6. Port 1 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit programmable, bidirectional, TTL-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently or globally as an open-drain output. Port 2 is always available for I/O operation.When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines $\overline{\text{DAV2}}$ and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7). After a RESET, Port 2 is configured as an input port. The Port 2 output portion of the circuit has open-drain as it's default configuration.

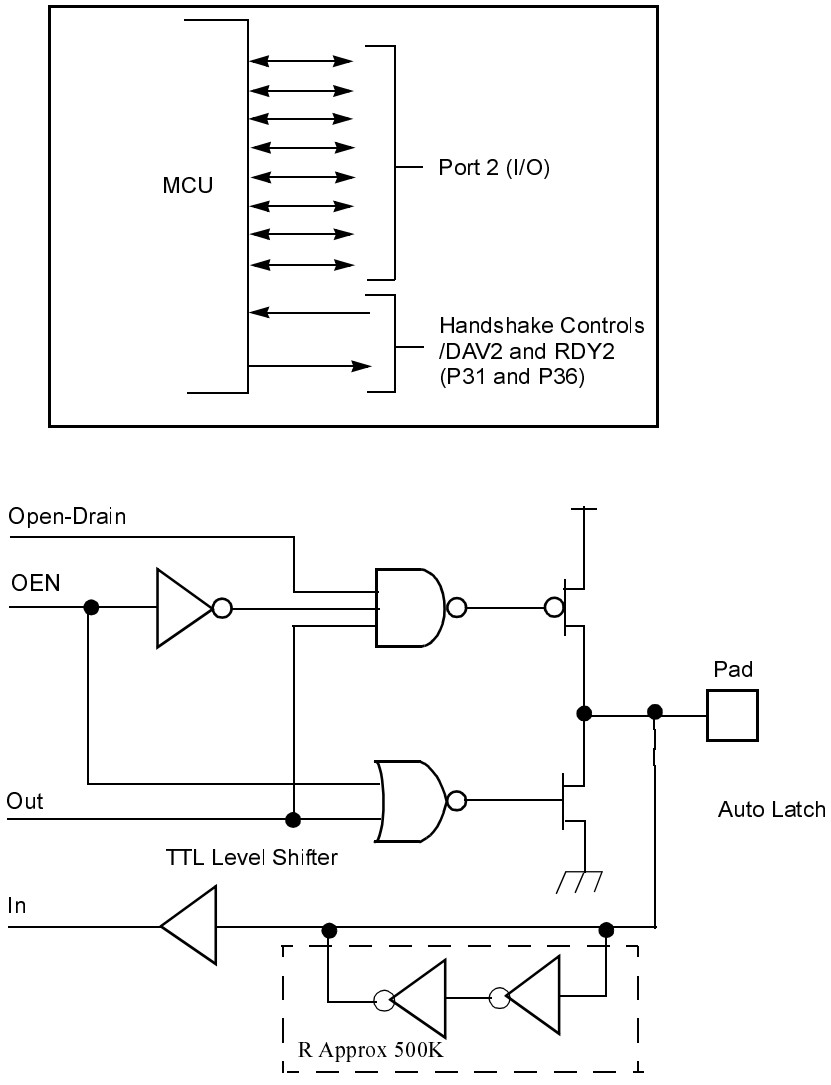


Figure 7. Port 2 Configuration

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

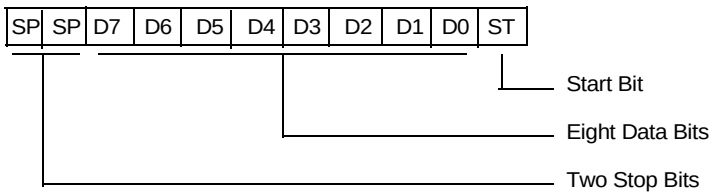


Figure 9. Transmitted Data (No Parity)

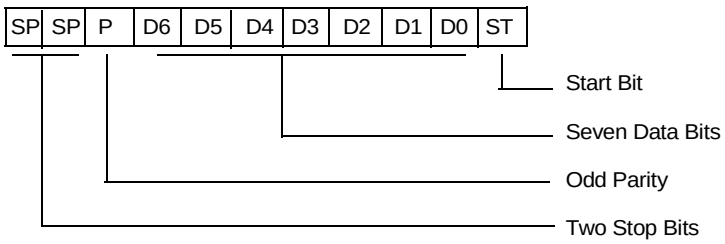


Figure 10. Transmitted Data (With Parity)

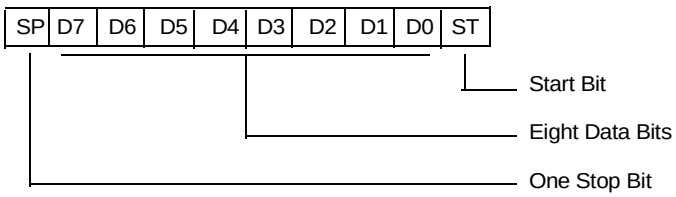


Figure 11. Received Data (No Parity)

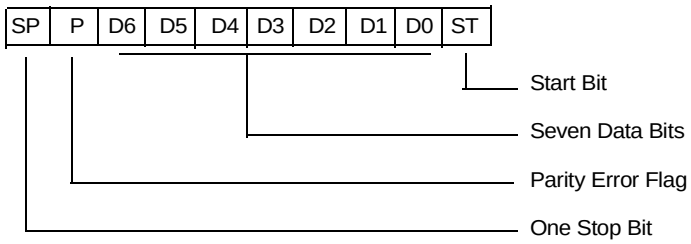


Figure 12. Received Data (With Parity)

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Stack Pointer (Bits 15-8)	SPH
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240	Serial I/O	SIO
239	General Purpose Registers	
4		
3	Port 3	P3
2	Port 2	P2
1	Reserved	Reserved
0	Port 0	P0

Figure 15. Register File

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

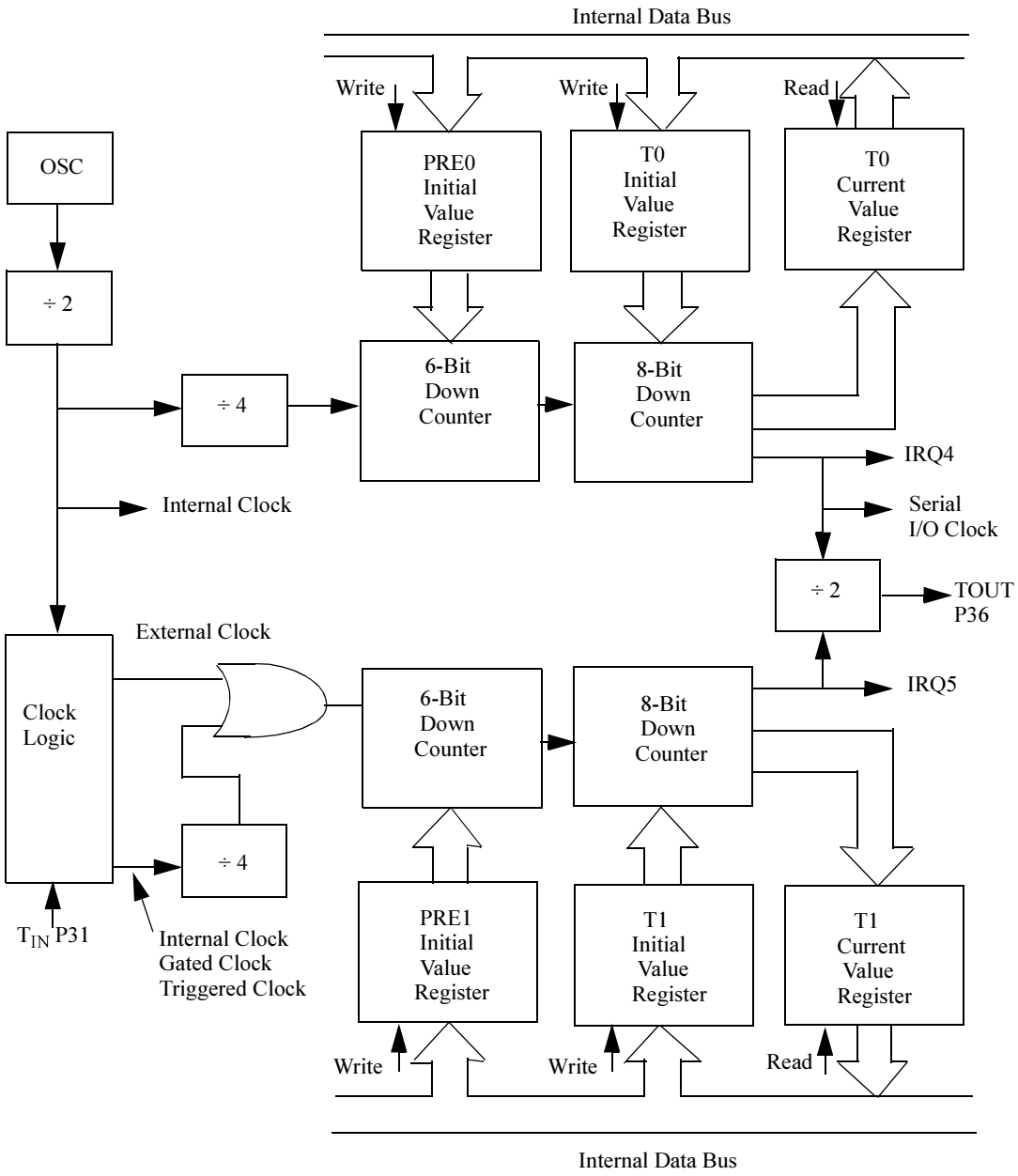


Figure 18. Counter/Timer Block Diagram

Interrupts. The Z8 has six different interrupts from eight different sources. These interrupts are maskable and prioritized. The 8 sources are divided as follows: 4 sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and 2 are claimed by counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register

All interrupts are vectored through locations in Program Memory. When an interrupt request is granted, the interrupt machine cycle is activated. This resets the interrupt request flag and disables all of the subsequent interrupts, except Program Counter and Status Flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16 bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Nested interrupts are supported by enabling interrupts in the interrupt service routine.

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48TpC (external XTAL clock cycles) are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

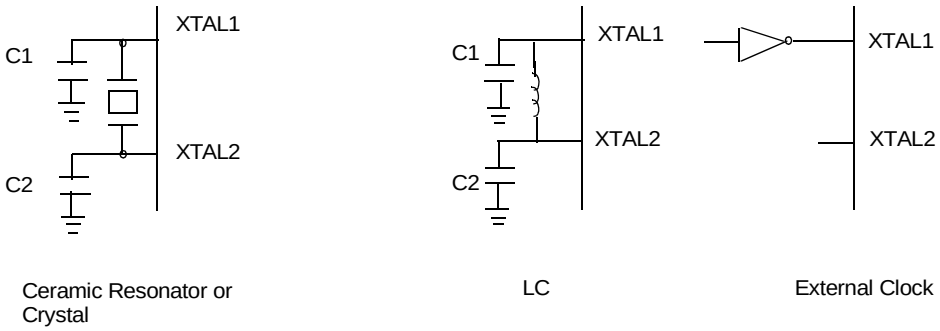


Figure 20. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation or the peripheral clock. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at location `000Ch`.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. Therefore, the user must execute a NOP (Op Code = `FFh`) immediately before the appropriate sleep instruction. For example:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

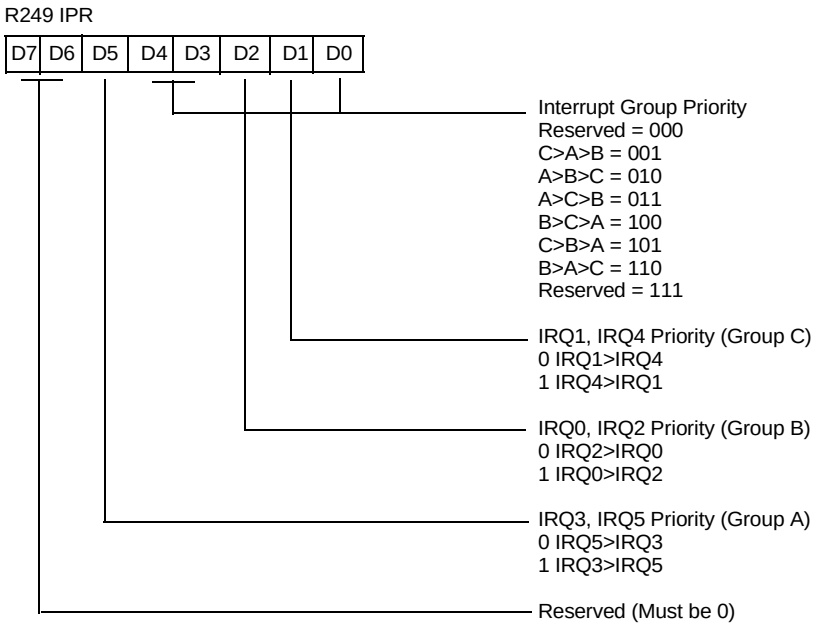


Figure 30. Interrupt Priority Register (F9h: Write Only)

Interrupt Request Register

The Interrupt Request Register, IRQ, controls interrupt functions and is shown in Figure 31.

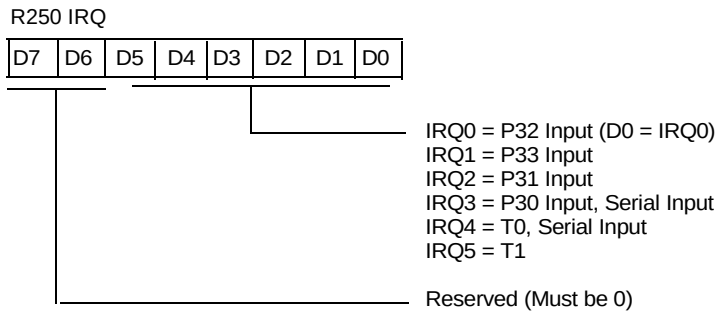


Figure 31. Interrupt Request Register (FAh: Read/Write)

Interrupt Mask Register

The Interrupt Mask Register, IMR, controls interrupt functions and is shown in Figure 32.

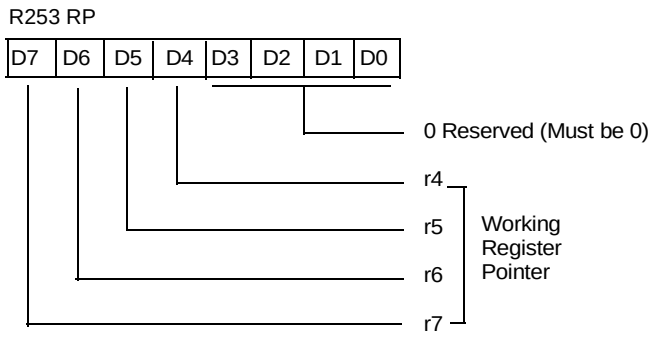


Figure 34. Register Pointer Register (FDh: Read/Write)

Stack Pointer High Register

The Stack Pointer High Register, SPH, controls pointer functions in the upper byte when the external stack is used and is shown in Figure 35.

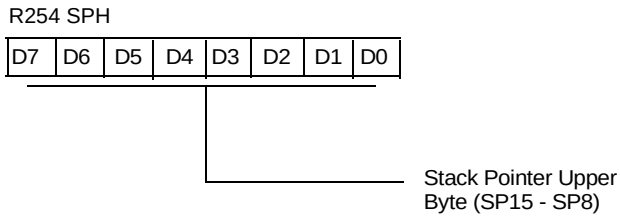


Figure 35. Stack Pointer Register (FEh: Read/Write)

Stack Pointer Low Register

The Stack Pointer Low Register, SPL, controls pointer functions in the lower byte and is shown in Figure 36.

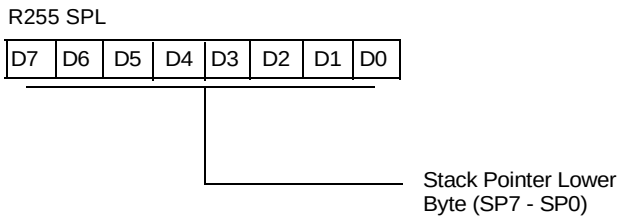


Figure 36. Stack Pointer Register (FFh: Read/Write)

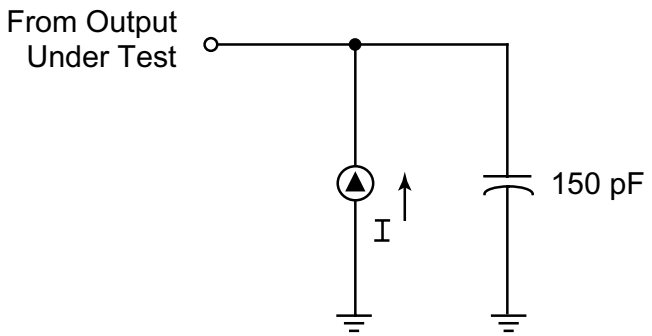


Figure 37. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC Electrical Characteristics

Table 17. DC Electrical Characteristics at Standard and External Temperatures

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical[2]		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@25°C**	**Units**	**Conditions**
	Max Input Voltage		7		7		V	I_{IH} <200µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	Driven by External Clock Generator

Note:
1. All inputs driven to 0V, V_{CC} and outputs floating.
2. V_{CC} = 5.0V

AC Electrical Characteristics

Figure 38 illustrates the timing characteristics of the Z86C91MCU with respect to external input/output sources. See Table 18 for descriptions of the numbered timing parameters in the figure.

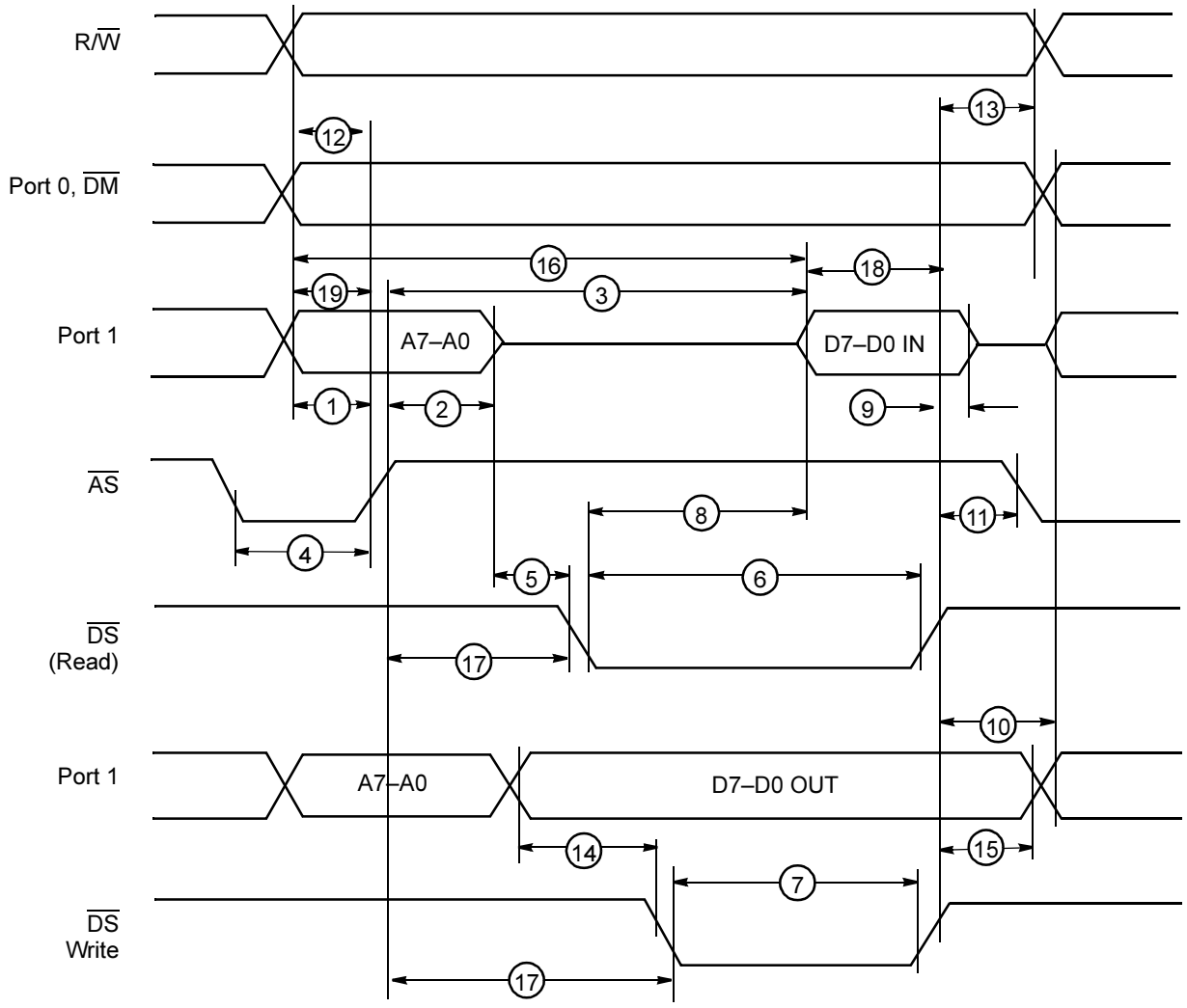


Figure 38. External I/O or Memory READ and WRITE Timing

Table 20. Additional Timing (Standard and Extended Temperature) (Continued)

			T_A = 0°C to +70°C 16 MHz		T_A =-4 0°C to +105°C 16 MHz			
No	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
6	T_PT_{IN}	Timer Input Period	$8T_PC$		$8T_PC$			2
7	T_RT_{IN},T_FT_{IN}	Timer Input Rise & Fall Timer	100		100		ns	2
8A	T_WIL	Interrupt Request Low Time	70		70		ns	2,4
8B	T_WIL	Interrupt Request Low Time	$3T_PC$		$3T_PC$			2,5
9	T_WIH	Interrupt Request Input High Time	$3T_PC$		$3T_PC$			2,3

Notes:
1. Clock timing references use 3.8V for a logic one and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request via Port 3.
4. The interrupt request via Port 3 (P31–P33).
5. The interrupt request via Port 3 (P30).

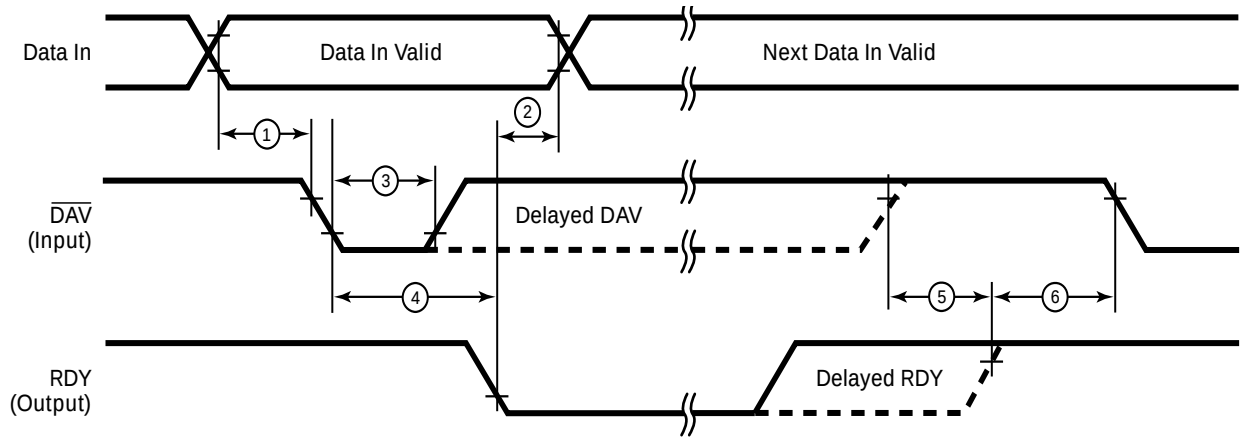


Figure 40. Input Handshake Timing

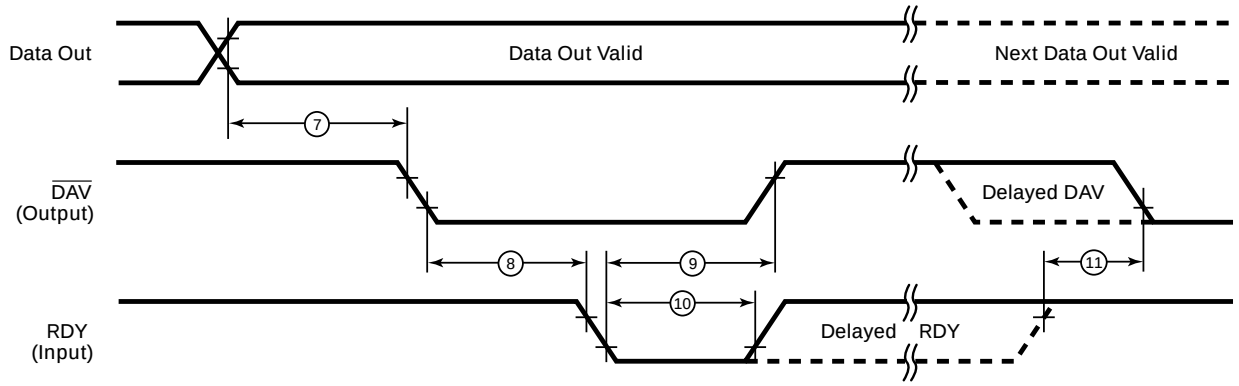
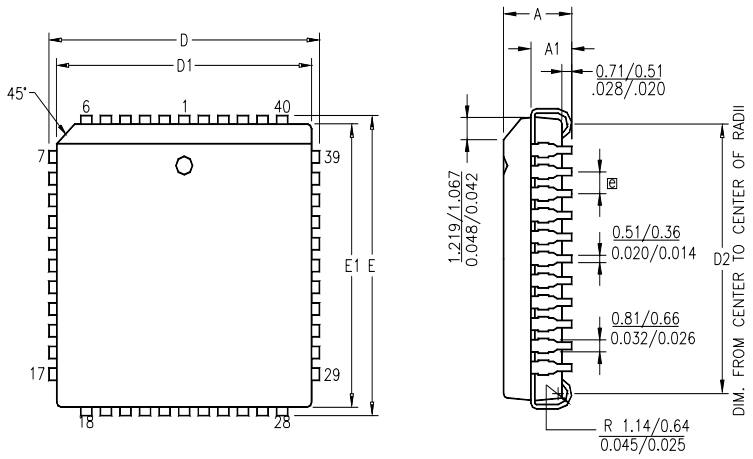


Figure 41. Output Handshake Timing

Table 21. Handshake Timing (Standard and Extended Temperatures)

No	Symbol	Parameter	T_A = 0ºC to +70ºC Min	T_A = 0ºC to +70ºC Max	T_A = -40ºC to +105ºC Min	T_A = -40ºC to +105ºC Max	Data Direction
1	T_SDI(DAV)	Data In Setup Time	0		0		Input
2	T_HDI(RDY)	Data In Hold Time	145		145		Input
3	T_WDAV	Data Available Width	110		110		Input
4	T_DDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	Input
5	T_DDAVId(RDY)	DAV Out to DAV Fall Delay		115		115	Input
6	RDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	0		0		Input
7	T_DD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	Output
8	T_DDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		Output
9	T_DRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	Output
10	T_WRDY	RDY Width	110		110		Output
11	T_DRDY0$_D$(DAV)	RDY Rise to DAV Fall Delay		115		115	Output

Note: All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
   INCH

Figure 43. 44-Pin PLCC Package Diagram