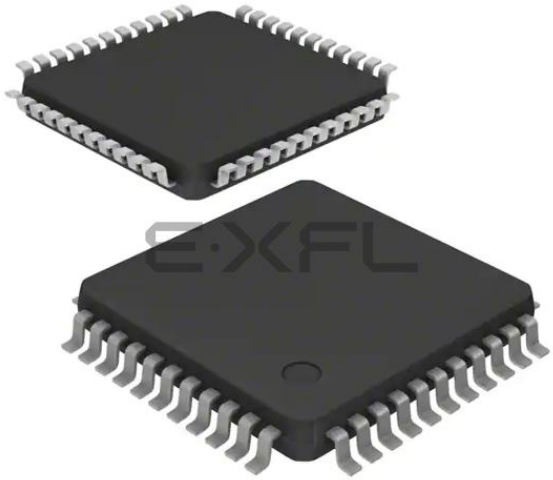

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9116fsg

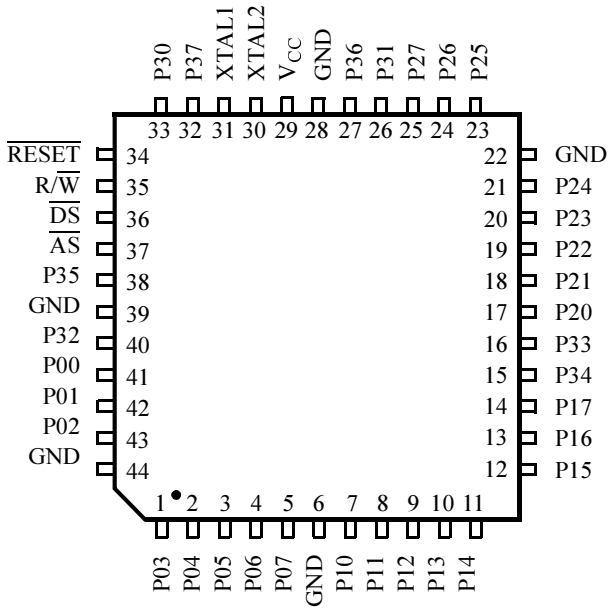

Figure 3. 44-Pin PQFP Pin Configuration

Table 13. 44-Pin PQFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0, Bits 3-7	Input/Output
6	GND	Ground	Output
7-14	P10-P17	Port 1, Bits 0-7	Input/Output
15	P34	Port 3, Bit 4	Output
16	P33	Port 3, Bit 3	Intput
17-21	P20-P24	Port 2, Bits 0-4	Input/Output
22	GND	Ground	Output
23-25	P25-P27	Port 2, Bits 5-7	Input/Output
26	P31	Port 3, Bit 1	Input
27	P36	Port 3, Bit 6	Output
28	GND	Ground	Output

Table 13. 44-Pin PQFP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3, Bit 7	Output
33	P30	Port 3, Bit 0	Intput
34	$\overline{\text{RESET}}$	Reset	Input
35	R/$\overline{\text{W}}$	Read/Write	Output
36	$\overline{\text{DS}}$	Data Strobe	Output
37	$\overline{\text{AS}}$	Address Strobe	Output
38	P35	Port 3, Bit 5	Output
39	GND	Ground	Output
40	P32	Port 3, Bit 2	Input
41-43	P00-P02	Port 0, Bits 0-2	Input/Output
44	GND	Ground	Output

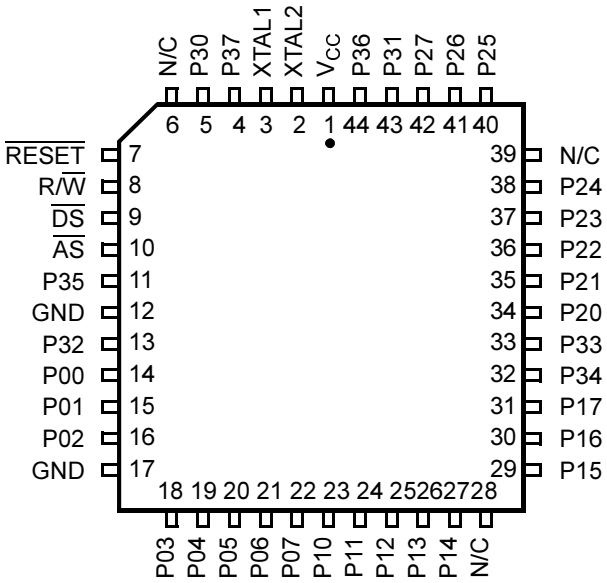

Figure 4. 44-Pin PLCC Configuration

Table 14. 44-Pin PLCC Configuration

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	$\overline{RESET}$	Reset	Input
8	R/$\overline{W}$	Read/Write	Output
9	$\overline{DS}$	Data Strobe	Output
10	$\overline{AS}$	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground V_{SS}	Output

Port 2 (P27–P20). Port 2 is an 8-bit programmable, bidirectional, TTL-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently or globally as an open-drain output. Port 2 is always available for I/O operation.When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines $\overline{\text{DAV2}}$ and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7). After a RESET, Port 2 is configured as an input port. The Port 2 output portion of the circuit has open-drain as it's default configuration.

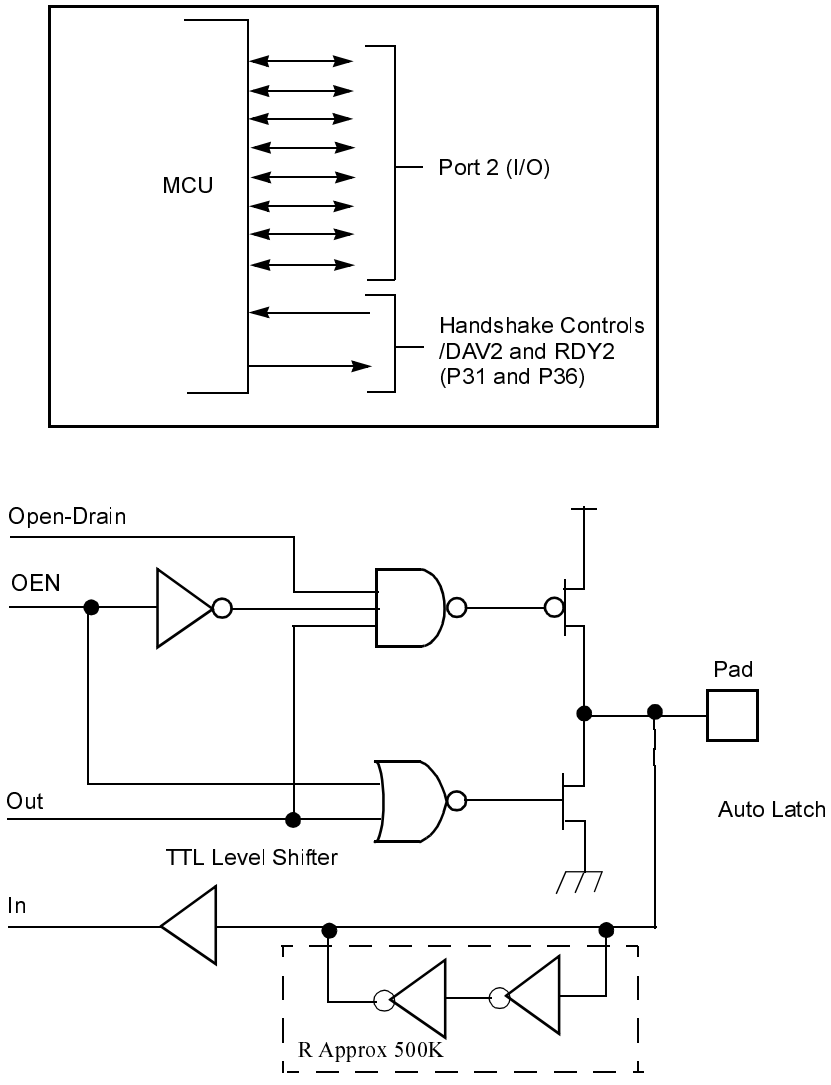

Figure 7. Port 2 Configuration

Table 15. Port 3 Pin Assignments

Pin	I/O	Control Timer	Interrupt	P0 HS	P2 HS	Ext	UART
P30	IN		IRQ3				Serial In
P31	IN	T_{IN}	IRQ2		D/R		
P32	IN		IRQ0	D/R			
P33	IN		IRQ1				
P34	OUT					$\overline{DM}$	
P35	OUT			R/D			
P36	OUT	T_{OUT}			R/D		
P37	OUT						Serial Out

Notes:
HS = Handshake Signals
D = $\overline{DAV}$ (Data Available)
R = RDY (Ready)

Autolatch. The autolatch places valid CMOS levels on all inputs that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Autolatches are available on Port 0, Port 1, Port 2, and P3 inputs.

$\overline{RESET}$ (input, Low). Initializes the MCU. RESET occurs through external reset only. During Power-On Reset, the externally-generated reset drives the $\overline{RESET}$ pin Low for the POR time. Pull-up is provided internally.

Caution: $\overline{RESET}$ depends on oscillator operation to achieve full reset conditions.

$\overline{RESET}$ is a Schmitt-triggered input. During the RESET cycle, $\overline{DS}$ is held active Low while $\overline{AS}$ cycles at a rate of $T_PC \div 2$. Program execution begins at location `000Ch`, after the $\overline{RESET}$ is released.

When program execution begins, $\overline{AS}$ and $\overline{DS}$ toggles only for external memory accesses. The Z8 can only exit Stop Mode by using the $\overline{RESET}$ pin.The Z8 does reset all registers on a Stop-Mode Recovery operation out of STOP mode.

Functional Description

The Z8 MCU incorporates the following functions that enhance the standard Z8® architecture and provide the user with increased design flexibility:

- Reset
- Program Memory
- Data Memory
- Working Register
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- HALT and STOP Modes
- Port Configuration Register

RESET. The device is reset in the following condition:

- External Reset

Automatic Power-On Reset circuitry is not built into this Z8. This Z8 requires an external reset circuit to reset upon power-up. The internal pull-up resistor is on the $\overline{\text{RESET}}$ pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a low-value pull-up resistor be used.

Program Memory. The Z86C91 can address up to 64 KB of external program memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location `000Ch` after reset. See Figure 13.

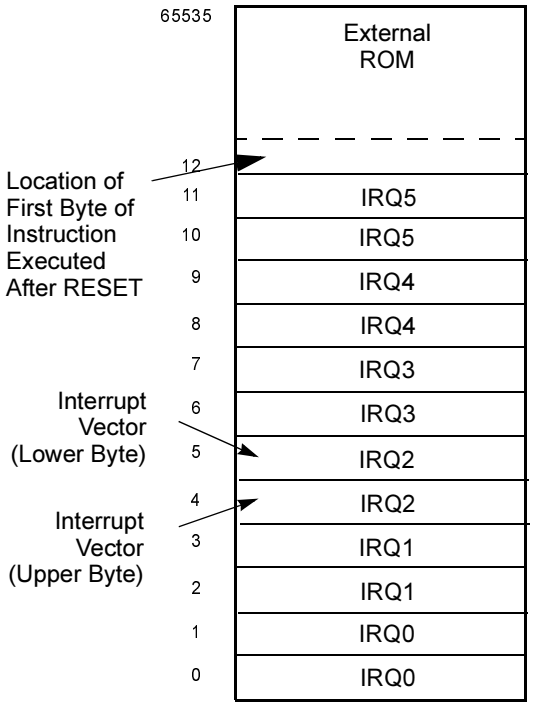

Figure 13. Program Memory Map

Data Memory ($\overline{DM}$). The Z86C91addresses up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that is programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode.

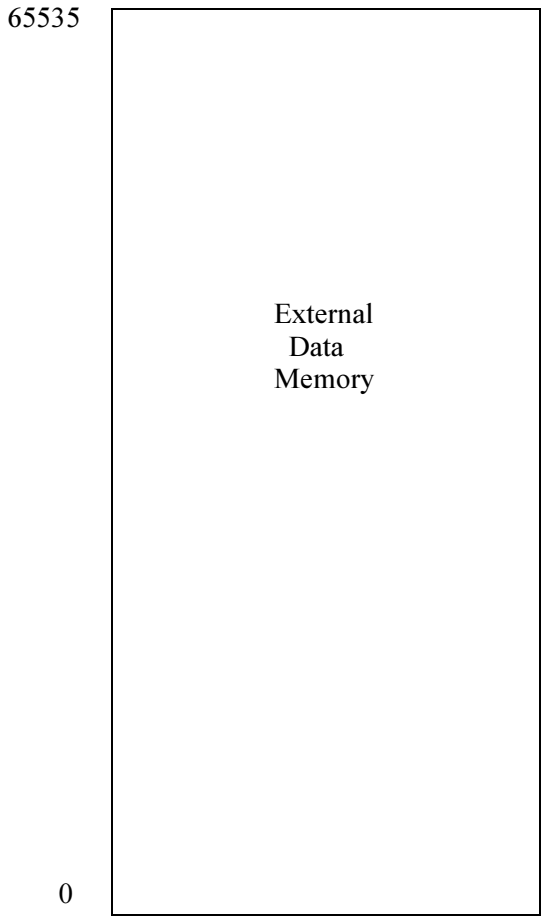

Figure 14. Data Memory Map

Register File. The register file contains three I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Stack Pointer (Bits 15-8)	SPH
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240	Serial I/O	SIO
239	General Purpose Registers	
4		
3	Port 3	P3
2	Port 2	P2
1	Reserved	Reserved
0	Port 0	P0

Figure 15. Register File

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

General-Purpose Registers (GPR). General-purpose registers are undefined after the device is powered up. These registers keep the most recent value after any RESET, as long as the RESET occurs in the V_{CC} voltage-specified operating range. General-purpose registers are not guaranteed to keep their most recent state from if V_{CC} drops below the minimum V_{CC} operating range.

Stack Pointer. The Z86C91 has a 16-bit Stack Pointer (SPH and SPL) used for the external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (SPL) is used for the internal stack that resides within the 236 general-purpose registers. Stack Pointer High (SPH) is used as a general-purpose register only when using an internal stack.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 17).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both the counter and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to START, STOP, restart to CONTINUE, or restart from the initial value. The counters can also be programmed to STOP upon reaching 1 (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO–N CONTINUOUS mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. Reading the prescalers returns the value `FFh`. The clock source for T1 is user-definable and is either the internal micro controller clock divide-by-four, or an external signal input through Port 3. The maximum frequency of the external timer signal is the XTAL clock signal divided by 8. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or nonretriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as an output (T_{OUT}) through which T0, T1, or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

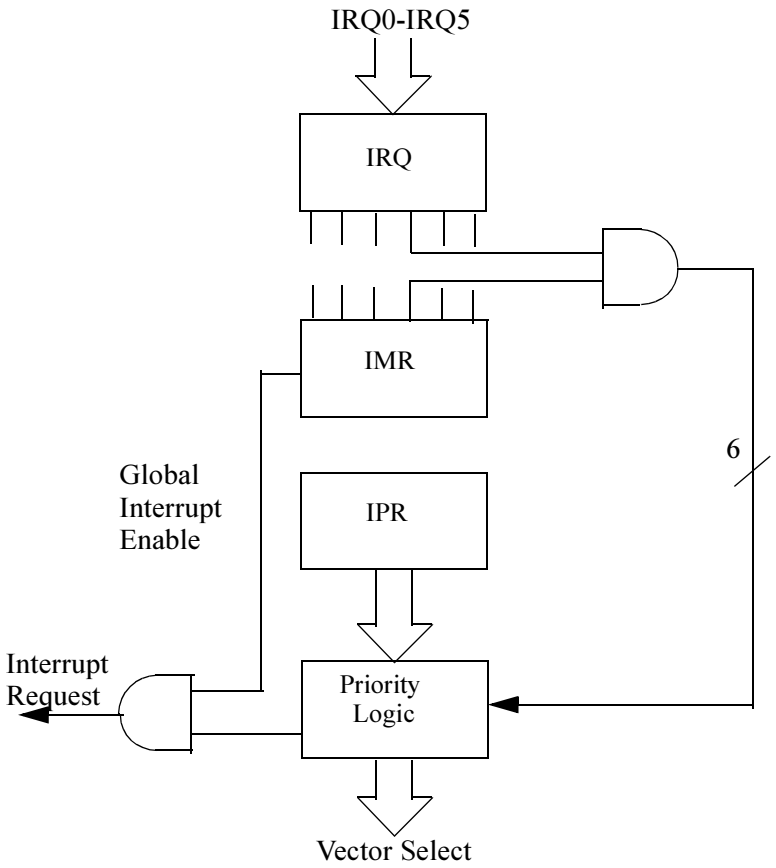

Figure 19. Interrupt Block Diagram

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT-cut, 1MHz to 20 MHz maximum, with a series resistance (RS) of less than or equal to 100Ω when oscillating from 1MHz to 16MHz.

The crystal should be connected across XTAL1 and XTAL2 using the oscillator manufacturer's recommended capacitor (10 pF<CL<300pF) from each pin to ground (Figure 20).

Prescaler 1 Register

The Prescaler 1 Register, PRE1, controls clocking functions and is shown in Figure 24.

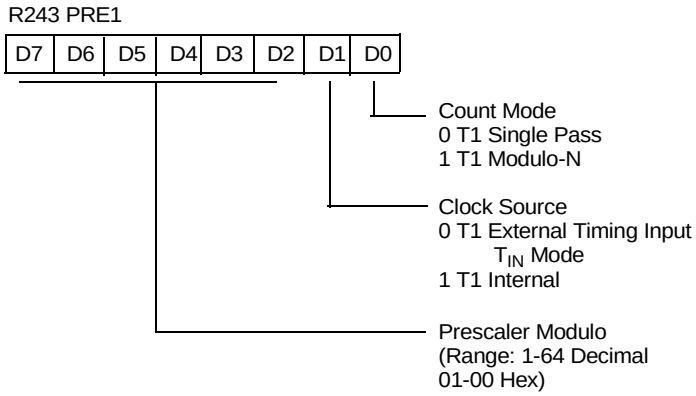

Figure 24. Prescaler 1 Register (F3h: Write Only)

Counter/Timer 0 Register

The Counter/Timer 0 Register, T0 is shown in Figure 25.

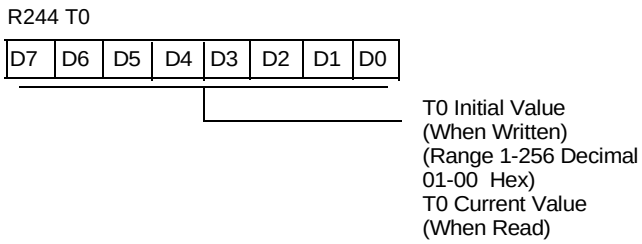

Figure 25. Counter/Timer 0 Register (F4h: Read/Write)

Prescaler 0 Register

The Prescaler 0 Register PRE0 controls clocking functions and is shown in Figure 26.

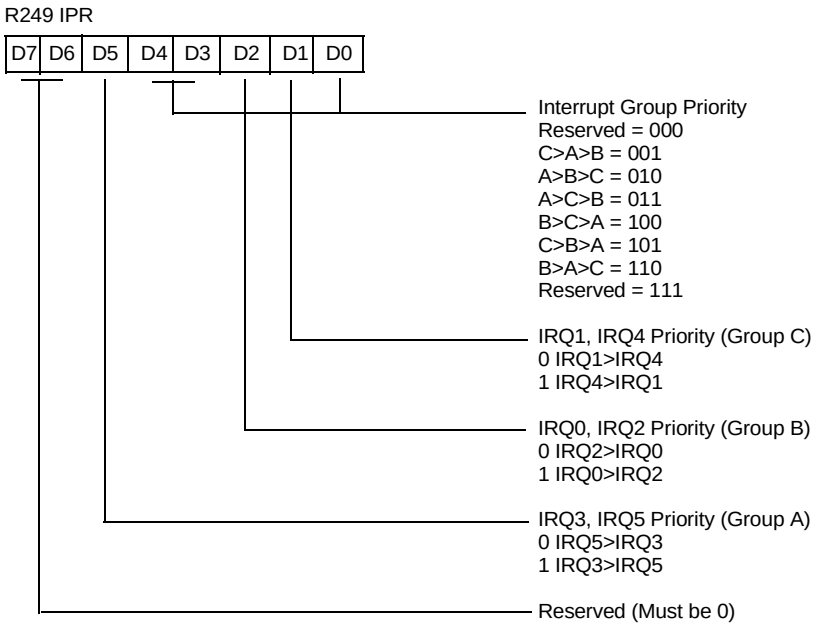

Figure 30. Interrupt Priority Register (F9h: Write Only)

Interrupt Request Register

The Interrupt Request Register, IRQ, controls interrupt functions and is shown in Figure 31.

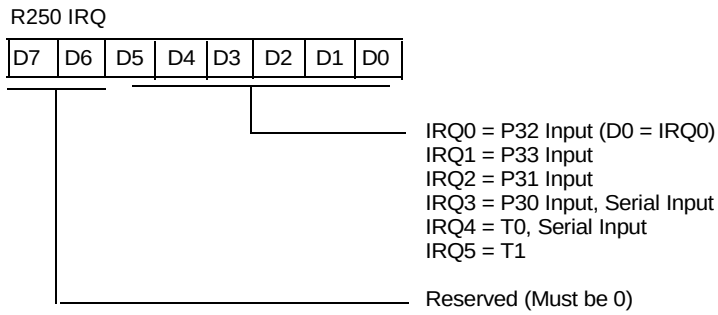

Figure 31. Interrupt Request Register (FAh: Read/Write)

Interrupt Mask Register

The Interrupt Mask Register, IMR, controls interrupt functions and is shown in Figure 32.

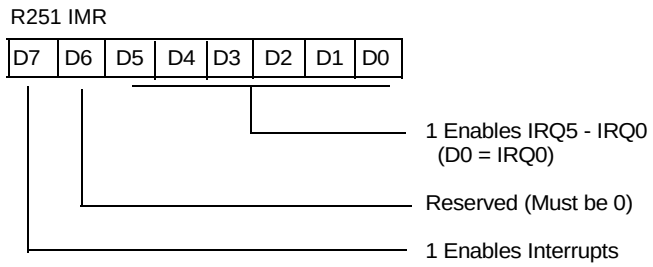

Figure 32. Interrupt Mask Register (FBh: Read/Write)

Flags Register

The CPU sets flags in the Flags Register, FLAGS, to allow the user to perform tests based on differing logical states. The FLAGS Register is shown in Figure 33 .

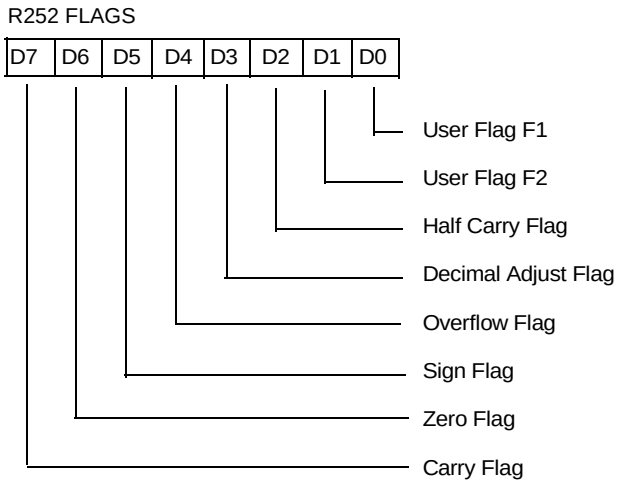

Figure 33. Flags Register (FCh: Read/Write)

Register Pointer Register

The Register Pointer Register, RP, controls pointer functions in the working registers and is shown in Figure 34.

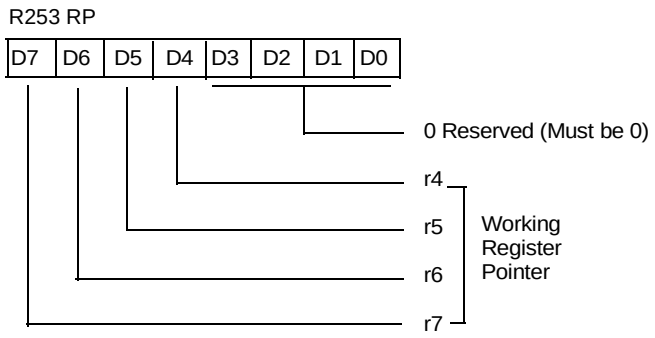

Figure 34. Register Pointer Register (FDh: Read/Write)

Stack Pointer High Register

The Stack Pointer High Register, SPH, controls pointer functions in the upper byte when the external stack is used and is shown in Figure 35.

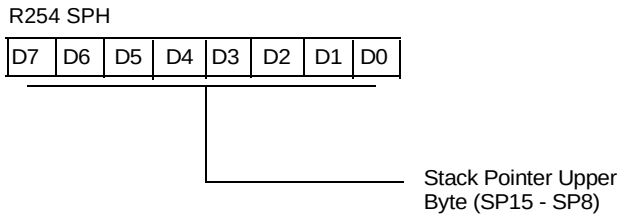

Figure 35. Stack Pointer Register (FEh: Read/Write)

Stack Pointer Low Register

The Stack Pointer Low Register, SPL, controls pointer functions in the lower byte and is shown in Figure 36.

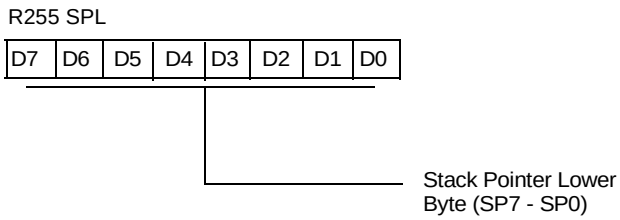

Figure 36. Stack Pointer Register (FFh: Read/Write)

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than the Absolute Maximum Ratings listed in Table 16 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STO}	Storage Temperature	–65	+150	C
T_A	Operating Ambient Temperature		[2]	C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 37).

AC Electrical Characteristics

Figure 38 illustrates the timing characteristics of the Z86C91MCU with respect to external input/output sources. See Table 18 for descriptions of the numbered timing parameters in the figure.

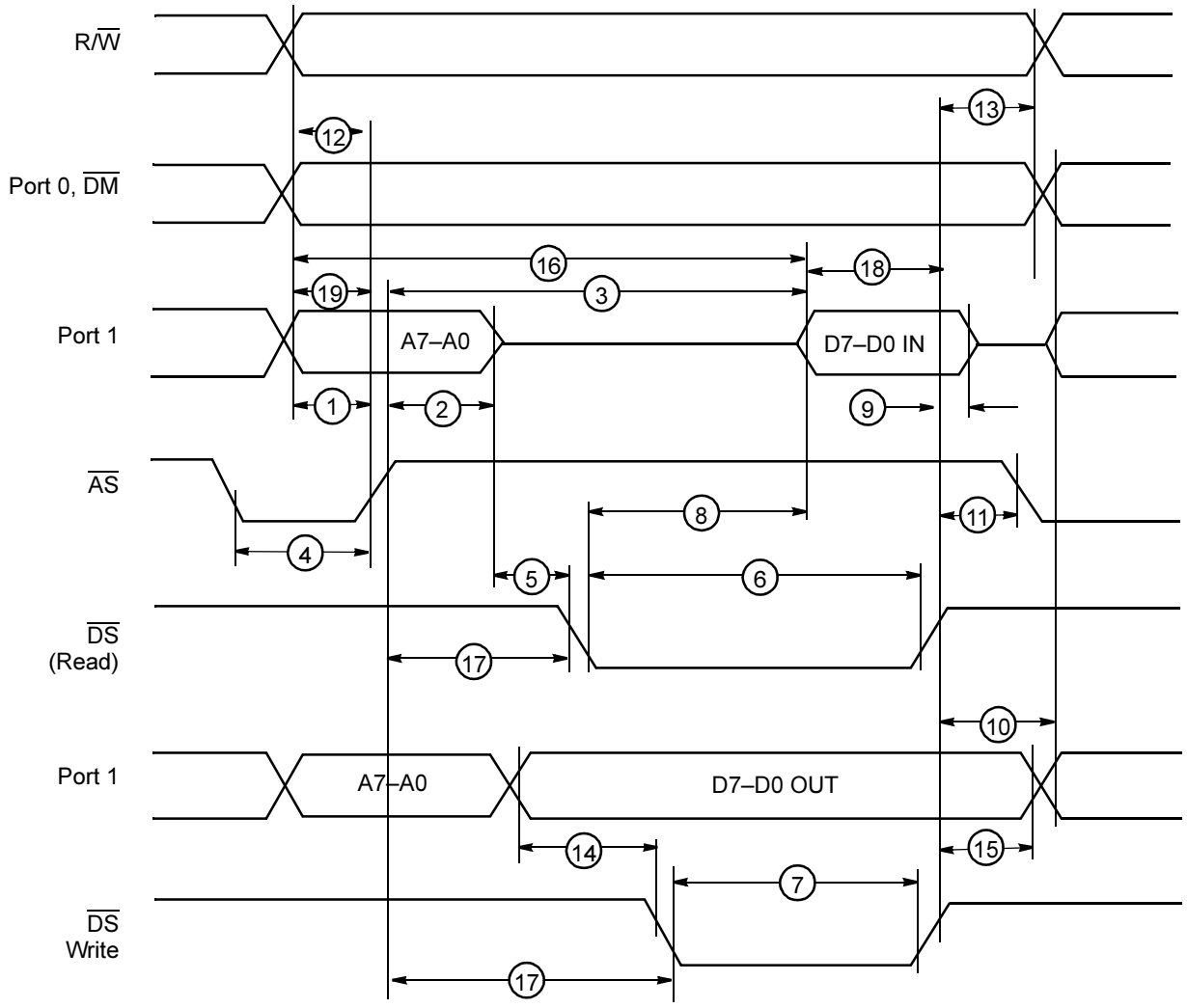

Figure 38. External I/O or Memory READ and WRITE Timing

Table 18. External I/O or Memory READ/WRITE Timing—Standard/Extended Temperature

			T_A = –0°C to 70°C @ 16 MHz		T_A = –40°C to 105°C @ 16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	T_DA(AS)	Address Valid to $\overline{AS}$ Rise Delay	25		25		ns	2,3
2	T_DAS(A)	$\overline{AS}$ Rise to Address Float Delay	35		35		ns	2,3
3	T_DAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid		180		180	ns	1,2,3
4	T_WAS	$\overline{AS}$ Low Width	40		40		ns	2,3
5	T_DAS(DS)	Address Float to $\overline{DS}$ Fall	0		0		ns	
6	T_WDSR	$\overline{DS}$ (Read) Low Width	135		135		ns	1,2,3
7	T_WDSW	$\overline{DS}$ (WRITE) Low Width	80		80		ns	1,2,3
8	T_DDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid		75		75	ns	1,2,3
9	T_HDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	0		0		ns	2,3
10	T_DDS(A)	$\overline{DS}$ Rise to Address Active Delay	50		50		ns	2,3
11	T_DDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	35		35		ns	2,3
12	T_DR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	25		25		ns	2,3
13	T_DDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	35		35		ns	2,3
14	T_DDW(DSW)	WRITE Data Valid to $\overline{DS}$ Fall (WRITE) Delay	25		25		ns	2,3
15	T_DDS(DW)	$\overline{DS}$ Rise to WRITE Data Not Valid Delay	35		35		ns	2,3
16	T_DA(DR)	Address Valid to Read Data Req'd Valid		230		230	ns	1,2,3
17	T_DAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	45		45		ns	2,3
18	T_DDI(DS)	Data Input Setup to $\overline{DS}$ Rise	60		60		ns	1,2,3
19	T_DDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	30		30		ns	2,3

Notes:
1. When using extended memory timing add 2 TpC.
2. Timing numbers provided are for minimum T_PC.
3. See Clock Cycle Dependent Characteristics table

Customer Feedback Form

Z86C91 Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126-3432
Fax: (408) 558-8536
Email: zservice@zilog.com

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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