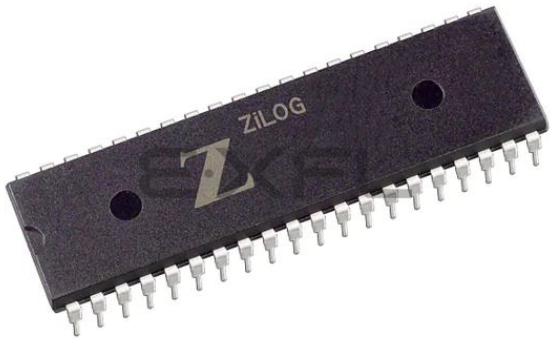

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9116pec

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Table of Contents

List of Figures

List of Tables

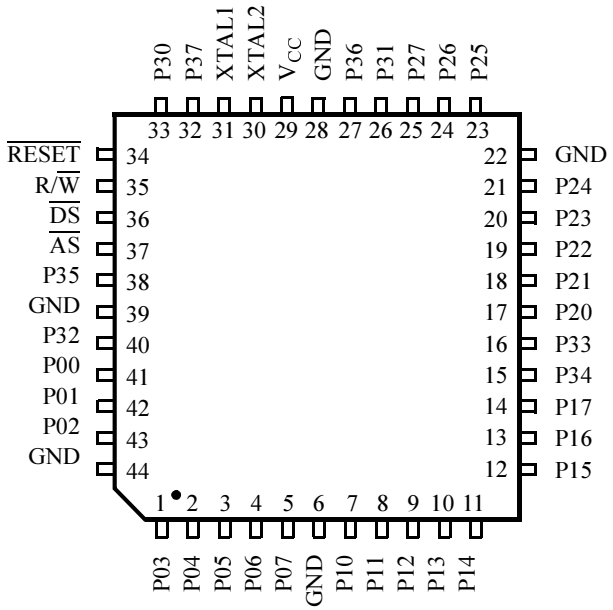

Figure 3. 44-Pin PQFP Pin Configuration

Table 13. 44-Pin PQFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0, Bits 3-7	Input/Output
6	GND	Ground	Output
7-14	P10-P17	Port 1, Bits 0-7	Input/Output
15	P34	Port 3, Bit 4	Output
16	P33	Port 3, Bit 3	Intput
17-21	P20-P24	Port 2, Bits 0-4	Input/Output
22	GND	Ground	Output
23-25	P25-P27	Port 2, Bits 5-7	Input/Output
26	P31	Port 3, Bit 1	Input
27	P36	Port 3, Bit 6	Output
28	GND	Ground	Output

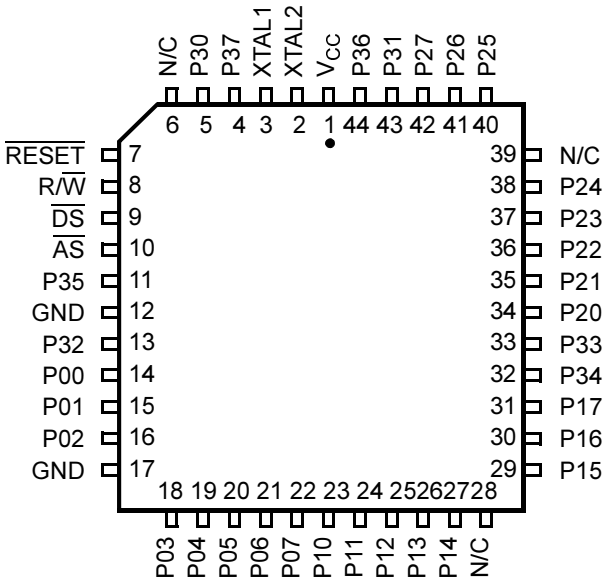

Figure 4. 44-Pin PLCC Configuration

Table 14. 44-Pin PLCC Configuration

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	$\overline{RESET}$	Reset	Input
8	R/$\overline{W}$	Read/Write	Output
9	$\overline{DS}$	Data Strobe	Output
10	$\overline{AS}$	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground V_{SS}	Output

both nibbles are required for I/O operation, they are configured by writing to the Port 01 mode register (P01M).

After a hardware RESET, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode.

Port 0 can be placed in a high-impedance state along with Port 1, $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 5). A hardware RESET is required to exit this high-impedance state.

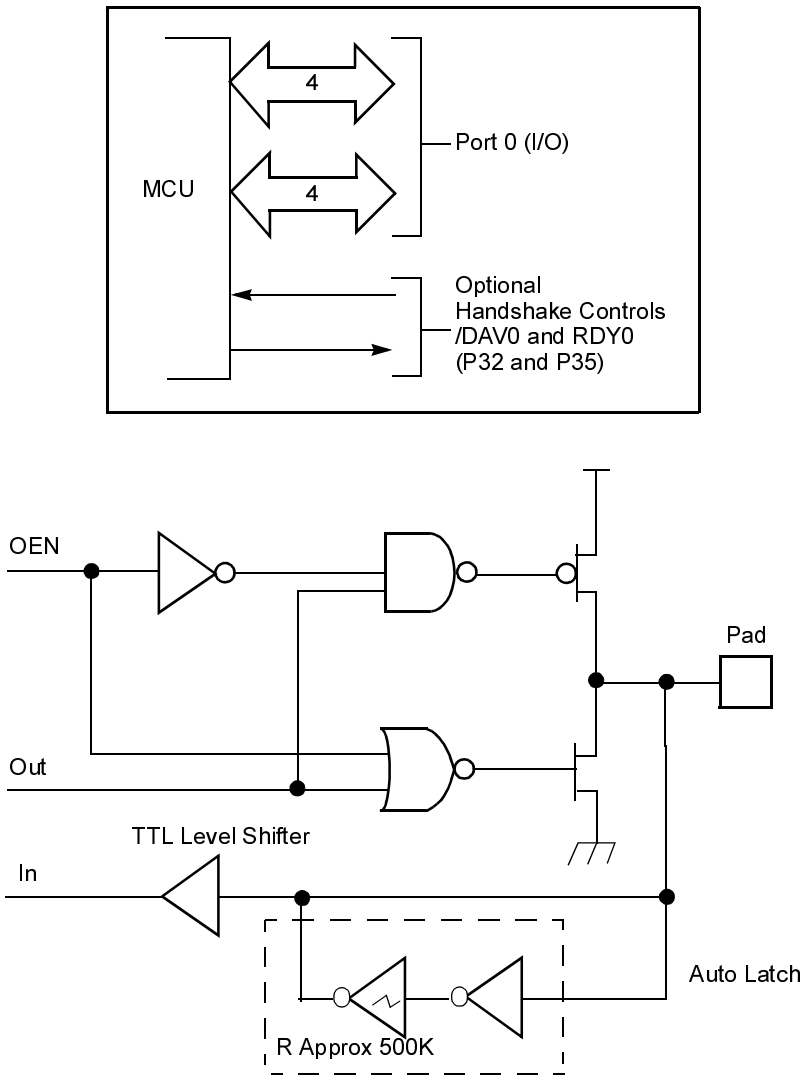

Figure 5. Port 0 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit programmable, bidirectional, TTL-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently or globally as an open-drain output. Port 2 is always available for I/O operation.When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines $\overline{\text{DAV2}}$ and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7). After a RESET, Port 2 is configured as an input port. The Port 2 output portion of the circuit has open-drain as it's default configuration.

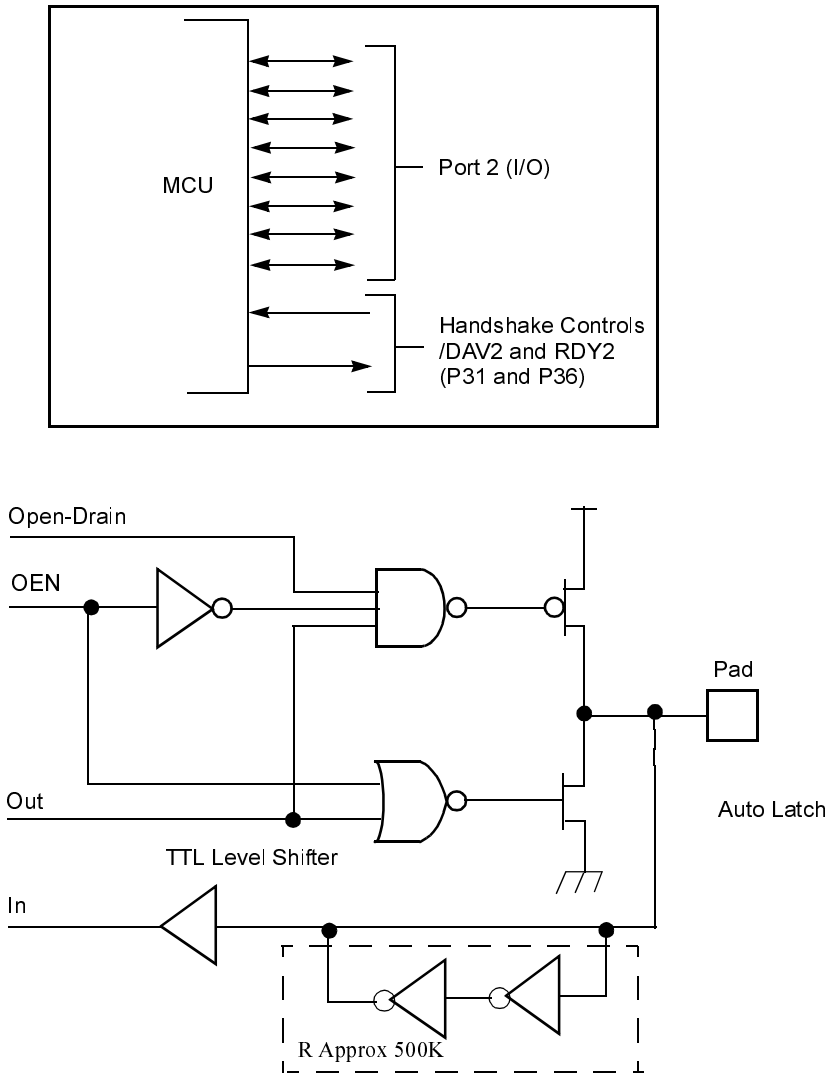

Figure 7. Port 2 Configuration

Functional Description

The Z8 MCU incorporates the following functions that enhance the standard Z8® architecture and provide the user with increased design flexibility:

- Reset
- Program Memory
- Data Memory
- Working Register
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- HALT and STOP Modes
- Port Configuration Register

RESET. The device is reset in the following condition:

- External Reset

Automatic Power-On Reset circuitry is not built into this Z8. This Z8 requires an external reset circuit to reset upon power-up. The internal pull-up resistor is on the $\overline{\text{RESET}}$ pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a low-value pull-up resistor be used.

Program Memory. The Z86C91 can address up to 64 KB of external program memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location `000Ch` after reset. See Figure 13.

General-Purpose Registers (GPR). General-purpose registers are undefined after the device is powered up. These registers keep the most recent value after any RESET, as long as the RESET occurs in the V_{CC} voltage-specified operating range. General-purpose registers are not guaranteed to keep their most recent state from if V_{CC} drops below the minimum V_{CC} operating range.

Stack Pointer. The Z86C91 has a 16-bit Stack Pointer (SPH and SPL) used for the external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (SPL) is used for the internal stack that resides within the 236 general-purpose registers. Stack Pointer High (SPH) is used as a general-purpose register only when using an internal stack.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 17).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both the counter and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to START, STOP, restart to CONTINUE, or restart from the initial value. The counters can also be programmed to STOP upon reaching 1 (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO–N CONTINUOUS mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. Reading the prescalers returns the value `FFh`. The clock source for T1 is user-definable and is either the internal micro controller clock divide-by-four, or an external signal input through Port 3. The maximum frequency of the external timer signal is the XTAL clock signal divided by 8. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or nonretriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as an output (T_{OUT}) through which T0, T1, or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

Interrupts. The Z8 has six different interrupts from eight different sources. These interrupts are maskable and prioritized. The 8 sources are divided as follows: 4 sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and 2 are claimed by counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register

All interrupts are vectored through locations in Program Memory. When an interrupt request is granted, the interrupt machine cycle is activated. This resets the interrupt request flag and disables all of the subsequent interrupts, except Program Counter and Status Flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16 bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Nested interrupts are supported by enabling interrupts in the interrupt service routine.

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48TpC (external XTAL clock cycles) are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

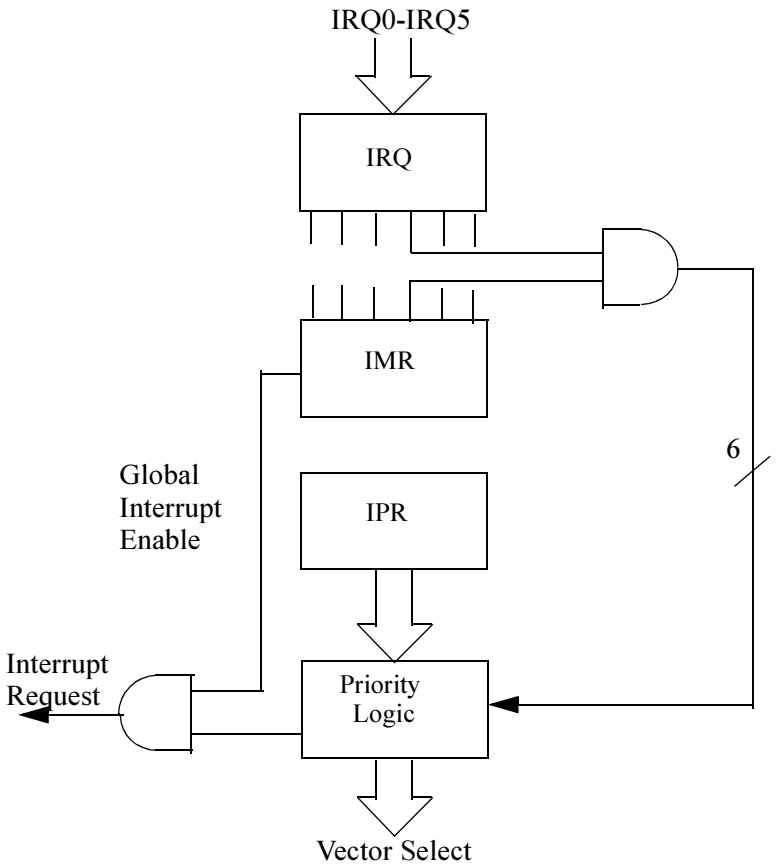

Figure 19. Interrupt Block Diagram

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT-cut, 1MHz to 20 MHz maximum, with a series resistance (RS) of less than or equal to 100Ω when oscillating from 1MHz to 16MHz.

The crystal should be connected across XTAL1 and XTAL2 using the oscillator manufacturer's recommended capacitor (10 pF<CL<300pF) from each pin to ground (Figure 20).

Control Registers

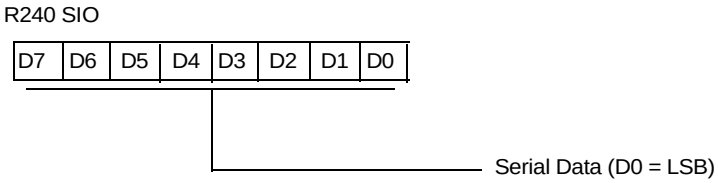

Figure 21. Serial I/O Register (F0h: Read/Write)

Caution: The majority of the control registers are read/write. The rest of the control are write only. The write-only registers are not readable. Attempting to read write-only registers will result in reading non-valid data. Any attempt to use logical or boolean types of instructions on these registers may corrupt the contents in the registers involved. Emulator operations on these write-only registers also reflect what is found on the Z8 device.

Prescaler 1 Register

The Prescaler 1 Register, PRE1, controls clocking functions and is shown in Figure 24.

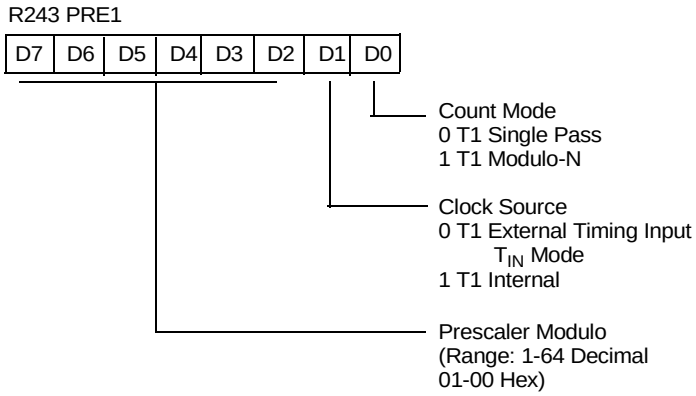

Figure 24. Prescaler 1 Register (F3h: Write Only)

Counter/Timer 0 Register

The Counter/Timer 0 Register, T0 is shown in Figure 25.

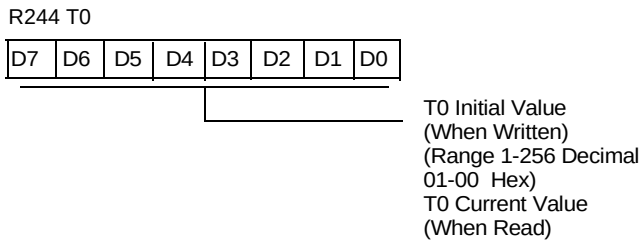

Figure 25. Counter/Timer 0 Register (F4h: Read/Write)

Prescaler 0 Register

The Prescaler 0 Register PRE0 controls clocking functions and is shown in Figure 26.

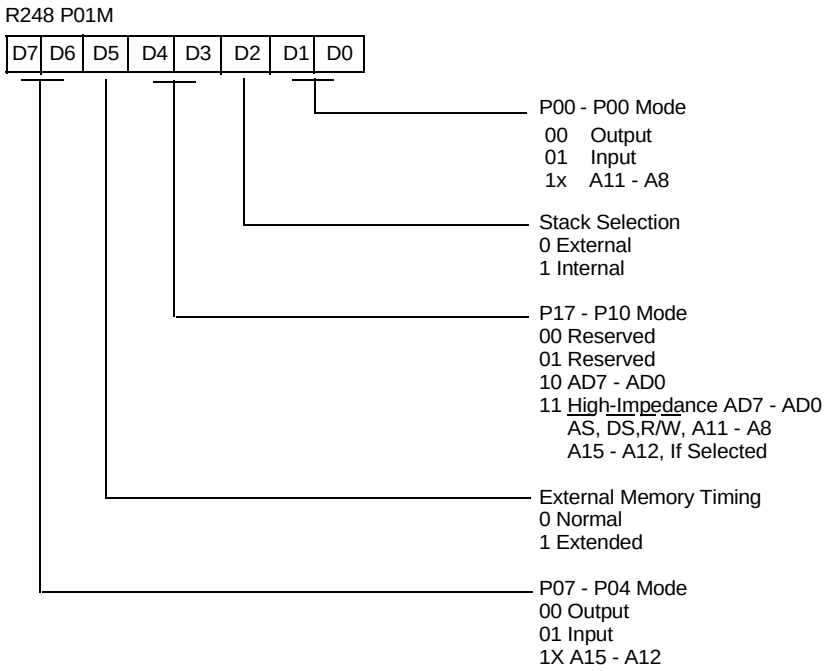

Figure 29. Port 0 and 1 Mode Register (F8h: Write Only)

Interrupt Priority Register. The Interrupt Priority Register, IPR, prioritizes interrupt functions and is shown in Figure 30.

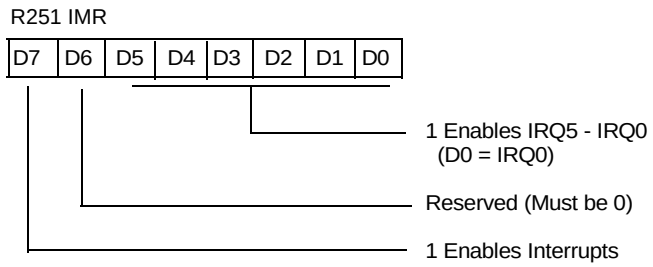

Figure 32. Interrupt Mask Register (FBh: Read/Write)

Flags Register

The CPU sets flags in the Flags Register, FLAGS, to allow the user to perform tests based on differing logical states. The FLAGS Register is shown in Figure 33 .

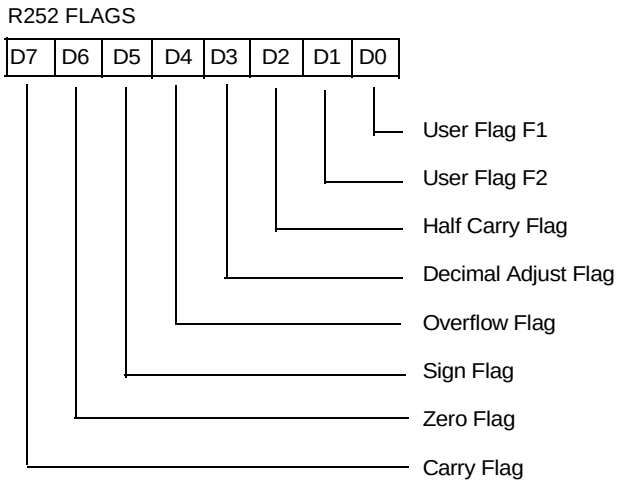

Figure 33. Flags Register (FCh: Read/Write)

Register Pointer Register

The Register Pointer Register, RP, controls pointer functions in the working registers and is shown in Figure 34.

Table 17. DC Electrical Characteristics at Standard and External Temperatures (Continued)

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical[2]		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@25°C**	**Units**	**Conditions**
V_{CL}	Clock Input Low Voltage	-0.3	0.8	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = -2.0 mA
V_{OH}	Output High Voltage	V_{CC}–100mV		V_{CC}–100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OH} = +2 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8	-0.3	0.8		V	
I_{IL}	Input Leakage	–2	2	-2	2		µA	Test at 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	-2	2		µA	Test at 0 V, V_{CC}
I_{IR}	Reset Input Current		–80		-80		µA	V_{RL}=0V
I_{CC}	Supply Current		35		35	24	mA	@ 16 MHz([1])
I_{CC1}	Standby Current		7		7	4.5	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		10	1	µA	STOP Mode V_{IN} = 0 V, V_{CC} ([1])
I_{ALL}	Autolatch Low Current	-10	10	-14	14		µA	

Note:
1. All inputs driven to 0V, V_{CC} and outputs floating.
2. V_{CC} = 5.0V

AC Electrical Characteristics

Figure 38 illustrates the timing characteristics of the Z86C91MCU with respect to external input/output sources. See Table 18 for descriptions of the numbered timing parameters in the figure.

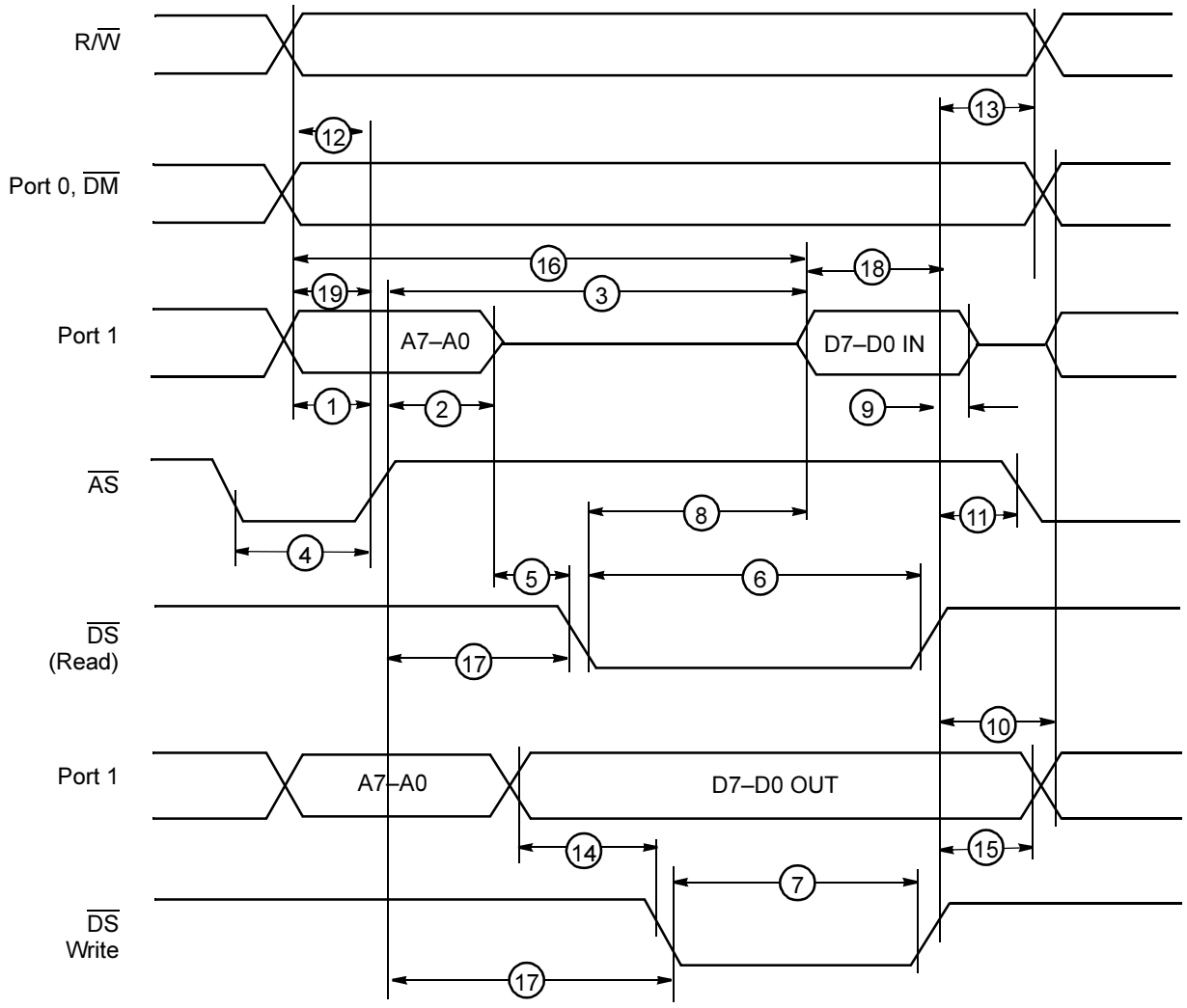

Figure 38. External I/O or Memory READ and WRITE Timing

Table 19. Clock Dependent Formulas

Number	Symbol	Equation
1	T_DA(AS)	0.40 TpC + 0.32
2	T_DAS(A)	0.59 TpC - 3.25
3	T_DAS(DR)	2.38 TpC + 6.14
4	T_WAS	0.66 TpC -1.65
6	T_WDSR	2.33TpC - 10.56
7	T_WDSW	1.27 TpC + 1.67
8	T_DDSR(DR)	1.97 TpC - 42.5
10	T_DDS(A)	0.8 TpC
11	T_DDS(AS)	0.59 TpC - 3.14
12	T_DR$\overline{W}$(AS)	0.4 TpC
13	T_DDS(R$\overline{W}$)	0.8 TpC - 15
14	T_DDW(DSW)	0.4 TpC
15	T_DDS(DW)	0.88 TpC - 19
16	T_DA(DR)	4 TpC - 20
17	T_DAS(DS)	0.91 TpC - 10.7
18	T_SDI(DS)	0.8 TpC - 10
19	T_DDM(AS)	0.9 TpC - 26.3

Additional Timing

Figure 39 illustrates the timing characteristics of the Z86C91 MCU with respect to system clock functions. See Table 20 for descriptions of the numbered timing parameters in the figure.

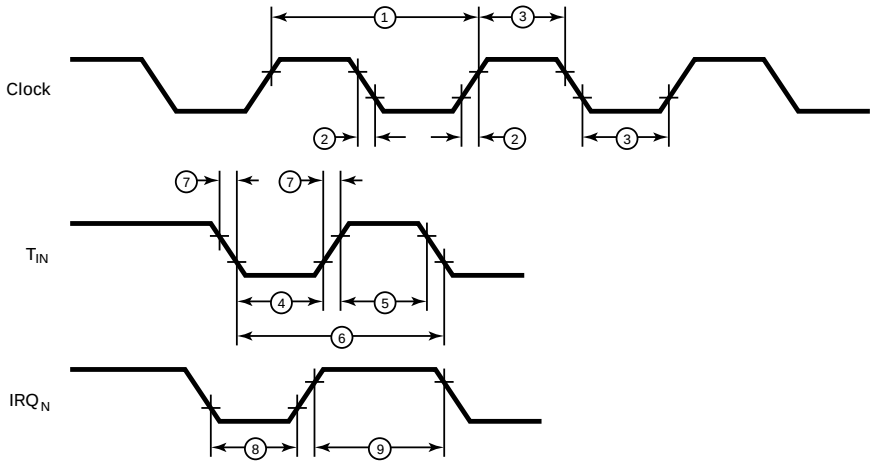

Figure 39. Additional Timing

Table 20. Additional Timing (Standard and Extended Temperature)

			T_A = 0ºC to +70ºC 16 MHz		T_A =-4 0ºC to +105ºC 16 MHz			
No	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	T_PC	Input Clock Period	62.5	1000	62.5	1000	ns	1
2	T_RC,T_FC	Clock Input Rise & Fall Times		10		10	ns	1
3	T_WC	Input Clock Width	25		25		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	75		75		ns	2
5	$T_WT_{IN}H$	Timer Input High Width	$3T_PC$		$3T_PC$			2

Notes:
1. Clock timing references use 3.8V for a logic one and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request via Port 3.
4. The interrupt request via Port 3 (P31–P33).
5. The interrupt request via Port 3 (P30).