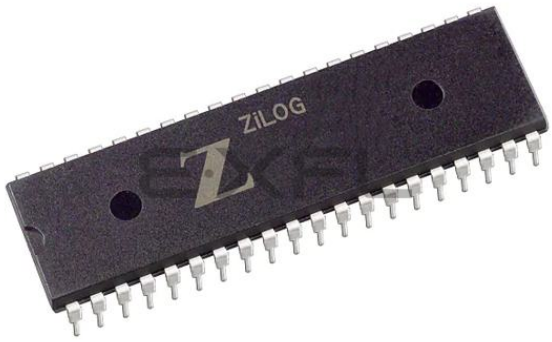

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9116psg

List of Figures

List of Tables

- Six Vectored, Prioritized Interrupts from Eight Different Sources
- Two Programmable 8-Bit Counter/Timers, each with two 6-Bit Programmable Prescalers
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock
- Two Standby Modes: STOP and HALT
- Auto Latches

Table 15. Port 3 Pin Assignments

Pin	I/O	Control Timer	Interrupt	P0 HS	P2 HS	Ext	UART
P30	IN		IRQ3				Serial In
P31	IN	T_{IN}	IRQ2		D/R		
P32	IN		IRQ0	D/R			
P33	IN		IRQ1				
P34	OUT					$\overline{DM}$	
P35	OUT			R/D			
P36	OUT	T_{OUT}			R/D		
P37	OUT						Serial Out

Notes:
HS = Handshake Signals
D = $\overline{DAV}$ (Data Available)
R = RDY (Ready)

Autolatch. The autolatch places valid CMOS levels on all inputs that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Autolatches are available on Port 0, Port 1, Port 2, and P3 inputs.

$\overline{RESET}$ (input, Low). Initializes the MCU. RESET occurs through external reset only. During Power-On Reset, the externally-generated reset drives the $\overline{RESET}$ pin Low for the POR time. Pull-up is provided internally.

Caution: $\overline{RESET}$ depends on oscillator operation to achieve full reset conditions.

$\overline{RESET}$ is a Schmitt-triggered input. During the RESET cycle, $\overline{DS}$ is held active Low while $\overline{AS}$ cycles at a rate of $T_PC \div 2$. Program execution begins at location `000Ch`, after the $\overline{RESET}$ is released.

When program execution begins, $\overline{AS}$ and $\overline{DS}$ toggles only for external memory accesses. The Z8 can only exit Stop Mode by using the $\overline{RESET}$ pin.The Z8 does reset all registers on a Stop-Mode Recovery operation out of STOP mode.

Functional Description

The Z8 MCU incorporates the following functions that enhance the standard Z8® architecture and provide the user with increased design flexibility:

- Reset
- Program Memory
- Data Memory
- Working Register
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- HALT and STOP Modes
- Port Configuration Register

RESET. The device is reset in the following condition:

- External Reset

Automatic Power-On Reset circuitry is not built into this Z8. This Z8 requires an external reset circuit to reset upon power-up. The internal pull-up resistor is on the $\overline{\text{RESET}}$ pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a low-value pull-up resistor be used.

Program Memory. The Z86C91 can address up to 64 KB of external program memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location `000Ch` after reset. See Figure 13.

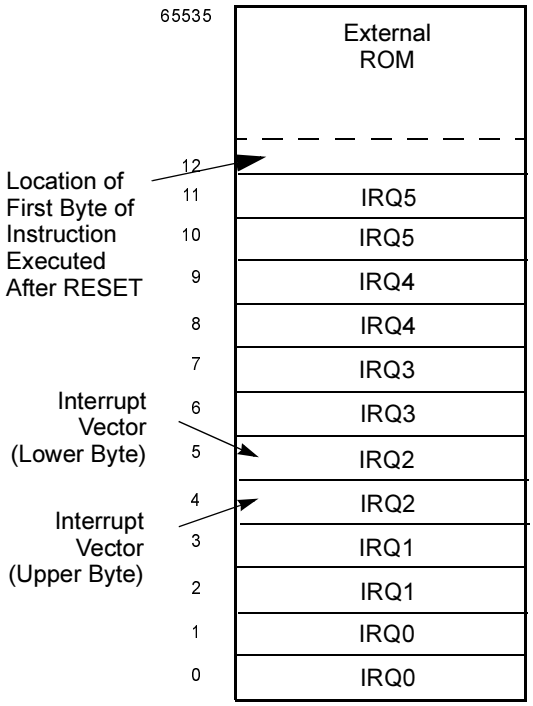


Figure 13. Program Memory Map

Data Memory ($\overline{DM}$). The Z86C91addresses up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that is programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode.

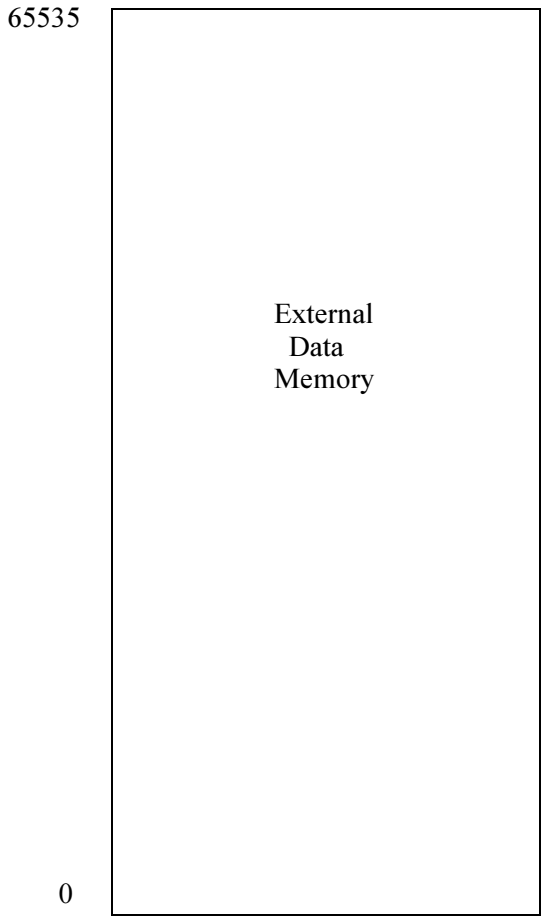


Figure 14. Data Memory Map

Register File. The register file contains three I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Stack Pointer (Bits 15-8)	SPH
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240	Serial I/O	SIO
239	General Purpose Registers	
4		
3	Port 3	P3
2	Port 2	P2
1	Reserved	Reserved
0	Port 0	P0

Figure 15. Register File

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

Interrupts. The Z8 has six different interrupts from eight different sources. These interrupts are maskable and prioritized. The 8 sources are divided as follows: 4 sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and 2 are claimed by counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register

All interrupts are vectored through locations in Program Memory. When an interrupt request is granted, the interrupt machine cycle is activated. This resets the interrupt request flag and disables all of the subsequent interrupts, except Program Counter and Status Flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16 bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Nested interrupts are supported by enabling interrupts in the interrupt service routine.

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48TpC (external XTAL clock cycles) are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

Control Registers

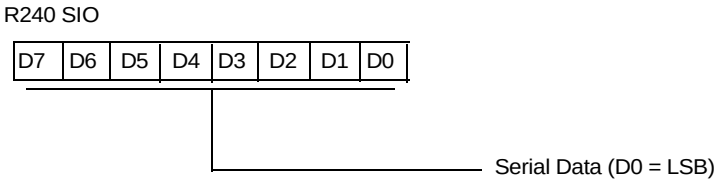


Figure 21. Serial I/O Register (F0h: Read/Write)

Caution: The majority of the control registers are read/write. The rest of the control are write only. The write-only registers are not readable. Attempting to read write-only registers will result in reading non-valid data. Any attempt to use logical or boolean types of instructions on these registers may corrupt the contents in the registers involved. Emulator operations on these write-only registers also reflect what is found on the Z8 device.

Prescaler 1 Register

The Prescaler 1 Register, PRE1, controls clocking functions and is shown in Figure 24.

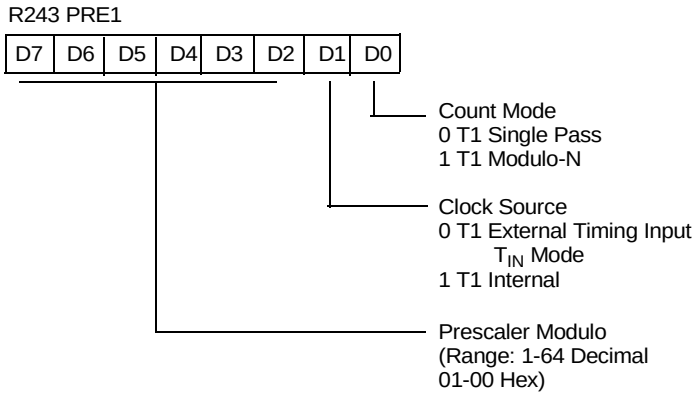


Figure 24. Prescaler 1 Register (F3h: Write Only)

Counter/Timer 0 Register

The Counter/Timer 0 Register, T0 is shown in Figure 25.

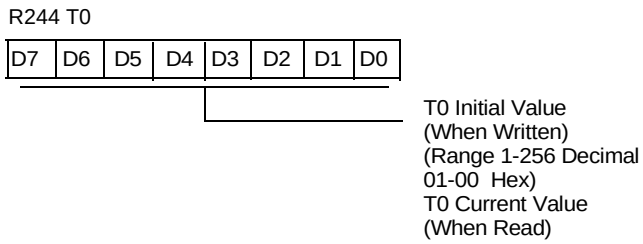


Figure 25. Counter/Timer 0 Register (F4h: Read/Write)

Prescaler 0 Register

The Prescaler 0 Register PRE0 controls clocking functions and is shown in Figure 26.

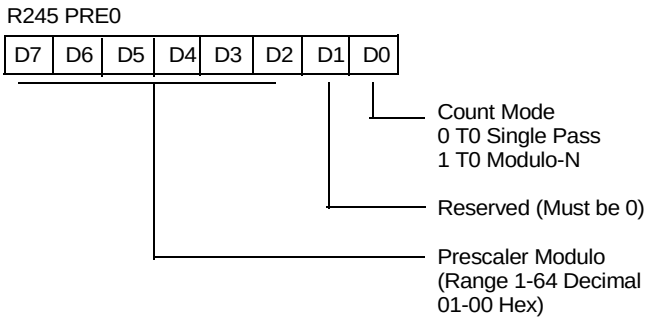


Figure 26. Prescaler 0 Register (F5h: Write Only)

Port 2 Mode Register

The Port 2 Mode Register, P2M, controls Port 2 I/O functions and is shown in Figure 27.

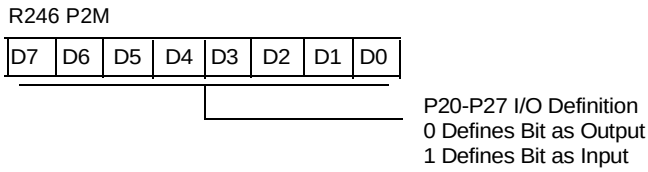


Figure 27. Port 2 Mode Register (F6h: Write Only)

Port 3 Mode Register

The Port 3 Mode Register P3M controls Port 3 I/O functions and is shown in Figure 28.

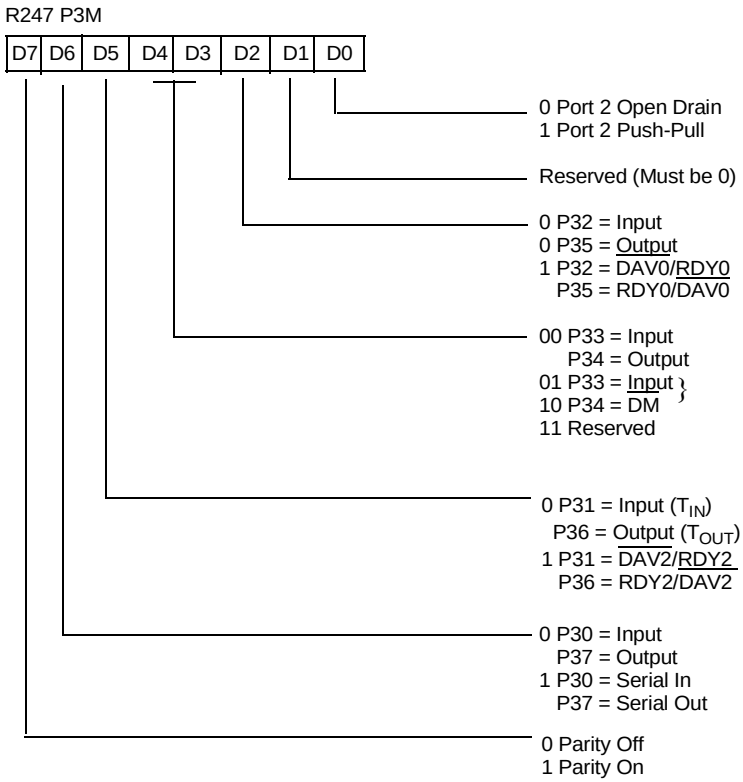


Figure 28. Port 3 Mode Register (F7h: Write Only)

Ports 0 and 1 Mode Register

The Ports 0 and 1 Mode Register, P01M, controls port and timing functions for Ports 0 and 1 and is shown in Figure 29.

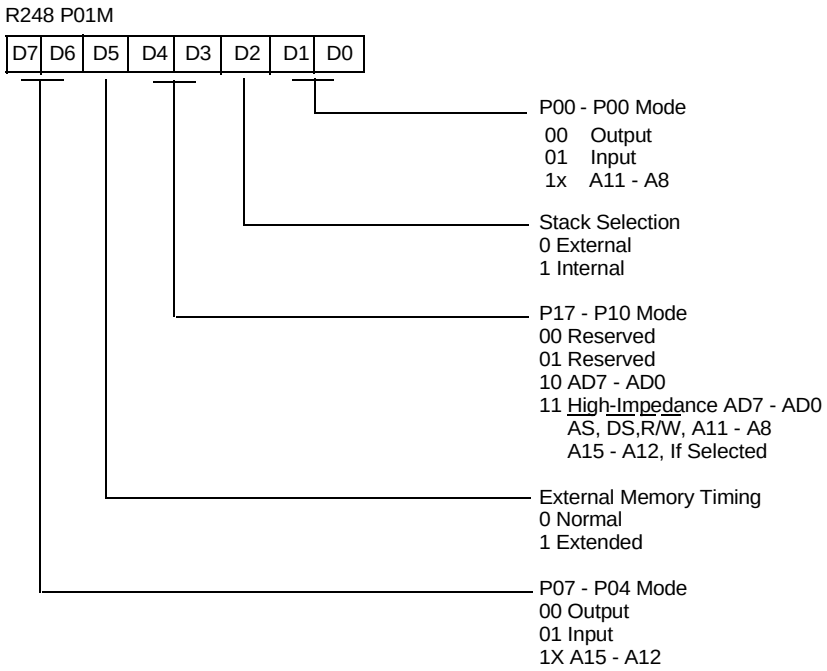


Figure 29. Port 0 and 1 Mode Register (F8h: Write Only)

Interrupt Priority Register. The Interrupt Priority Register, IPR, prioritizes interrupt functions and is shown in Figure 30.

AC Electrical Characteristics

Figure 38 illustrates the timing characteristics of the Z86C91MCU with respect to external input/output sources. See Table 18 for descriptions of the numbered timing parameters in the figure.

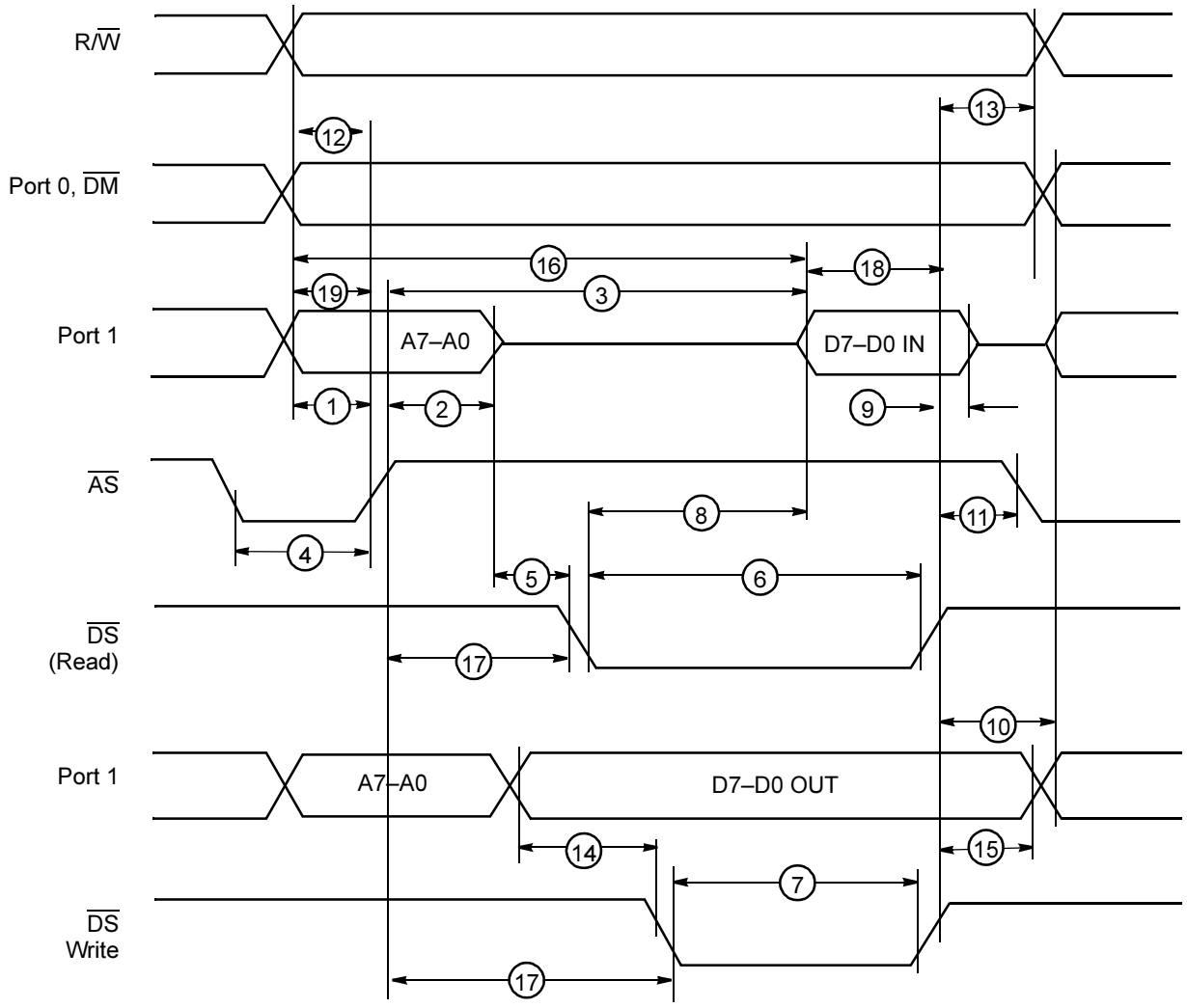


Figure 38. External I/O or Memory READ and WRITE Timing

Table 19. Clock Dependent Formulas

Number	Symbol	Equation
1	T_DA(AS)	0.40 TpC + 0.32
2	T_DAS(A)	0.59 TpC - 3.25
3	T_DAS(DR)	2.38 TpC + 6.14
4	T_WAS	0.66 TpC -1.65
6	T_WDSR	2.33TpC - 10.56
7	T_WDSW	1.27 TpC + 1.67
8	T_DDSR(DR)	1.97 TpC - 42.5
10	T_DDS(A)	0.8 TpC
11	T_DDS(AS)	0.59 TpC - 3.14
12	T_DR$\overline{W}$(AS)	0.4 TpC
13	T_DDS(R$\overline{W}$)	0.8 TpC - 15
14	T_DDW(DSW)	0.4 TpC
15	T_DDS(DW)	0.88 TpC - 19
16	T_DA(DR)	4 TpC - 20
17	T_DAS(DS)	0.91 TpC - 10.7
18	T_SDI(DS)	0.8 TpC - 10
19	T_DDM(AS)	0.9 TpC - 26.3

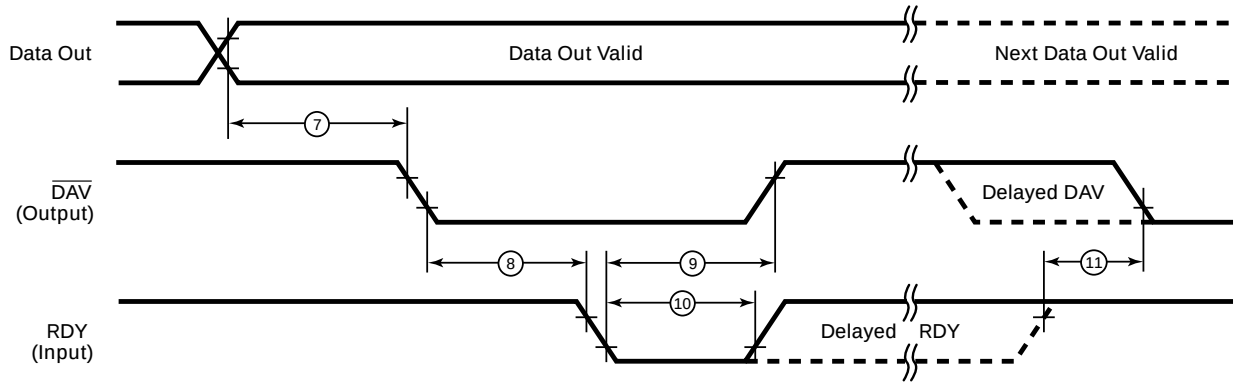
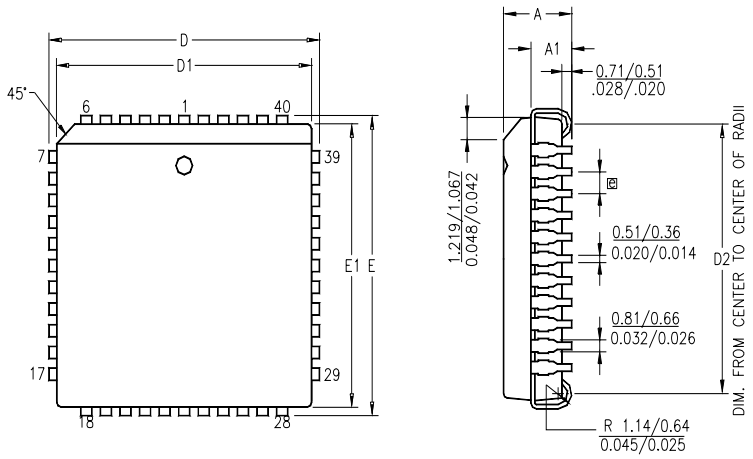


Figure 41. Output Handshake Timing

Table 21. Handshake Timing (Standard and Extended Temperatures)

No	Symbol	Parameter	T_A = 0ºC to +70ºC Min	T_A = 0ºC to +70ºC Max	T_A = -40ºC to +105ºC Min	T_A = -40ºC to +105ºC Max	Data Direction
1	T_SDI(DAV)	Data In Setup Time	0		0		Input
2	T_HDI(RDY)	Data In Hold Time	145		145		Input
3	T_WDAV	Data Available Width	110		110		Input
4	T_DDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	Input
5	T_DDAVId(RDY)	DAV Out to DAV Fall Delay		115		115	Input
6	RDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	0		0		Input
7	T_DD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	Output
8	T_DDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		Output
9	T_DRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	Output
10	T_WRDY	RDY Width	110		110		Output
11	T_DRDY0$_D$(DAV)	RDY Rise to DAV Fall Delay		115		115	Output

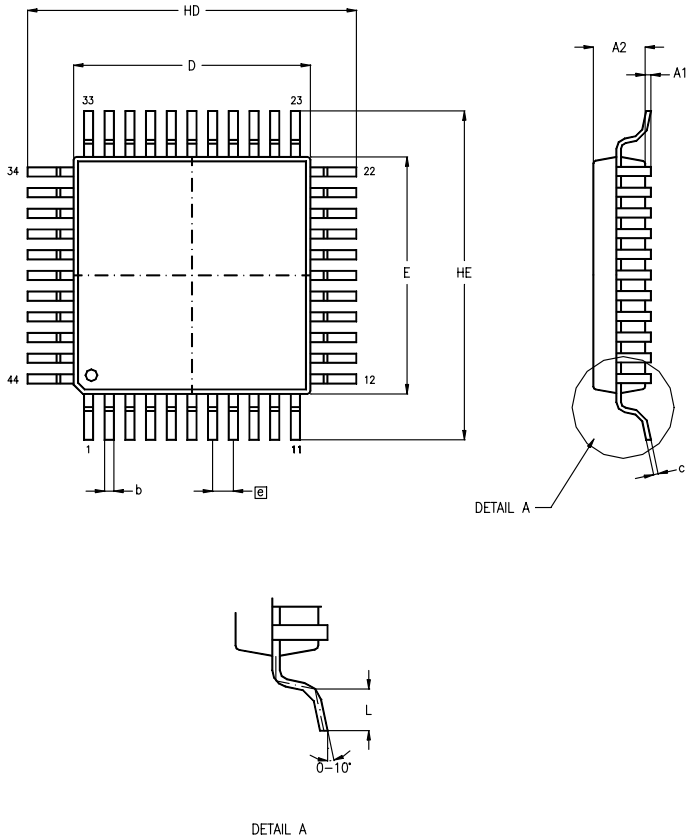
Note: All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
   INCH

Figure 43. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 44. 44-Pin PQFP Package Diagram

Ordering Information

Table 22. Ordering Information

Pin Count	Package	Order Number
40	DIP	Z86C9116PSC
40	DIP	Z86C9116PEC
44	PLCC	Z86C9116VSC
44	PLCC	Z86C9116VEC
44	QFP	Z86C9116FEC
44	QFP	Z86C9116FSC

Part Number Description

ZiLOG part numbers consist of a number of components. For example, part number Z86C9116PSC is a 16-MHz 40-pin DIP that operates in the –0ºC to +70ºC temperature range, with Plastic Standard Flow. The Z86C9116PSC part number corresponds to the code segments indicated in the following table.

Z	ZiLOG Prefix
86	Z8 Product
C	OTP Product
91	Product Number
16	Speed (MHz)
P	Package
S	Temperature
C	Environmental Flow

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

ZiLOG, Inc.
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Telephone (408) 558-8500
FAX 408 558-8300
Internet: www.ZiLOG.com