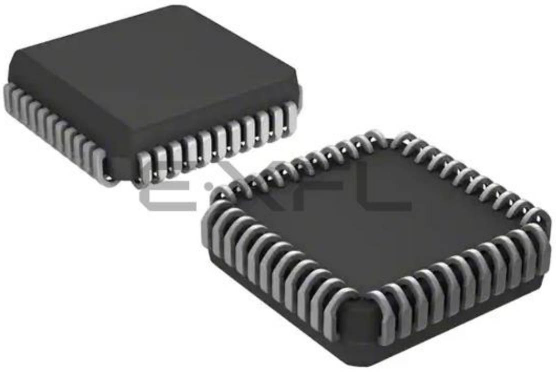

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9116vec00tr

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Table of Contents

- Six Vectored, Prioritized Interrupts from Eight Different Sources
- Two Programmable 8-Bit Counter/Timers, each with two 6-Bit Programmable Prescalers
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock
- Two Standby Modes: STOP and HALT
- Auto Latches

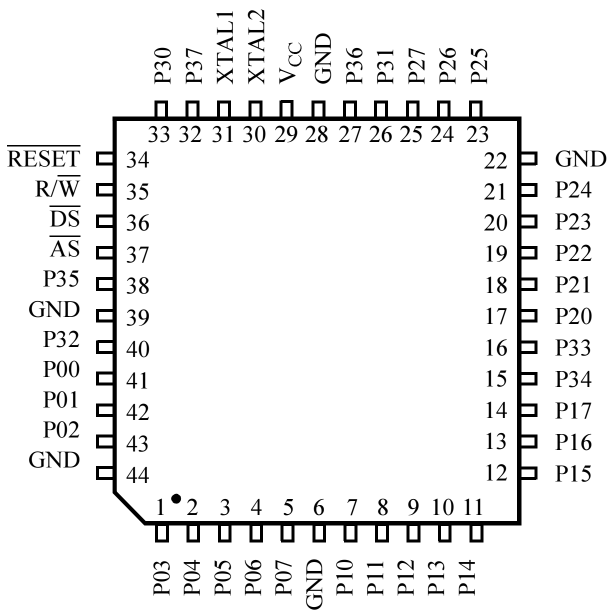


Figure 3. 44-Pin PQFP Pin Configuration

Table 13. 44-Pin PQFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0, Bits 3-7	Input/Output
6	GND	Ground	Output
7-14	P10-P17	Port 1, Bits 0-7	Input/Output
15	P34	Port 3, Bit 4	Output
16	P33	Port 3, Bit 3	Intput
17-21	P20-P24	Port 2, Bits 0-4	Input/Output
22	GND	Ground	Output
23-25	P25-P27	Port 2, Bits 5-7	Input/Output
26	P31	Port 3, Bit 1	Input
27	P36	Port 3, Bit 6	Output
28	GND	Ground	Output

Port 3 (P37–P30). Port 3 is an 8-bit, TTL-compatible port, with four fixed inputs (P33–P30) and four fixed outputs (P34–P37). Port 3 is configured under software control for Input/Output, Counter/Timers, interrupt, UART, port handshake, and data Memory functions. Port 3, when used as serial I/O are programmed as serial in and serial out respectively (Figure 8).

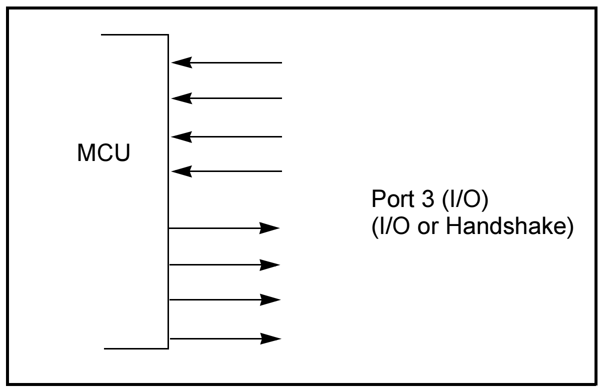


Figure 8. Port 3 Configuration

For interrupt functions, Port 3 inputs are falling-edge interrupt inputs. Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 ($\overline{DAV}$ and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}); Data Memory Select.

P34 output is software-programmed to function as a Data Memory Select ($\overline{DM}$). The Port 3 Mode Register (P3M) bit D3,D4 selects this function. When accessing external data memory, P34 goes active Low; when accessing external program memory, P34 goes High.

An onboard UART is enabled by software setting bit D5 of the Port 3 Mode Register P3M. When enabled, P30 is the receive input and P37 is the transmit output.

Port 3, lines P30 and P37 are programmed as serial I/O for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer0.

The Z8 automatically adds a start bit and two stop bits to transmitted data. Serial Data formats are shown in Figure 9 and Figure 10. Odd parity is also available by setting bit D7 in the P3M register. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

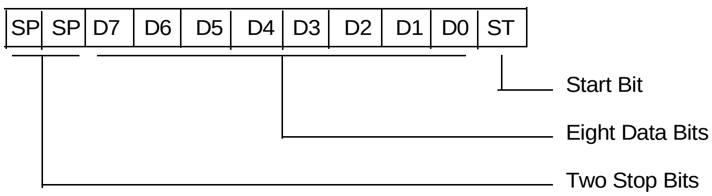


Figure 9. Transmitted Data (No Parity)

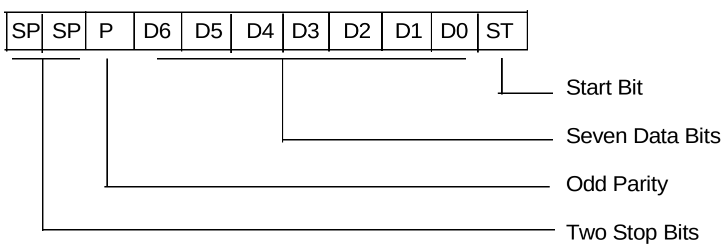


Figure 10. Transmitted Data (With Parity)

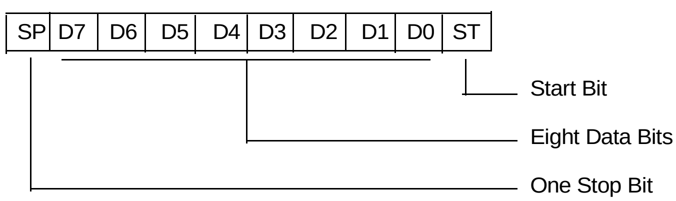


Figure 11. Received Data (No Parity)

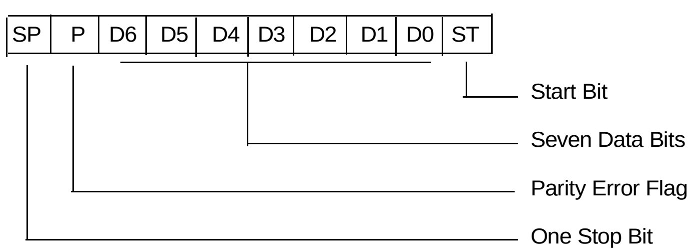


Figure 12. Received Data (With Parity)

Functional Description

The Z8 MCU incorporates the following functions that enhance the standard Z8® architecture and provide the user with increased design flexibility:

- Reset
- Program Memory
- Data Memory
- Working Register
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- HALT and STOP Modes
- Port Configuration Register

$\overline{\text{RESET}}$. The device is reset in the following condition:

- External Reset

Automatic Power-On Reset circuitry is not built into this Z8. This Z8 requires an external reset circuit to reset upon power-up. The internal pull-up resistor is on the $\overline{\text{RESET}}$ pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a low-value pull-up resistor be used.

Program Memory. The Z86C91 can address up to 64 KB of external program memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location `000Ch` after reset. See Figure 13.

General-Purpose Registers (GPR). General-purpose registers are undefined after the device is powered up. These registers keep the most recent value after any RESET, as long as the RESET occurs in the V_{CC} voltage-specified operating range. General-purpose registers are not guaranteed to keep their most recent state from if V_{CC} drops below the minimum V_{CC} operating range.

Stack Pointer. The Z86C91 has a 16-bit Stack Pointer (SPH and SPL) used for the external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (SPL) is used for the internal stack that resides within the 236 general-purpose registers. Stack Pointer High (SPH) is used as a general-purpose register only when using an internal stack.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 17).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both the counter and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to START, STOP, restart to CONTINUE, or restart from the initial value. The counters can also be programmed to STOP upon reaching 1 (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO–N CONTINUOUS mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. Reading the prescalers returns the value `FFh`. The clock source for T1 is user-definable and is either the internal micro controller clock divide-by-four, or an external signal input through Port 3. The maximum frequency of the external timer signal is the XTAL clock signal divided by 8. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or nonretriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as an output (T_{OUT}) through which T0, T1, or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

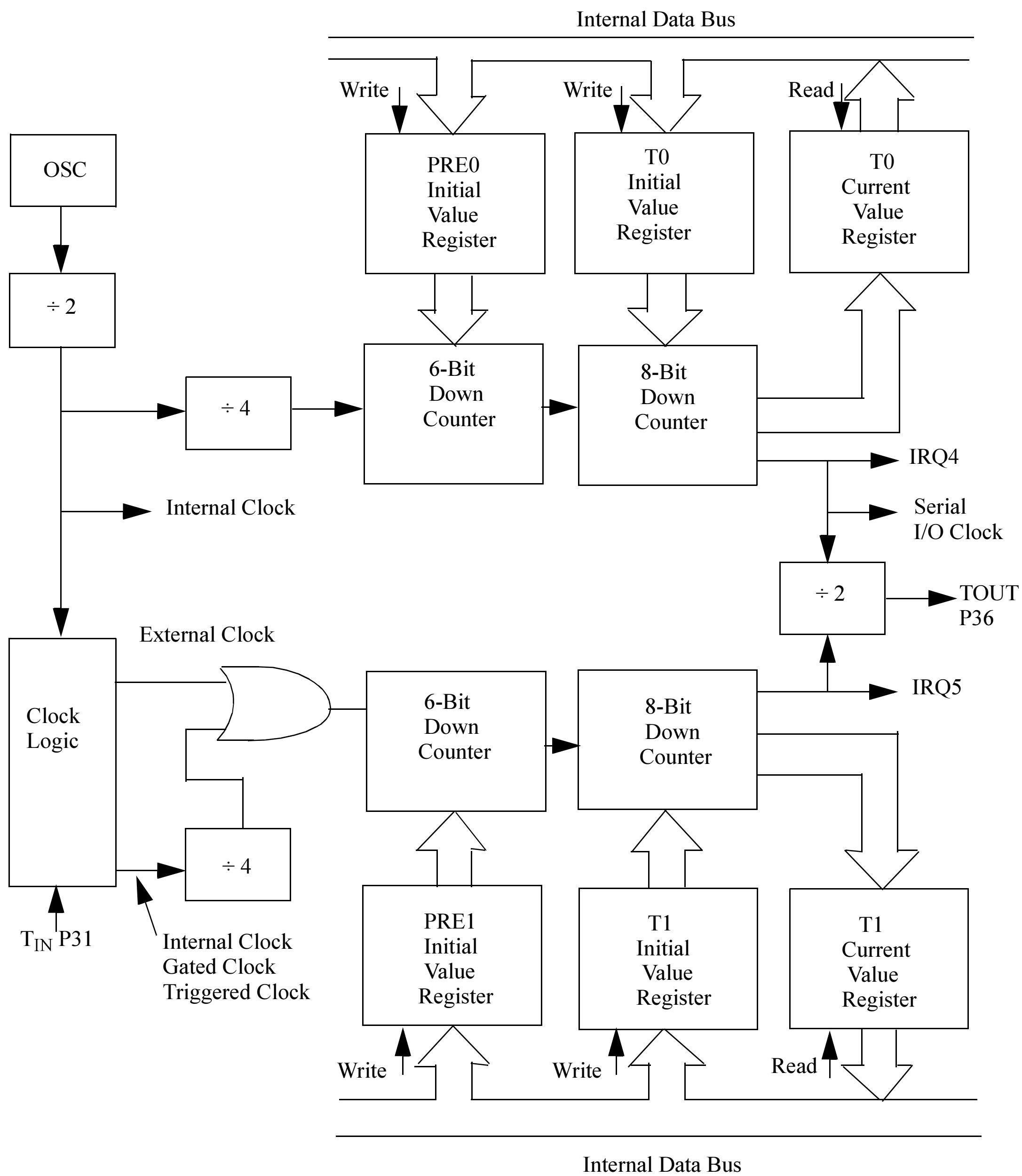


Figure 18. Counter/Timer Block Diagram

Control Registers

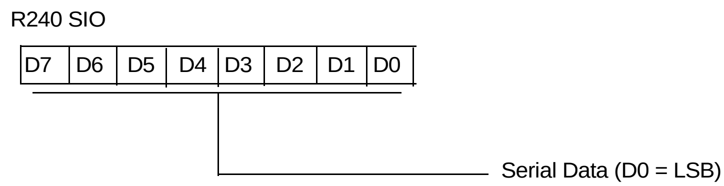


Figure 21. Serial I/O Register (F0h: Read/Write)

Caution: The majority of the control registers are read/write. The rest of the control are write only. The write-only registers are not readable. Attempting to read write-only registers will result in reading non-valid data. Any attempt to use logical or boolean types of instructions on these registers may corrupt the contents in the registers involved. Emulator operations on these write-only registers also reflect what is found on the Z8 device.

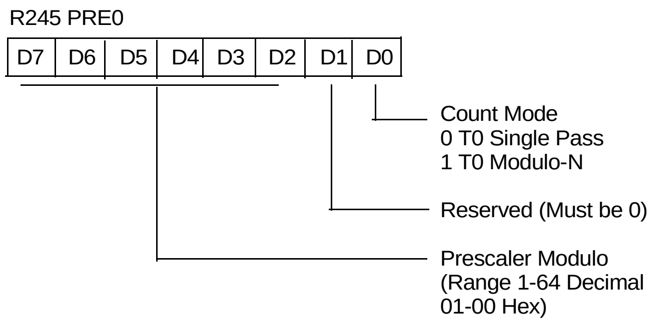


Figure 26. Prescaler 0 Register (F5h: Write Only)

Port 2 Mode Register

The Port 2 Mode Register, P2M, controls Port 2 I/O functions and is shown in Figure 27.

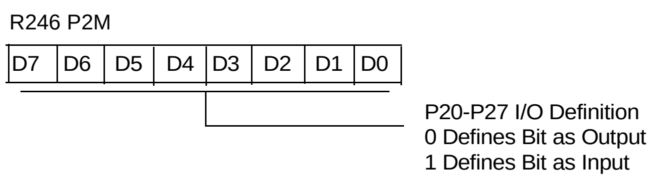


Figure 27. Port 2 Mode Register (F6h: Write Only)

Port 3 Mode Register

The Port 3 Mode Register P3M controls Port 3 I/O functions and is shown in Figure 28.

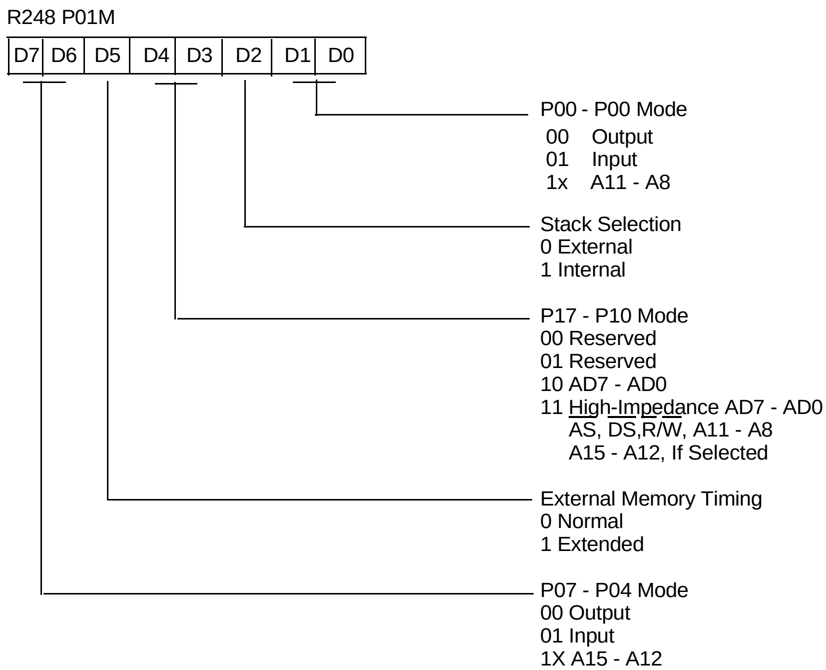


Figure 29. Port 0 and 1 Mode Register (F8h: Write Only)

Interrupt Priority Register. The Interrupt Priority Register, IPR, prioritizes interrupt functions and is shown in Figure 30.

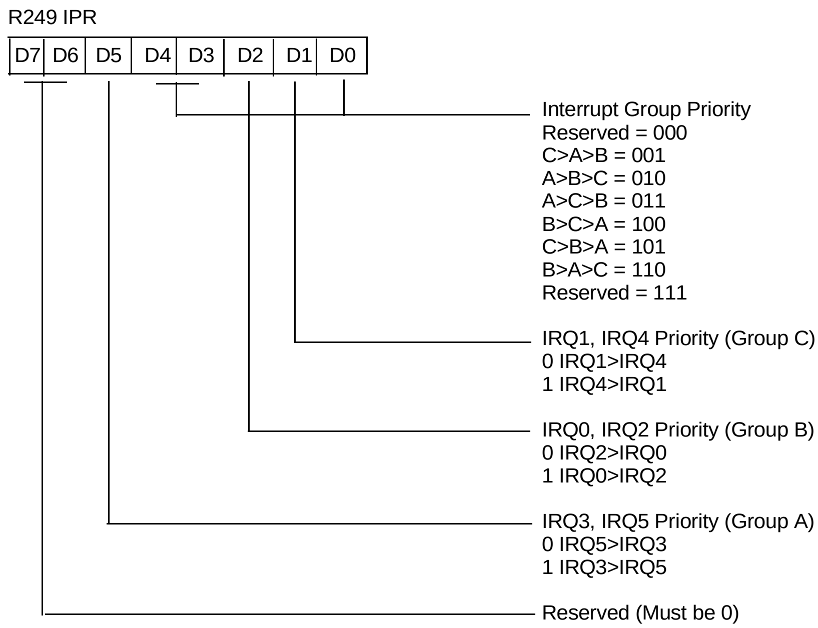


Figure 30. Interrupt Priority Register (F9h: Write Only)

Interrupt Request Register

The Interrupt Request Register, IRQ, controls interrupt functions and is shown in Figure 31.

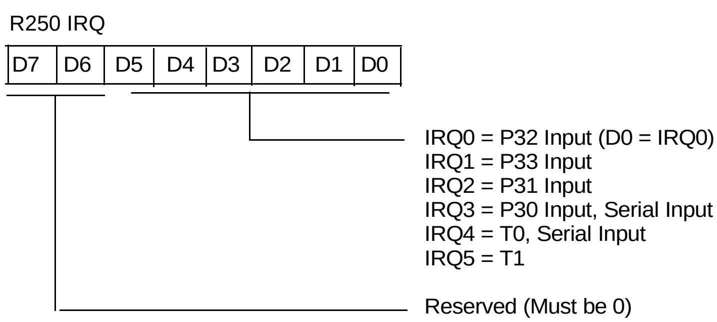


Figure 31. Interrupt Request Register (FAh: Read/Write)

Interrupt Mask Register

The Interrupt Mask Register, IMR, controls interrupt functions and is shown in Figure 32.

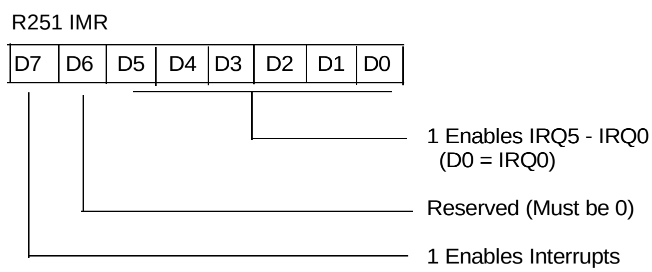


Figure 32. Interrupt Mask Register (FBh: Read/Write)

Flags Register

The CPU sets flags in the Flags Register, FLAGS, to allow the user to perform tests based on differing logical states. The FLAGS Register is shown in Figure 33 .

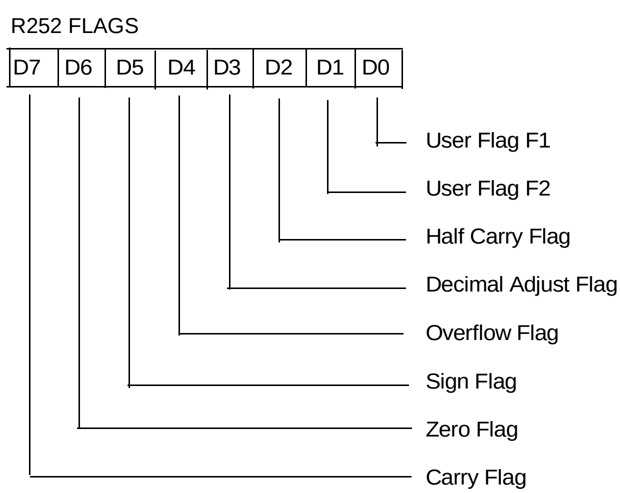


Figure 33. Flags Register (FCh: Read/Write)

Register Pointer Register

The Register Pointer Register, RP, controls pointer functions in the working registers and is shown in Figure 34.

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than the Absolute Maximum Ratings listed in Table 16 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STO}	Storage Temperature	–65	+150	C
T_A	Operating Ambient Temperature		[2]	C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 37).

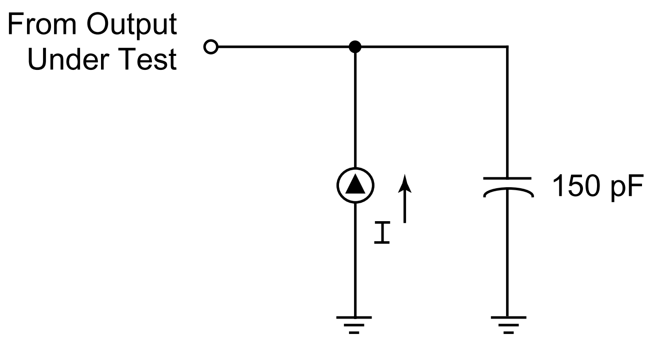


Figure 37. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC Electrical Characteristics

Table 17. DC Electrical Characteristics at Standard and External Temperatures

		T_A = 0°C to +70°C		T_A = -40°C to +105°C				
Sym	Parameter	Min	Max	Min	Max	Typical[2] @25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IH} <200µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	Driven by External Clock Generator

Note:
1. All inputs driven to 0V, V_{CC} and outputs floating.
2. V_{CC} = 5.0V

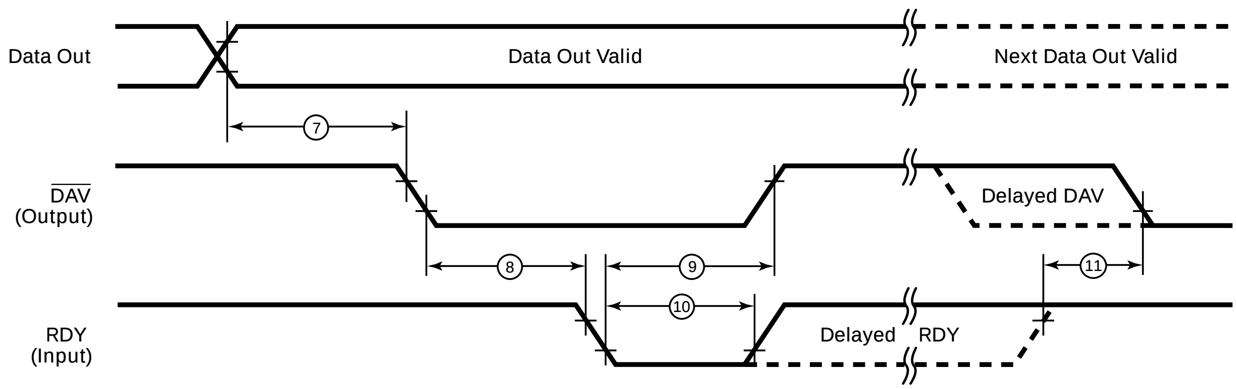


Figure 41. Output Handshake Timing

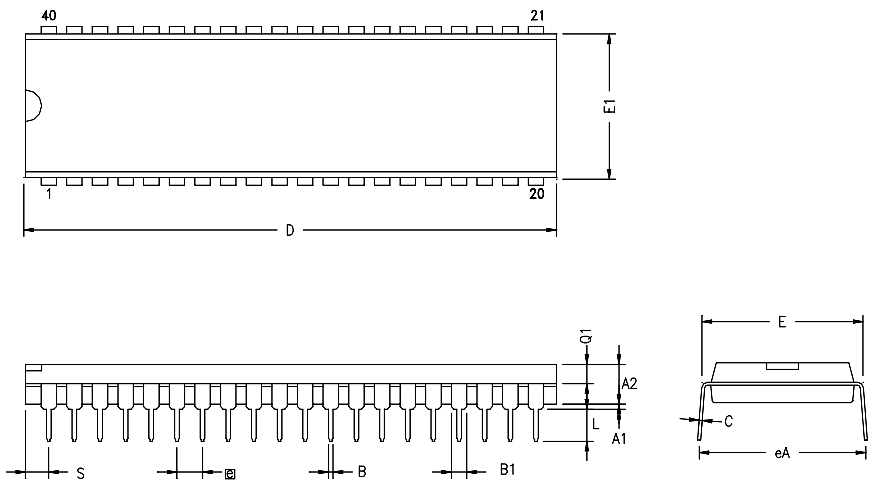
Table 21. Handshake Timing (Standard and Extended Temperatures)

No	Symbol	Parameter	T_A = 0ºC to +70ºC Min	Max	T_A = -40ºC to +105ºC Min	Max	Data Direction
1	T_SDI(DAV)	Data In Setup Time	0		0		Input
2	T_HDI(RDY)	Data In Hold Time	145		145		Input
3	T_WDAV	Data Available Width	110		110		Input
4	T_DDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	Input
5	T_DDAVId(RDY)	DAV Out to DAV Fall Delay		115		115	Input
6	RDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	0		0		Input
7	T_DD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	Output
8	T_DDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		Output
9	T_DRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	Output
10	T_WRDY	RDY Width	110		110		Output
11	T_DRDY0$_D$(DAV)	RDY Rise to DAV Fall Delay		115		115	Output

Note: All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Packaging

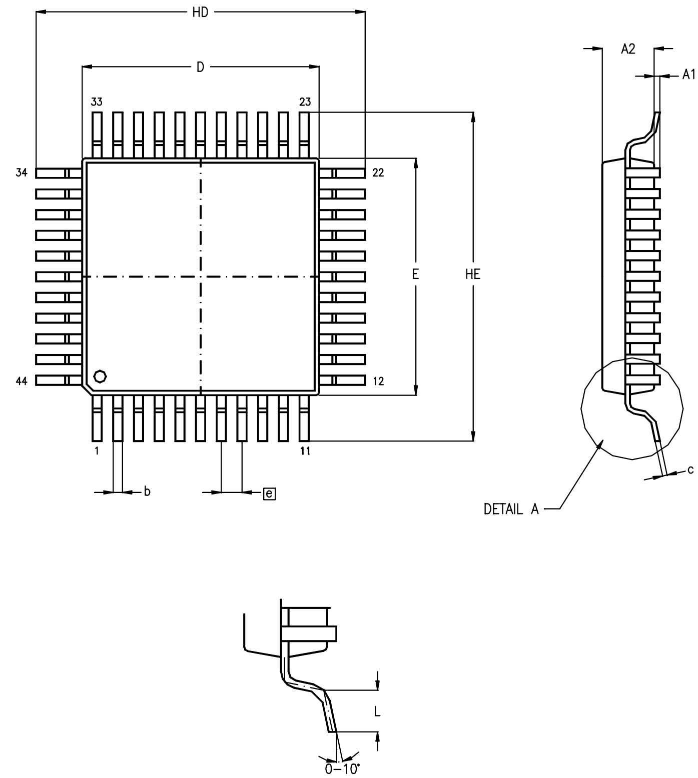
Figure 42 illustrates the 40-pin DIP package for the microcontroller devices.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 42. 40-Pin DIP Package Diagram



DETAIL A

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 44. 44-Pin PQFP Package Diagram

Document Information

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

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0185	Unique Document Number
01	Revision Number
0802	Month and Year Published