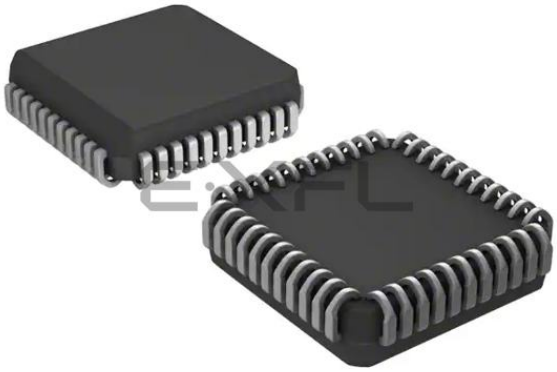

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Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
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- Six Vectored, Prioritized Interrupts from Eight Different Sources
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- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock
- Two Standby Modes: STOP and HALT
- Auto Latches

Functional Block Diagrams

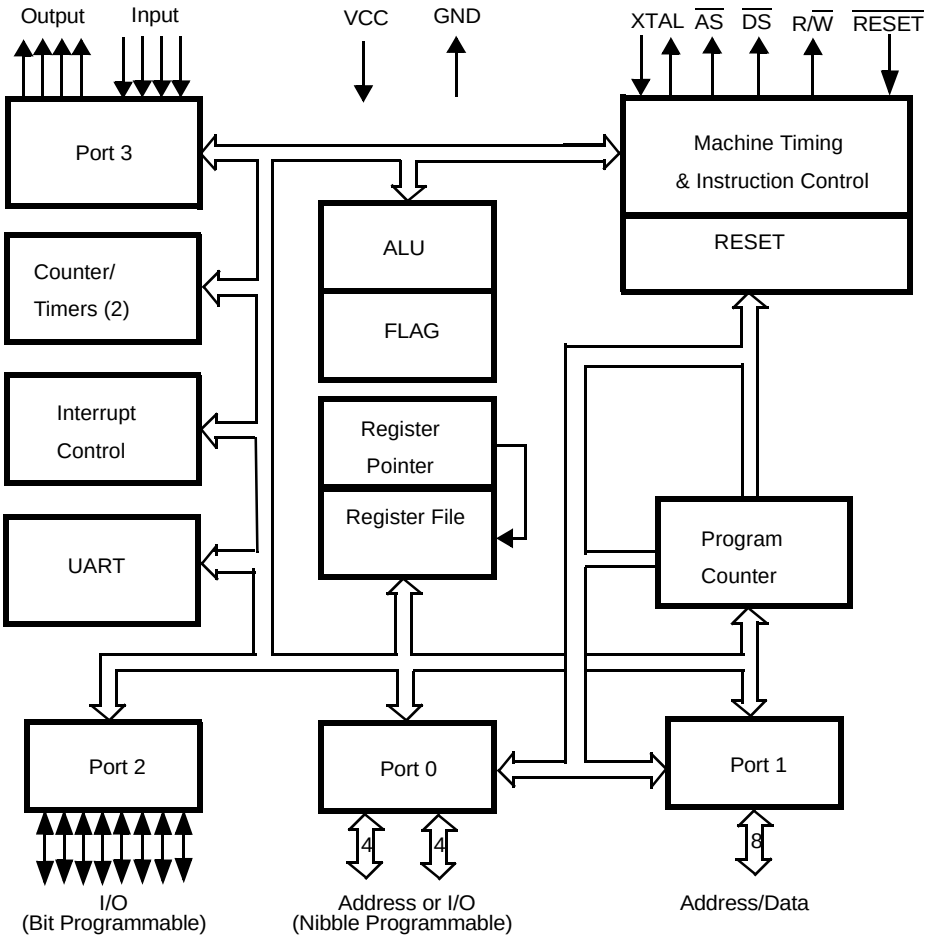


Figure 1. Z86C91 Functional Block Diagram

Pin Functions

The following paragraphs describe the function of each available Z86C91 pin.

$\overline{\text{DS}}$ (output, active Low). The Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). The Address Strobe is pulsed one time at the beginning of each machine cycle for external memory transfer. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and READ/WRITE.

XTAL1 (Crystal 1)Time-Based Oscillator Input. This pin connects a parallel-resonant crystal, ceramic resonator, LC network, or an external single-phase clock to the on-chip oscillatorand buffer.

XTAL2 (Crystal 2) Time-Based Oscillator Output. This pin connects a parallel-resonant crystal, ceramic resonant, LC network to the on-chip oscillator and buffer.

R/$\overline{\text{W}}$ (output, WRITE Low). The READ/WRITE signal is Low when the Z8 writes to external data memory.

$\overline{\text{RESET}}$ (input, Low). To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external XTAL clocks (4TpC). If the external $\overline{\text{RESET}}$ signal is less than 4TpC in duration, reset does not occur.

On the fifth clock after $\overline{\text{RESET}}$ is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external $\overline{\text{RESET}}$, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. When $\overline{\text{RESET}}$ is deactivated, program execution begins at location 000Ch. Power-Up reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P00–P07). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03–P00 input/output and P07–P04 input/output), or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control $\overline{\text{DAV0}}$ and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04–P07. The lower nibble must indicate the same direction as the upper nibble.

For external memory references, Port 1 provides address bits A7–A0 (lower nibble) and Port 0 provides address bits A15–A8 (upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 is programmed independently as I/O while the lower nibble is used for addressing. If one or

both nibbles are required for I/O operation, they are configured by writing to the Port 01 mode register (P01M).

After a hardware RESET, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode.

Port 0 can be placed in a high-impedance state along with Port 1, $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 5). A hardware RESET is required to exit this high-impedance state.

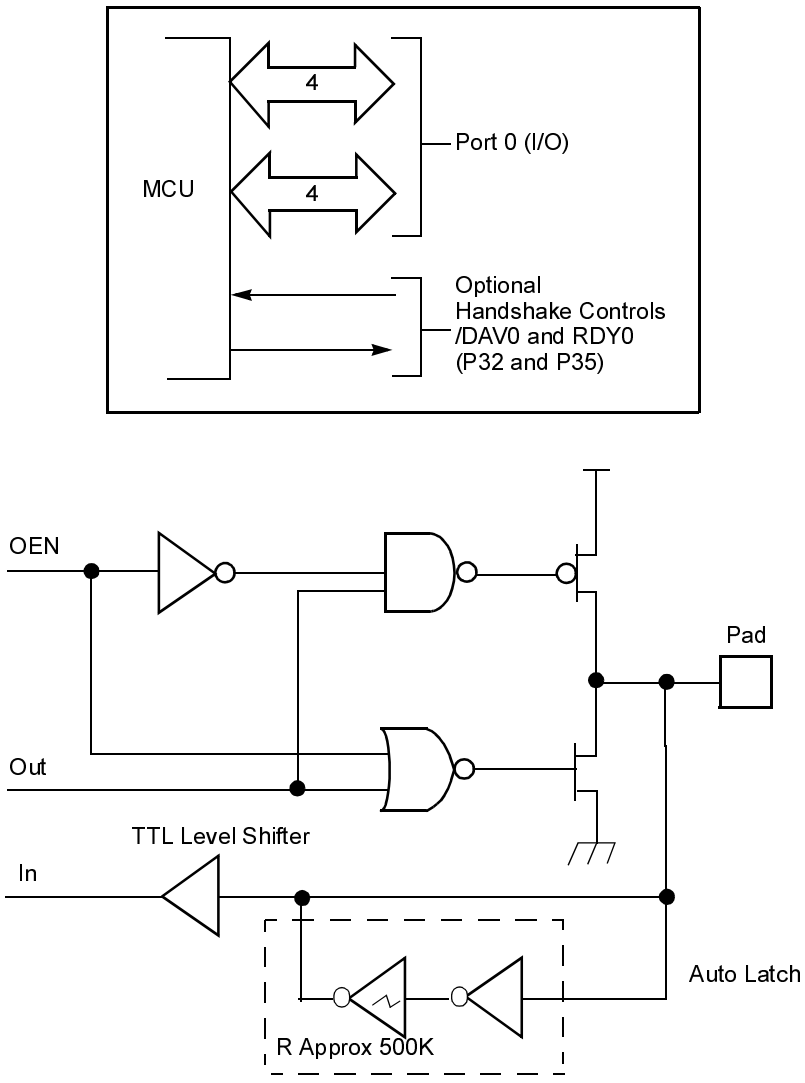


Figure 5. Port 0 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit programmable, bidirectional, TTL-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently or globally as an open-drain output. Port 2 is always available for I/O operation.When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines $\overline{\text{DAV2}}$ and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7). After a RESET, Port 2 is configured as an input port. The Port 2 output portion of the circuit has open-drain as it's default configuration.

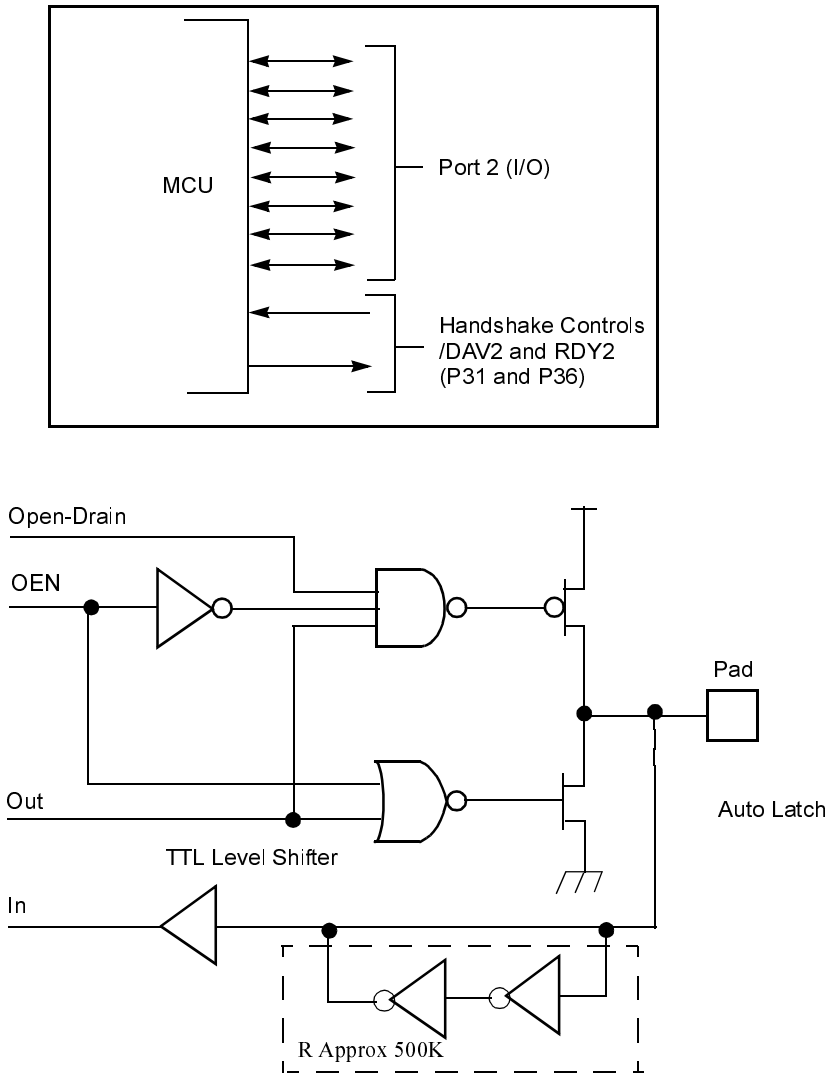


Figure 7. Port 2 Configuration

Table 15. Port 3 Pin Assignments

Pin	I/O	Control Timer	Interrupt	P0 HS	P2 HS	Ext	UART
P30	IN		IRQ3				Serial In
P31	IN	T_{IN}	IRQ2		D/R		
P32	IN		IRQ0	D/R			
P33	IN		IRQ1				
P34	OUT					$\overline{DM}$	
P35	OUT			R/D			
P36	OUT	T_{OUT}			R/D		
P37	OUT						Serial Out

Notes:
HS = Handshake Signals
D = $\overline{DAV}$ (Data Available)
R = RDY (Ready)

Autolatch. The autolatch places valid CMOS levels on all inputs that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Autolatches are available on Port 0, Port 1, Port 2, and P3 inputs.

$\overline{RESET}$ (input, Low). Initializes the MCU. RESET occurs through external reset only. During Power-On Reset, the externally-generated reset drives the $\overline{RESET}$ pin Low for the POR time. Pull-up is provided internally.

Caution: $\overline{RESET}$ depends on oscillator operation to achieve full reset conditions.

$\overline{RESET}$ is a Schmitt-triggered input. During the RESET cycle, $\overline{DS}$ is held active Low while $\overline{AS}$ cycles at a rate of $T_PC \div 2$. Program execution begins at location `000Ch`, after the $\overline{RESET}$ is released.

When program execution begins, $\overline{AS}$ and $\overline{DS}$ toggles only for external memory accesses. The Z8 can only exit Stop Mode by using the $\overline{RESET}$ pin.The Z8 does reset all registers on a Stop-Mode Recovery operation out of STOP mode.

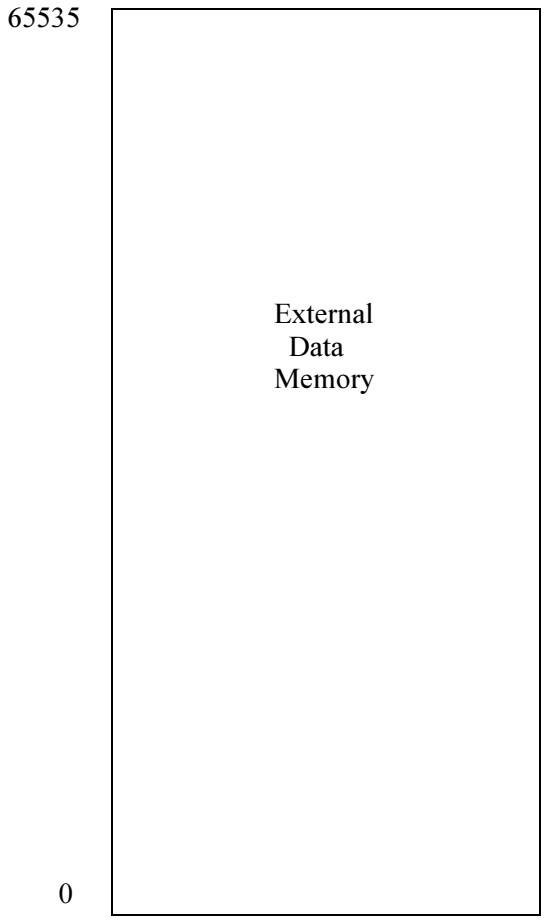


Figure 14. Data Memory Map

Register File. The register file contains three I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Stack Pointer (Bits 15-8)	SPH
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240	Serial I/O	SIO
239	General Purpose Registers	
4		
3	Port 3	P3
2	Port 2	P2
1	Reserved	Reserved
0	Port 0	P0

Figure 15. Register File

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

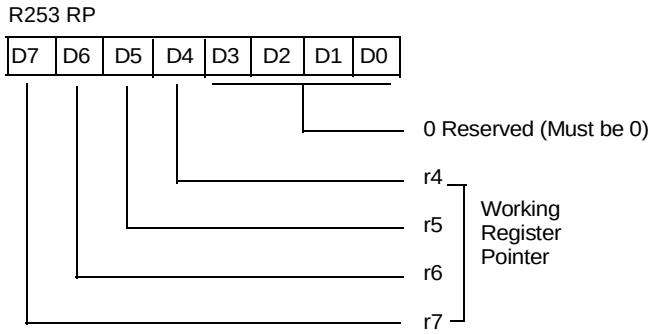


Figure 16. Register Pointer Register

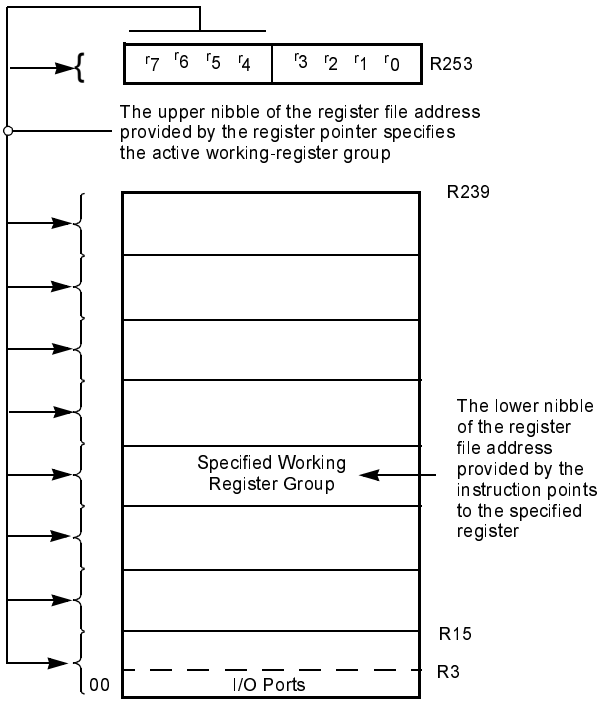


Figure 17. Register Pointer—Detail

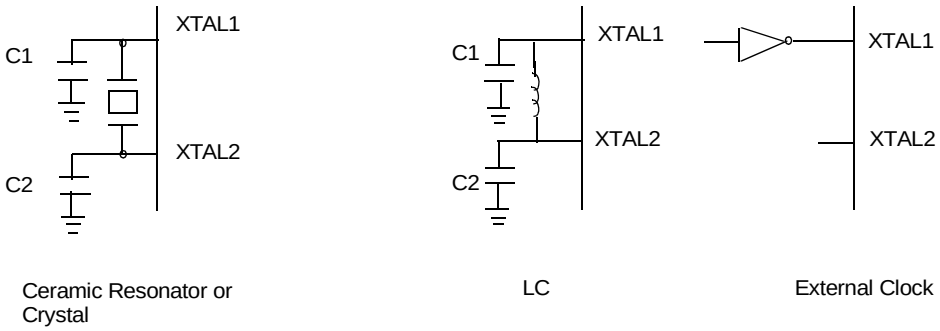


Figure 20. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation or the peripheral clock. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at location `000Ch`.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. Therefore, the user must execute a NOP (Op Code = `FFh`) immediately before the appropriate sleep instruction. For example:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

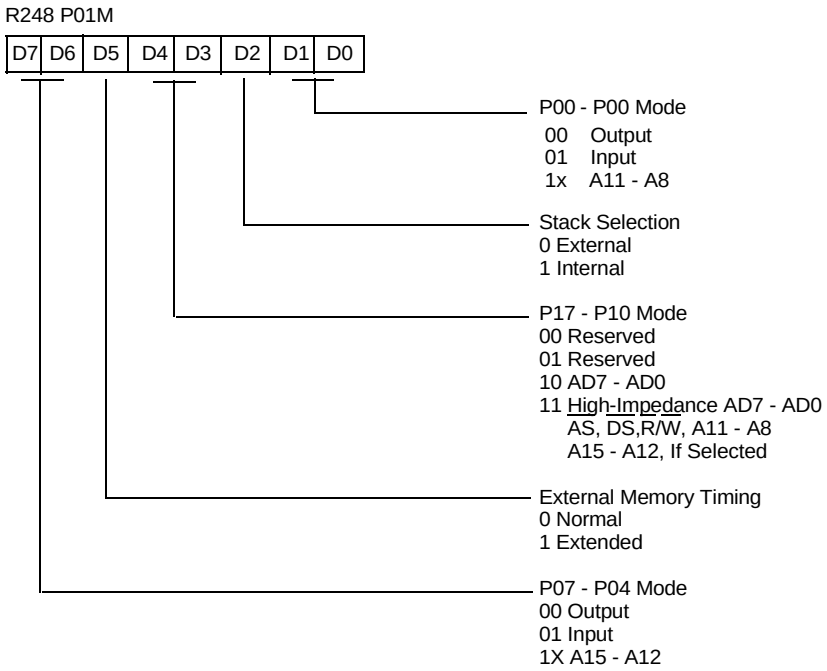


Figure 29. Port 0 and 1 Mode Register (F8h: Write Only)

Interrupt Priority Register. The Interrupt Priority Register, IPR, prioritizes interrupt functions and is shown in Figure 30.

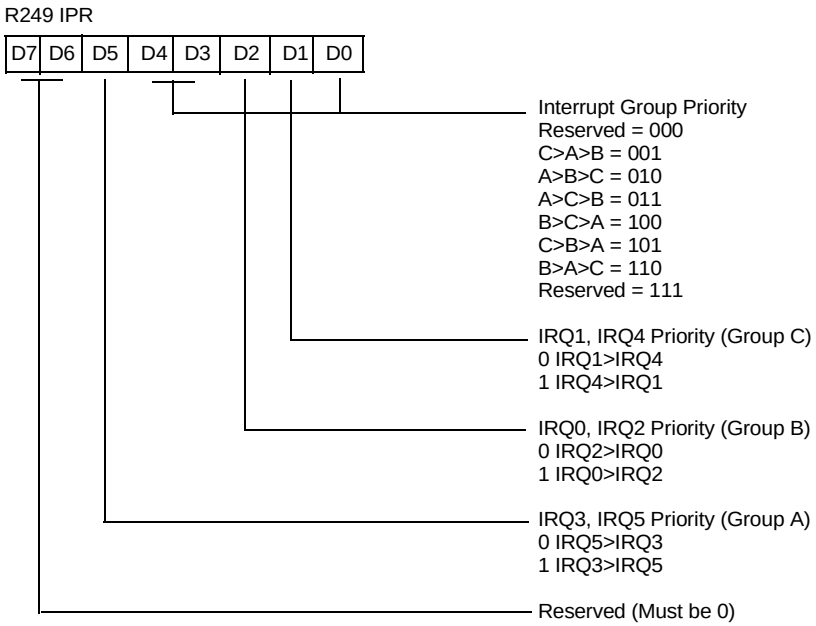


Figure 30. Interrupt Priority Register (F9h: Write Only)

Interrupt Request Register

The Interrupt Request Register, IRQ, controls interrupt functions and is shown in Figure 31.

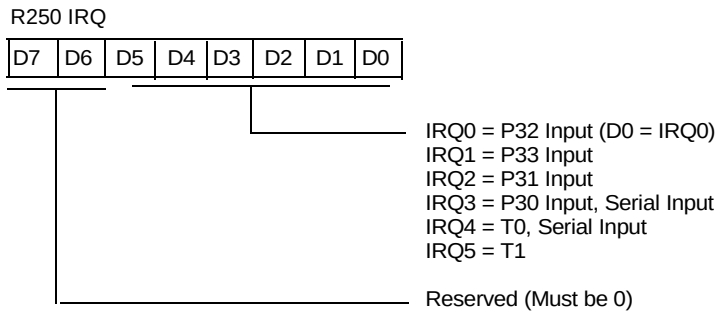


Figure 31. Interrupt Request Register (FAh: Read/Write)

Interrupt Mask Register

The Interrupt Mask Register, IMR, controls interrupt functions and is shown in Figure 32.

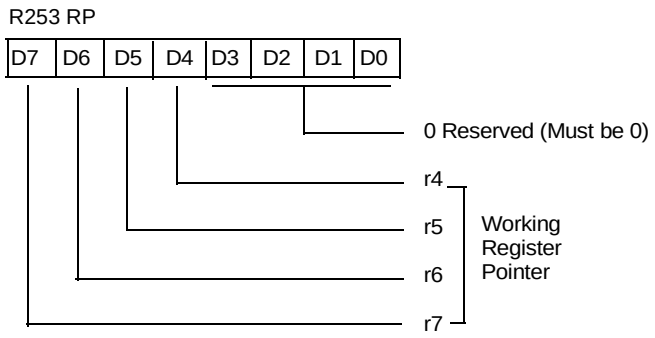


Figure 34. Register Pointer Register (FDh: Read/Write)

Stack Pointer High Register

The Stack Pointer High Register, SPH, controls pointer functions in the upper byte when the external stack is used and is shown in Figure 35.

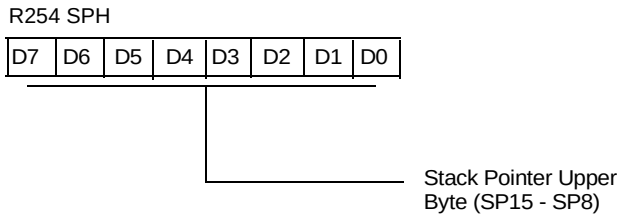


Figure 35. Stack Pointer Register (FEh: Read/Write)

Stack Pointer Low Register

The Stack Pointer Low Register, SPL, controls pointer functions in the lower byte and is shown in Figure 36.

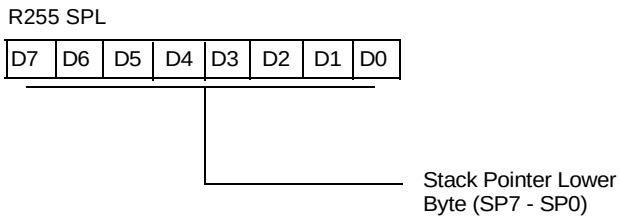


Figure 36. Stack Pointer Register (FFh: Read/Write)

Table 17. DC Electrical Characteristics at Standard and External Temperatures (Continued)

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical[2]		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@25°C**	**Units**	**Conditions**
V_{CL}	Clock Input Low Voltage	-0.3	0.8	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = -2.0 mA
V_{OH}	Output High Voltage	V_{CC}–100mV		V_{CC}–100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OH} = +2 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8	-0.3	0.8		V	
I_{IL}	Input Leakage	–2	2	-2	2		µA	Test at 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	-2	2		µA	Test at 0 V, V_{CC}
I_{IR}	Reset Input Current		–80		-80		µA	V_{RL}=0V
I_{CC}	Supply Current		35		35	24	mA	@ 16 MHz([1])
I_{CC1}	Standby Current		7		7	4.5	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		10	1	µA	STOP Mode V_{IN} = 0 V, V_{CC} ([1])
I_{ALL}	Autolatch Low Current	-10	10	-14	14		µA	

Note:
1. All inputs driven to 0V, V_{CC} and outputs floating.
2. V_{CC} = 5.0V

AC Electrical Characteristics

Figure 38 illustrates the timing characteristics of the Z86C91MCU with respect to external input/output sources. See Table 18 for descriptions of the numbered timing parameters in the figure.

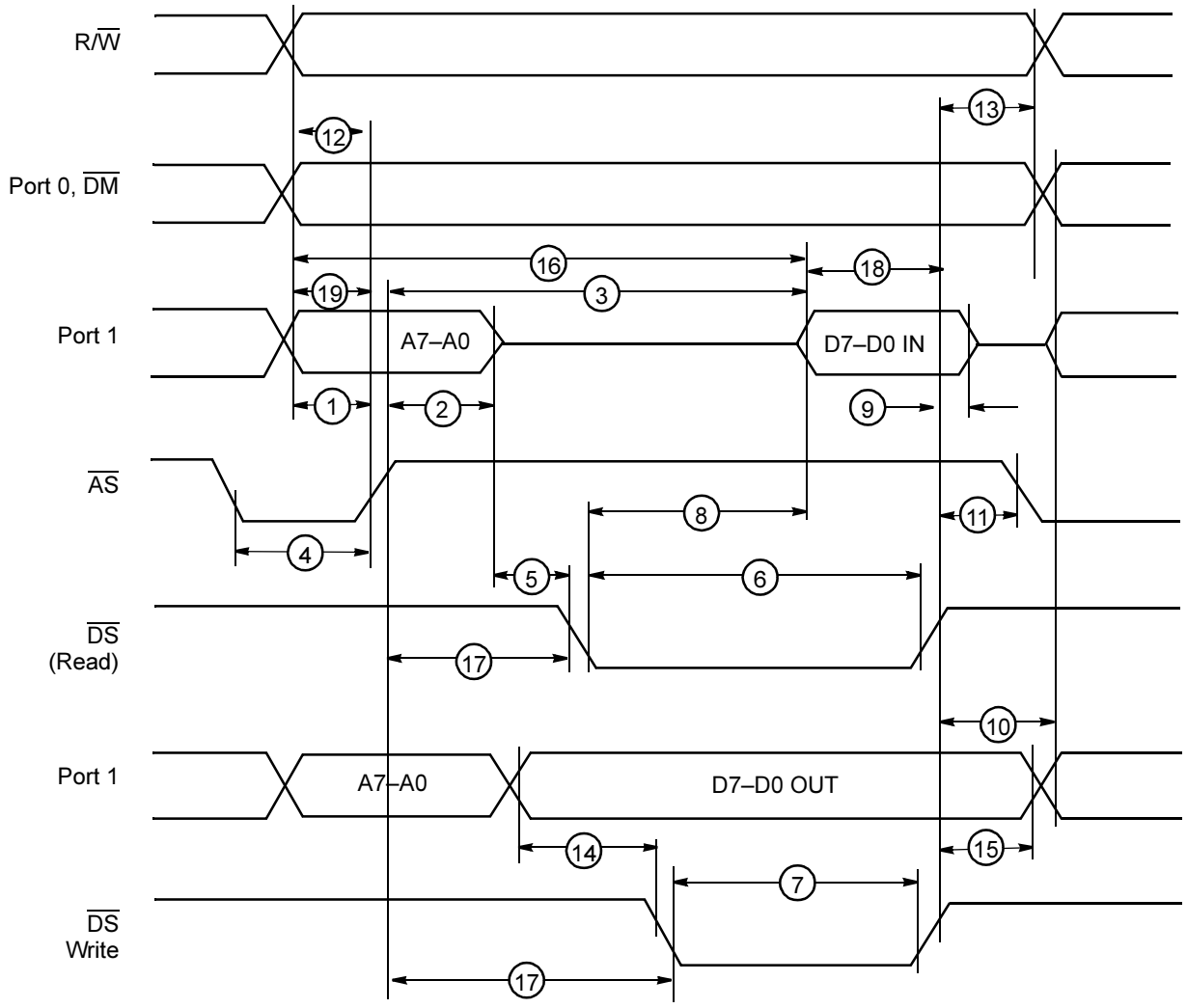


Figure 38. External I/O or Memory READ and WRITE Timing

Table 18. External I/O or Memory READ/WRITE Timing—Standard/Extended Temperature

			T_A = –0°C to 70°C @ 16 MHz		T_A = –40°C to 105°C @ 16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	T_DA(AS)	Address Valid to $\overline{AS}$ Rise Delay	25		25		ns	2,3
2	T_DAS(A)	$\overline{AS}$ Rise to Address Float Delay	35		35		ns	2,3
3	T_DAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid		180		180	ns	1,2,3
4	T_WAS	$\overline{AS}$ Low Width	40		40		ns	2,3
5	T_DAS(DS)	Address Float to $\overline{DS}$ Fall	0		0		ns	
6	T_WDSR	$\overline{DS}$ (Read) Low Width	135		135		ns	1,2,3
7	T_WDSW	$\overline{DS}$ (WRITE) Low Width	80		80		ns	1,2,3
8	T_DDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid		75		75	ns	1,2,3
9	T_HDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	0		0		ns	2,3
10	T_DDS(A)	$\overline{DS}$ Rise to Address Active Delay	50		50		ns	2,3
11	T_DDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	35		35		ns	2,3
12	T_DR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	25		25		ns	2,3
13	T_DDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	35		35		ns	2,3
14	T_DDW(DSW)	WRITE Data Valid to $\overline{DS}$ Fall (WRITE) Delay	25		25		ns	2,3
15	T_DDS(DW)	$\overline{DS}$ Rise to WRITE Data Not Valid Delay	35		35		ns	2,3
16	T_DA(DR)	Address Valid to Read Data Req'd Valid		230		230	ns	1,2,3
17	T_DAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	45		45		ns	2,3
18	T_DDI(DS)	Data Input Setup to $\overline{DS}$ Rise	60		60		ns	1,2,3
19	T_DDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	30		30		ns	2,3

Notes:
1. When using extended memory timing add 2 TpC.
2. Timing numbers provided are for minimum T_PC.
3. See Clock Cycle Dependent Characteristics table

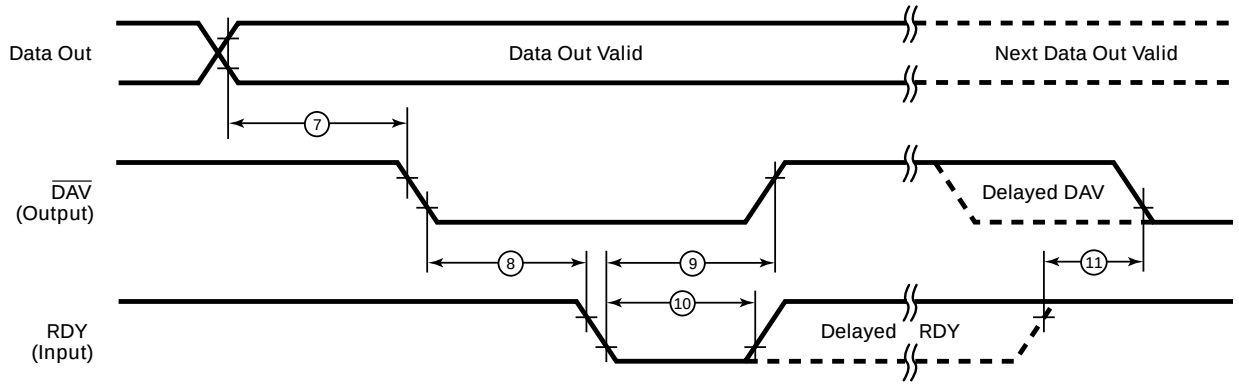
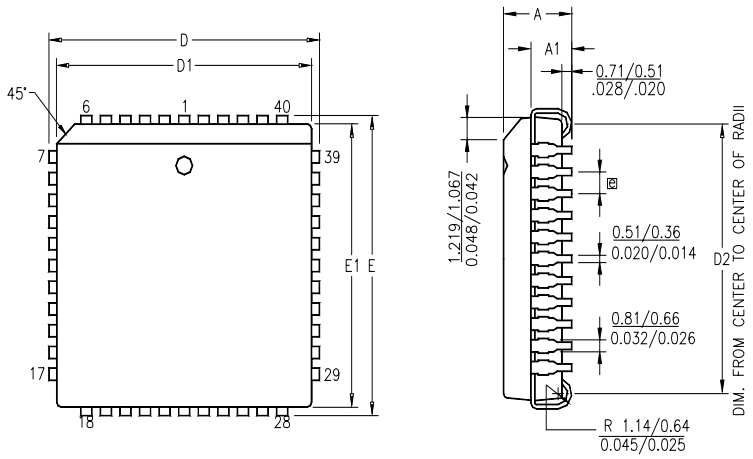


Figure 41. Output Handshake Timing

Table 21. Handshake Timing (Standard and Extended Temperatures)

No	Symbol	Parameter	T_A = 0ºC to +70ºC Min	T_A = 0ºC to +70ºC Max	T_A = -40ºC to +105ºC Min	T_A = -40ºC to +105ºC Max	Data Direction
1	T_SDI(DAV)	Data In Setup Time	0		0		Input
2	T_HDI(RDY)	Data In Hold Time	145		145		Input
3	T_WDAV	Data Available Width	110		110		Input
4	T_DDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	Input
5	T_DDAVId(RDY)	DAV Out to DAV Fall Delay		115		115	Input
6	RDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	0		0		Input
7	T_DD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	Output
8	T_DDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		Output
9	T_DRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	Output
10	T_WRDY	RDY Width	110		110		Output
11	T_DRDY0$_D$(DAV)	RDY Rise to DAV Fall Delay		115		115	Output

Note: All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
   INCH

Figure 43. 44-Pin PLCC Package Diagram

Document Information

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0185	Unique Document Number
01	Revision Number
0802	Month and Year Published