What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	10MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	2KB (1K x 16)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90s2313-10si

Architectural Overview

The fast-access Register File concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Figure 4. The AT90S2313 AVR RISC Architecture
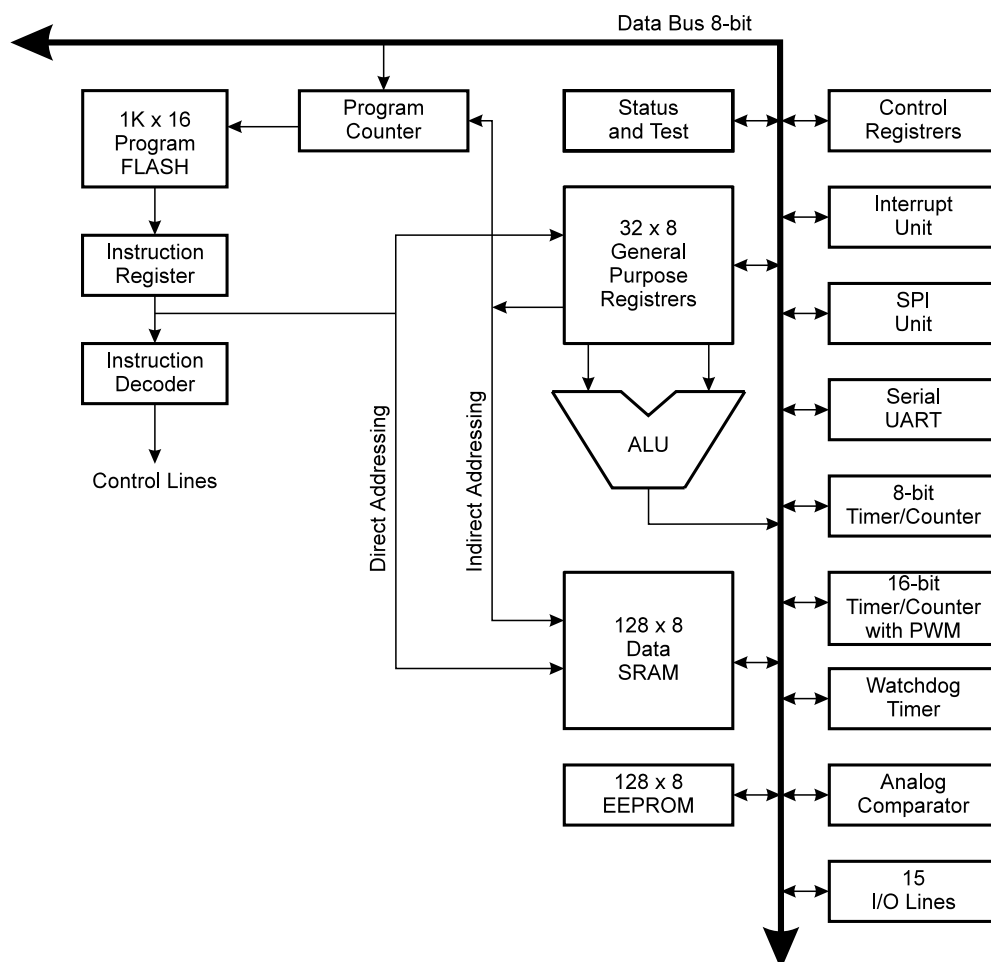
Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look-up function. These added function registers are the 16-bit X-register, Y-register, and Z-register.

The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S2313 AVR RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the Register File as well. This is enabled by the fact that the Register File is assigned the 32 lowermost Data Space addresses ($00 - $1F), allowing them to be accessed as though they were ordinary memory locations.

Operand address is contained in 6 bits of the instruction word. n is the destination or source register address.
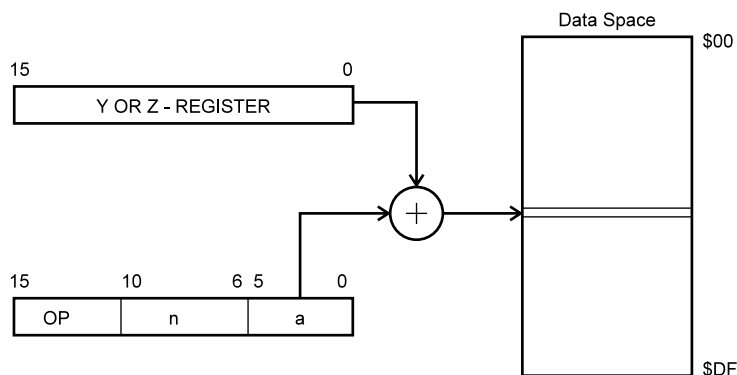
Data Direct

Figure 12. Direct Data Addressing
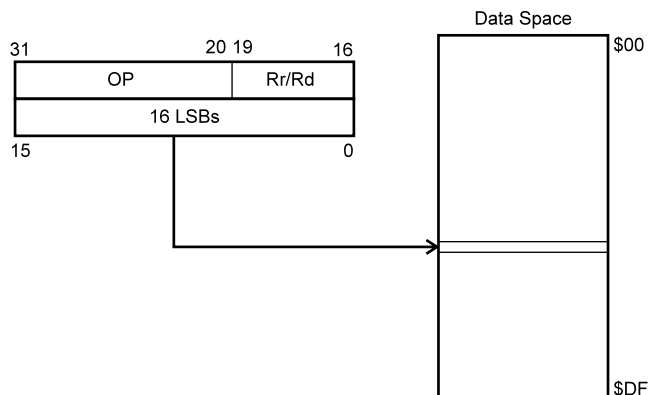
A 16-bit data address is contained in the 16 LSBs of a 2-word instruction. Rd/Rr specify the destination or source register.
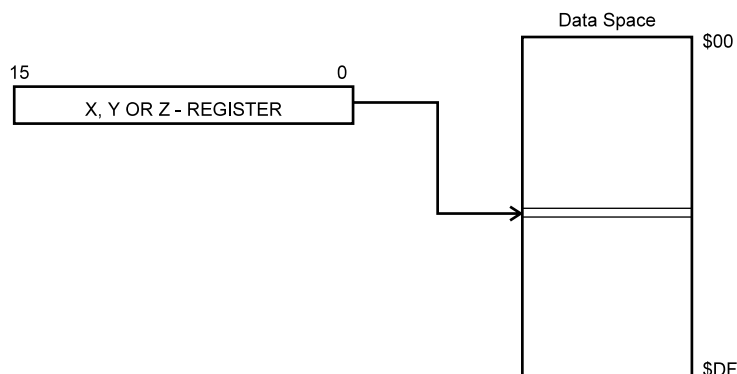
Data Indirect with Displacement

Figure 13. Data Indirect with Displacement

Operand address is the result of the Y- or Z-register contents added to the address contained in 6 bits of the instruction word.

Data Indirect

Figure 14. Data Indirect Addressing

Operand address is the contents of the X-, Y-, or Z-register.

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Memory Access and Instruction Execution Timing

This section describes the general access timing concepts for instruction execution and internal memory access.

The AVR CPU is driven by the System Clock Ø, directly generated from the external clock crystal for the chip. No internal clock division is used.

Figure 20 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access Register File concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks and functions per power-unit.

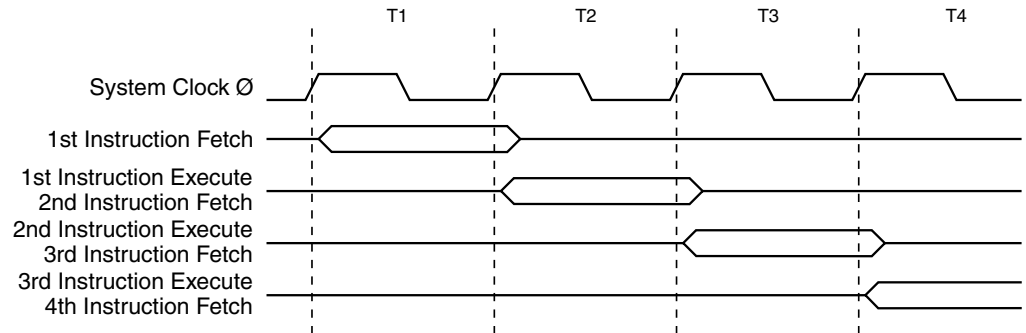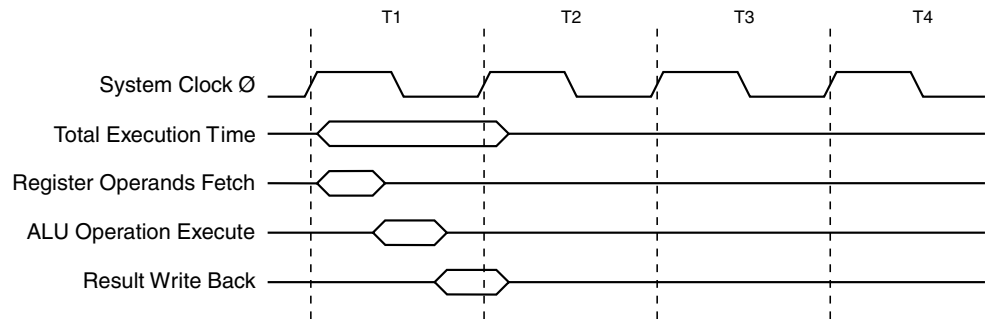**Figure 20.** The Parallel Instruction Fetches and Instruction Executions

Figure 21 shows the internal timing concept for the Register File. In a single clock cycle an ALU operation using two register operands is executed, and the result is stored back to the destination register.

Figure 21. Single-cycle ALU Operation

The internal data SRAM access is performed in two System Clock cycles as described in Figure 22.

Reset Sources

The AT90S2313 has three sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the Power-on Reset threshold (V_{POT}).
- External Reset. The MCU is reset when a low level is present on the $\overline{RESET}$ pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog Timer period expires and the Watchdog is enabled.

During Reset, all I/O Registers are then set to their initial values, and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP (Relative Jump) instruction to the reset handling routine. If the program never enables an interrupt source, the Interrupt Vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 23 shows the reset logic. Table 3 defines the timing and electrical parameters of the reset circuitry.

Figure 23. Reset Logic
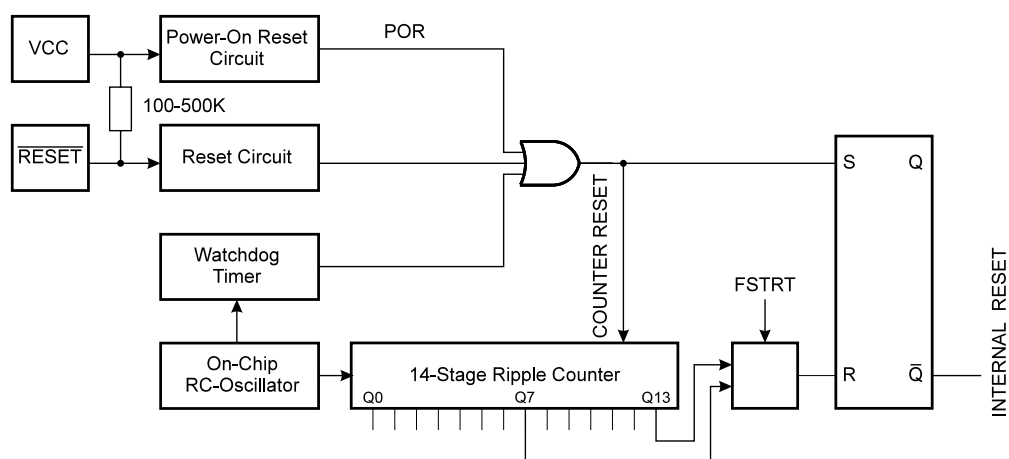
Table 3. Reset Characteristics (V_{CC} = 5.0V)

Symbol	Parameter	Min	Typ	Max	Units
V_{POT}[1]	Power-on Reset Threshold Voltage (rising)	1.0	1.4	1.8	V
	Power-on Reset Threshold Voltage (falling)	0.4	0.6	0.8	V
V_{RST}	$\overline{RESET}$ Pin Threshold Voltage		–	0.85 V_{CC}	V
t_{TOUT}	Reset Delay Time-out Period FSTRT Unprogrammed	11.0	16.0	21.0	ms
t_{TOUT}	Reset Delay Time-out Period FSTRT Programmed	0.25	0.28	0.31	ms

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

The user can select the start-up time according to typical Oscillator start-up. The number of WDT Oscillator cycles used for each time-out is shown in Table 4. The frequency of the Watchdog Oscillator is voltage-dependent, as shown in "Typical Characteristics" on page 74.

General Interrupt FLAG Register – GIFR

Bit	7	6	5	4	3	2	1	0	
$3A ($5A)	INTF1	INTF0	–	–	–	–	–	–	GIFR
Read/Write	R/W	R/W	R	R	R	R	R	R	
Initial value	0	0	0	0	0	0	0	0	

• Bit 7 – INTF1: External Interrupt Flag1

When an edge on the INT1 pin triggers an interrupt request, the corresponding Interrupt Flag, INTF1, becomes set (one). If the I-bit in SREG and the corresponding interrupt enable bit, INT1 bit in GIMSK, are set (one), the MCU will jump to the Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical "1" to it. The flag is always cleared when INT1 is configured as level interrupt.

• Bit 6 – INTF0: External Interrupt Flag0

When an edge on the INT0 pin triggers an interrupt request, the corresponding Interrupt Flag, INTF0, becomes set (one). If the I-bit in SREG and the corresponding interrupt enable bit, INT0 bit in GIMSK, are set (one), the MCU will jump to the Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical "1" to it. The flag is always cleared when INT0 is configured as level interrupt.

• Bits 5..0 – Res: Reserved Bits

These bits are reserved bits in the AT90S2313 and always read as zero.

Note that external level interrupt does not have a flag, and will only be remembered for as long as the interrupt condition is active.

Timer/Counter Interrupt Mask Register – TIMSK

Bit	7	6	5	4	3	2	1	0	
$39 ($59)	TOIE1	OCIE1A	–	–	TICIE1	–	TOIE0	–	TIMSK
Read/Write	R/W	R/W	R	R	R/W	R	R/W	R	
Initial value	0	0	0	0	0	0	0	0	

• Bit 7 – TOIE1: Timer/Counter1 Overflow Interrupt Enable

When the TOIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Overflow Interrupt is enabled. The corresponding interrupt (at vector $005) is executed if an overflow in Timer/Counter1 occurs (i.e., when the TOV1 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

• Bit 6 – OCIE1A: Timer/Counter1 Output Compare Match Interrupt Enable

When the OCIE1A bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Compare Match Interrupt is enabled. The corresponding interrupt (at vector $004) is executed if a compare match in Timer/Counter1 occurs (i.e., when the OCF1A bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

• Bit 5,4 – Res: Reserved Bits

These bits are reserved bits in the AT90S2313 and always read as zero.

• Bit 3 – TICIE1: Timer/Counter1 Input Capture Interrupt Enable

When the TICIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Input Capture Event Interrupt is enabled. The corresponding interrupt (at vector $003) is executed if a capture-triggering event occurs on PD6(ICP) (i.e., when the ICF1 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

• Bit 2 – Res: Reserved Bit

This bit is a reserved bit in the AT90S2313 and always reads as zero.

• Bit 1 – TOIE0: Timer/Counter0 Overflow Interrupt Enable

When the TOIE0 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow Interrupt is enabled. The corresponding interrupt (at vector $006) is executed if an overflow in Timer/Counter0 occurs (i.e., when the TOV0 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

• Bit 0 – Res: Reserved Bit

This bit is a reserved bit in the AT90S2313 and always read as zero.

Timer/Counter Interrupt FLAG Register – TIFR

Bit	7	6	5	4	3	2	1	0	
$38 ($58)	TOV1	OCF1A	–	–	ICF1	–	TOV0	–	TIFR
Read/Write	R/W	R/W	R	R	R/W	R	R/W	R	
Initial value	0	0	0	0	0	0	0	0	

• Bit 7 – TOV1: Timer/Counter1 Overflow Flag

The TOV1 is set (one) when an overflow occurs in Timer/Counter1. TOV1 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV1 is cleared by writing a logical "1" to the flag. When the I-bit in SREG and TOIE1 (Timer/Counter1 Overflow Interrupt Enable) and TOV1 are set (one), the Timer/Counter1 Overflow Interrupt is executed. In PWM mode, this bit is set when Timer/Counter1 changes counting direction at $0000.

• Bit 6 – OCF1A: Output Compare Flag 1A

The OCF1A bit is set (one) when a compare match occurs between the Timer/Counter1 and the data in OCR1A (Output Compare Register1 A). OCF1A is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF1A is cleared by writing a logical "1" to the flag. When the I-bit in SREG and OCIE1A (Timer/Counter1 Compare Match Interrupt Enable) and the OCF1A are set (one), the Timer/Counter1 Compare Match Interrupt is executed.

• Bits 5, 4 – Res: Reserved Bits

These bits are reserved bits in the AT90S2313 and always read as zero.

• Bit 3 – ICF1: Input Capture Flag 1

The ICF1 bit is set (one) to flag an input capture event, indicating that the Timer/Counter1 value has been transferred to the Input Capture Register (ICR1). ICF1 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ICF1 is cleared by writing a logical "1" to the flag. When the SREG I-bit and TICIE1 (Timer/Counter1 Input Capture Interrupt Enable) and ICF1 are set (one), the Timer/Counter1 Capture Interrupt is executed.

• Bit 2 – Res: Reserved Bit

This bit is a reserved bit in the AT90S2313 and always reads as zero.

• Bit 1 – TOV0: Timer/Counter0 Overflow Flag

The bit TOV0 is set (one) when an overflow occurs in Timer/Counter0. TOV0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV0 is cleared by writing a logical "1" to the flag. When the SREG I-bit and TOIE0 (Timer/Counter0 Overflow Interrupt Enable) and TOV0 are set (one), the Timer/Counter0 Overflow Interrupt is executed.

• Bit 0 – Res: Reserved Bit

This bit is a reserved bit in the AT90S2313 and always reads as zero.

External Interrupts

The External Interrupts are triggered by the INT1 and INT0 pins. Observe that, if enabled, the interrupts will trigger even if the INT0/INT1 pins are configured as outputs. This feature provides a way of generating a software interrupt. The External Interrupts can be triggered by a falling or rising edge or a low level. This is set up as indicated in the specification for the MCU Control Register (MCUCR). When the External Interrupt is enabled and is configured as level-triggered, the interrupt will trigger as long as the pin is held low.

The External Interrupts are set up as described in the specification for the MCU Control Register (MCUCR).

Interrupt Response Time

The interrupt execution response for all the enabled AVR interrupts is four clock cycles, minimum. Four clock cycles after the Interrupt Flag has been set, the Program Vector address for the actual interrupt handling routine is executed. During this four clock cycle period, the Program Counter (two bytes) is pushed onto the Stack, and the Stack Pointer is decremented by two. The Power-down is normally a relative jump to the interrupt routine, and this jump takes two clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter (two bytes) is popped back from the Stack, the Stack Pointer is incremented by two, and the I-flag in SREG is set. When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

MCU Control Register – MCUCR

The MCU Control Register contains control bits for general MCU functions.

Bit	7	6	5	4	3	2	1	0	
$35 ($55)	–	–	SE	SM	ISC11	ISC10	ISC01	ISC00	MCUCR
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

• Bits 7, 6 – Res: Reserved Bits

These bits are reserved bits in the AT90S2313 and always read as zero.

• Bit 5 – SE: Sleep Enable

The SE bit must be set (one) to make the MCU enter the sleep mode when the SLEEP instruction is executed. To avoid the MCU entering the sleep mode unless it is the programmer's purpose, it is recommended to set the Sleep Enable (SE) bit just before the execution of the SLEEP instruction.

• **Bits 2,1,0 – CS12, CS11, CS10: Clock Select1, Bits 2, 1 and 0**

The Clock Select1 bits 2, 1, and 0 define the prescaling source of Timer/Counter1.

Table 10. Clock 1 Prescale Select

CS12	CS11	CS10	Description
0	0	0	Stop, the Timer/Counter1 is stopped.
0	0	1	CK
0	1	0	CK/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T1, falling edge
1	1	1	External Pin T1, rising edge

The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK Oscillator clock. If the external pin modes are used for Timer/Counter1, transitions on PD5/(T1) will clock the counter even if the pin is configured as an output. This feature can give the user software control of the counting.

Timer/Counter1 – TCNT1H and TCNT1L

Bit	15	14	13	12	11	10	9	8	
$2D ($4D)	MSB								TCNT1H
$2C ($4C)								LSB	TCNT1L
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

This 16-bit register contains the prescaled value of the 16-bit Timer/Counter1. To ensure that both the high and low bytes are read and written simultaneously when the CPU accesses these registers, the access is performed using an 8-bit temporary register (TEMP). This temporary register is also used when accessing OCR1A and ICR1. If the main program and interrupt routines perform access to registers using TEMP, interrupts must be disabled during access from the main program or interrupts if interrupts are re-enabled.

•	TCNT1 Timer/Counter1 Write:
	When the CPU writes to the high byte TCNT1H, the written data is placed in the TEMP Register. Next, when the CPU writes the low byte TCNT1L, this byte of data is combined with the byte data in the TEMP Register, and all 16 bits are written to the TCNT1 Timer/Counter1 Register simultaneously. Consequently, the high byte TCNT1H must be accessed first for a full 16-bit register write operation.

•	TCNT1 Timer/Counter1 Read:
	When the CPU reads the low byte TCNT1L, the data of the low byte TCNT1L is sent to the CPU and the data of the high byte TCNT1H is placed in the TEMP Register. When the CPU reads the data in the high byte TCNT1H, the CPU receives the data in the TEMP Register. Consequently, the low byte TCNT1L must be accessed first for a full 16-bit register read operation.

Watchdog Timer

The Watchdog Timer is clocked from a separate On-chip Oscillator that runs at 1 MHz. This is the typical value at $V_{CC} = 5V$. See characterization data for typical values at other V_{CC} levels. By controlling the Watchdog Timer prescaler, the Watchdog Reset interval can be adjusted. See Table 14 for a detailed description. The WDR (Watchdog Reset) instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog Reset, the AT90S2313 resets and executes from the Reset Vector. For timing details on the Watchdog Reset, refer to page 21.

To prevent unintentional disabling of the Watchdog, a special turn-off sequence must be followed when the Watchdog is disabled. Refer to the description of the Watchdog Timer Control Register for details.

Figure 33. Watchdog Timer
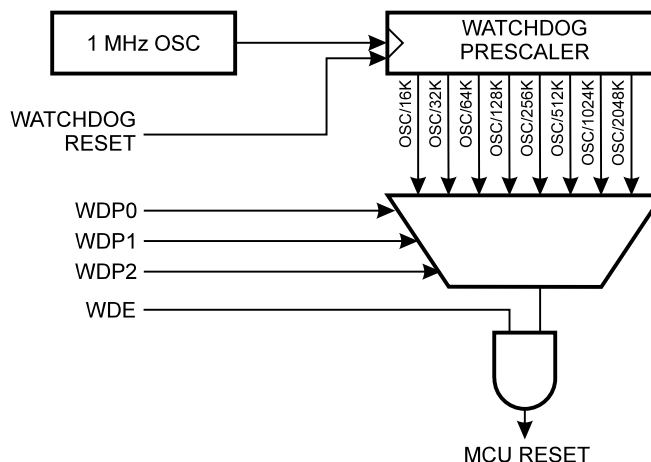
Watchdog Timer Control Register – WDTCR

Bit	7	6	5	4	3	2	1	0	
$21 ($41)	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

• Bits 7..5 – Res: Reserved Bits

These bits are reserved bits in the AT90S2313 and will always read as zero.

• Bit 4 – WDTOE: Watchdog Turn-off Enable

This bit must be set (one) when the WDE bit is cleared. Otherwise, the Watchdog will not be disabled. Once set, hardware will clear this bit to zero after four clock cycles. Refer to the description of the WDE bit for a Watchdog disable procedure.

• Bit 3 – WDE: Watchdog Enable

When the WDE is set (one) the Watchdog Timer is enabled, and if the WDE is cleared (zero), the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit is set (one). To disable an enabled Watchdog Timer, the following procedure must be followed:

1. In the same operation, write a logical "1" to WDTOE and WDE. A logical "1" must be written to WDE even though it is set to 1 before the disable operation starts.

2. Within the next four clock cycles, write a logical "0" to WDE. This disables the Watchdog.

• Bits 2..0 – WDP2, WDP1, WDP0: Watchdog Timer Prescaler 2, 1 and 0

The WDP2, WDP1 and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding time-out periods are shown in Table 14.

Table 14. Watchdog Timer Prescale Select[1]

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles	Typical Time-out at V_{CC} = 3.0V	Typical Time-out at V_{CC} = 5.0V
0	0	0	16K cycles	47 ms	15 ms
0	0	1	32K cycles	94 ms	30 ms
0	1	0	64K cycles	0.19 s	60 ms
0	1	1	128K cycles	0.38 s	0.12 s
1	0	0	256K cycles	0.75 s	0,24 s
1	0	1	512K cycles	1.5 s	0.49 s
1	1	0	1,024K cycles	3.0 s	0.97 s
1	1	1	2,048K cycles	6.0 s	1.9 s

Note: 1. The frequency of the Watchdog Oscillator is voltage-dependent, as shown in the Electrical Characteristics section.
The WDR (Watchdog Reset) instruction should always be executed before the Watchdog Timer is enabled. This ensures that the reset period will be in accordance with the Watchdog Timer prescale settings. If the Watchdog Timer is enabled without reset, the Watchdog Timer may not start counting from zero.
To avoid unintentional MCU Reset, the Watchdog Timer should be disabled or reset before changing the Watchdog Timer Prescale Select.

tus Register (USR) is set. When this bit is set (one), the UART is ready to receive the next character. At the same time as the data is transferred from UDR to the 10(11)-bit Shift Register, bit 0 of the Shift Register is cleared (start bit) and bit 9 or 10 is set (stop bit). If 9-bit data word is selected (the CHR9 bit in the UART Control Register [UCR] is set), the TXB8 bit in UCR is transferred to bit 9 in the Transmit Shift Register.

On the Baud Rate clock following the transfer operation to the Shift Register, the start bit is shifted out on the TXD pin. Then follows the data, LSB first. When the stop bit has been shifted out, the Shift Register is loaded if any new data has been written to the UDR during the transmission. During loading, UDRE is set. If there is no new data in the UDR Register to send when the stop bit is shifted out, the UDRE Flag will remain set until UDR is written again. When no new data has been written, and the stop bit has been present on TXD for one bit length, the TX Complete Flag (TXC) in USR is set.

The TXEN bit in UCR enables the UART transmitter when set (one). When this bit is cleared (zero), the PD1 pin can be used for general I/O. When TXEN is set, the UART Transmitter will be connected to PD1, which is forced to be an output pin regardless of the setting of the DDD1 bit in DDRD.

Data Reception

Figure 35 shows a block diagram of the UART Receiver.

Figure 35. UART Receiver
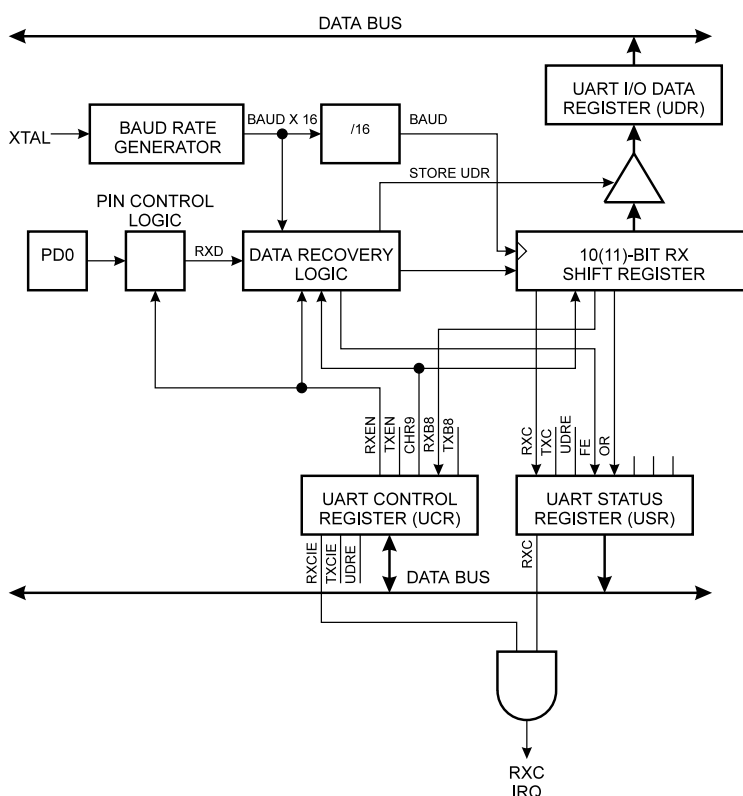
The Receiver front-end logic samples the signal on the RXD pin at a frequency of 16 times the baud rate. While the line is idle, one single sample of logical "0" will be interpreted as the falling edge of a start bit, and the start bit detection sequence is initiated. Let sample 1 denote the first zero-sample. Following the 1-to-0 transition, the receiver samples the RXD pin at samples 8, 9 and 10. If two or more of these three samples are

Figure 39. Port B Schematic Diagram (Pin PB3)

WP: WRITE PORTB
WD: WRITE DDRB
RL: READ PORTB LATCH
RP: READ PORTB PIN
RD: READ DDRB
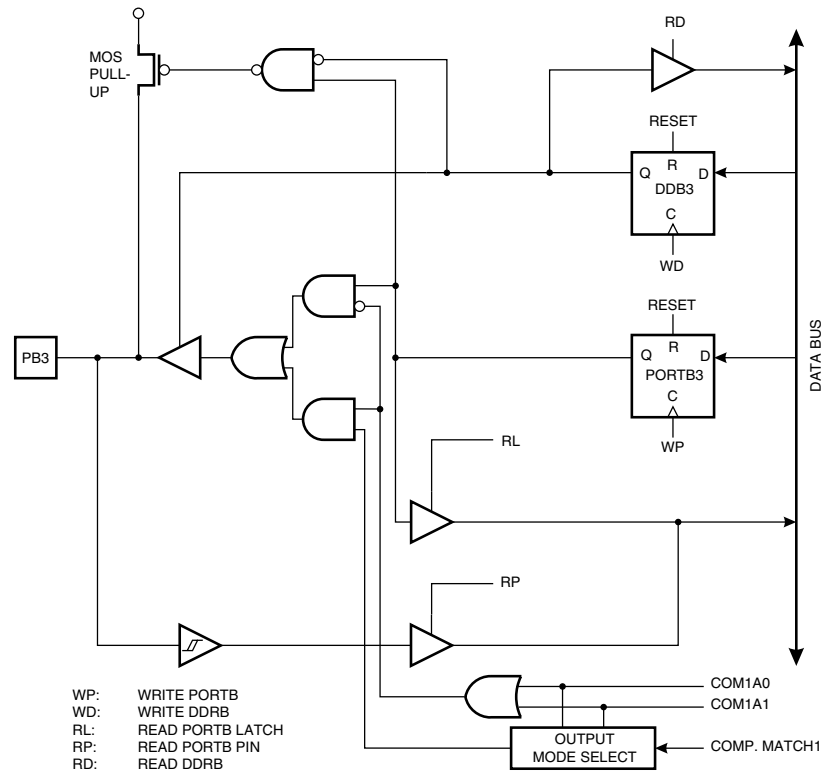
Figure 40. Port B Schematic Diagram (Pins PB2 and PB4)

WP: WRITE PORTB
WD: WRITE DDRB
RL: READ PORTB LATCH
RP: READ PORTB PIN
RD: READ DDRB
n: 2, 4

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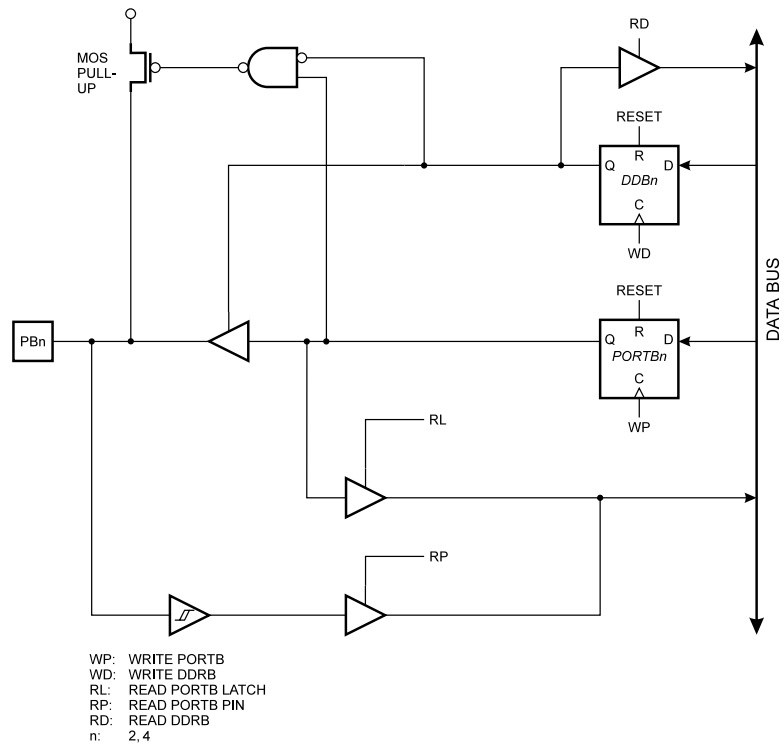
Port D Data Register – PORTD

Bit	7	6	5	4	3	2	1	0	
$12 ($32)	–	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

Port D Data Direction Register – DDRD

Bit	7	6	5	4	3	2	1	0	
$11 ($31)	–	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

Port D Input Pins Address – PIND

Bit	7	6	5	4	3	2	1	0	
$10 ($30)	–	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
Read/Write	R	R	R	R	R	R	R	R	
Initial value	0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port D Input Pins address (PIND) is not a register; this address enables access to the physical value on each Port D pin. When reading PORTD, the Port D Data Latch is read, and when reading PIND, the logical values present on the pins are read.

Port D as General Digital I/O   PDn, general I/O pin: The DDDn bit in the DDRD Register selects the direction of this pin. If DDDn is set (one), PDn is configured as an output pin. If DDDn is cleared (zero), PDn is configured as an input pin. If PORTDn is set (one) when configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, the PORTDn has to be cleared (zero) or the pin has to be configured as an output pin. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Table 20. DDDn Bits on Port D Pins[1]

DDDn	PORTDn	I/O	Pull-up	Comment
0	0	Input	No	Tri-state (High-Z)
0	1	Input	Yes	PDn will source current if ext. pulled low
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: 1. n: 6…0, pin number.

Alternate Functions of Port D   The alternate functions of Port D are:

• ICP – Port D, Bit 6

Timer/Counter1 Input Capture pin. See the Timer/Counter1 description for further details.

• T1 – Port D, Bit 5

T1, Timer 1 Clock source. See the Timer description for further details.

• T0 – Port D, Bit 4

T0, Timer/Counter0 Clock source. See the Timer description for further details.

Memory Programming

Program and Data Memory Lock Bits

The AT90S2313 MCU provides two Lock bits that can be left unprogrammed ("1") or can be programmed ("0") to obtain the additional features listed in Table 21. The Lock bits can only be erased with the Chip Erase operation.

Table 21. Lock Bit Protection Modes

Memory Lock Bits			
Mode	LB1	LB2	Protection Type
1	1	1	No memory lock features enabled.
2	0	1	Further programming of the Flash and EEPROM is disabled.[1]
3	0	0	Same as mode 2, and verify is also disabled.

Note: 1. In the Parallel mode, further programming of the Fuse bits are also disabled. Program the Fuse bits before programming the Lock bits.

Fuse Bits

The AT90S2313 has two Fuse bits: SPIEN and FSTRT.

- When the SPIEN Fuse is programmed ("0"), Serial Program and Data Downloading is enabled. The default value is programmed ("0").

- When the FSTRT Fuse is programmed ("0"), the short start-up time is selected. The default value is unprogrammed ("1"). Parts with this bit pre-programmed ("0") can be delivered on demand.

The Fuse bits are not accessible in Serial Programming mode. The status of the fuses are not affected by Chip Erase.

Signature Bytes

All Atmel microcontrollers have a 3-byte signature code that identifies the device. This code can be read in both serial and parallel mode. The three bytes reside in a separate address space.

For the AT90S2313[1] they are:

1. $000: $1E (indicates manufactured by Atmel).
2. $001: $91 (indicates 2 Kb Flash memory).
3. $002: $01 (indicates AT90S2313 device when signature byte $001 is $91).

Note: 1. When both Lock bits are programmed (Lock mode 3), the signature bytes cannot be read in serial mode. Reading the signature bytes will return: $00, $01 and $02.

Programming the Flash and EEPROM

Atmel's AT90S2313 offers 2K bytes of In-System Reprogrammable Flash Program memory and 128 bytes of EEPROM Data memory.

The AT90S2313 is shipped with the On-chip Flash Program and EEPROM Data memory arrays in the erased state (i.e., contents = $FF) and ready to be programmed. This device supports a high-voltage (12V) Parallel Programming mode and a low-voltage Serial Programming mode. The +12V is used for programming enable only, and no current of significance is drawn by this pin. The Serial Programming mode provides a convenient way to download program and data into the AT90S2313 inside the user's system.

The program and EEPROM memory arrays in the AT90S2313 are programmed byte-by-byte in either programming mode. For the EEPROM, an auto-erase cycle is provided

within the self-timed write instruction in the Serial Programming mode. During programming, the supply voltage must be in accordance with Table 22.

Table 22. Supply Voltage during Programming

Part	Serial Programming	Parallel Programming
AT90S2313	2.7 - 6.0V	4.5 - 5.5V

Parallel Programming

This section describes how to parallel program and verify Flash Program memory, EEPROM data memory, Lock bits and Fuse bits in the AT90S2313.

Signal Names

In this section, some pins of the AT90S2313 are referenced by signal names describing their function during parallel programming. Pins not described in the following table are referenced by pin names. See Figure 49 and Table 23. Pins not described in Table 23 are referenced by pin names.

The XA1/XA0 pins determine the action executed when the XTAL1 pin is given a positive pulse. The bit coding is shown in Table 24.

When pulsing $\overline{WR}$ or $\overline{OE}$, the command loaded determines the action executed. The command is a byte where the different bits are assigned functions as shown in Table 25.
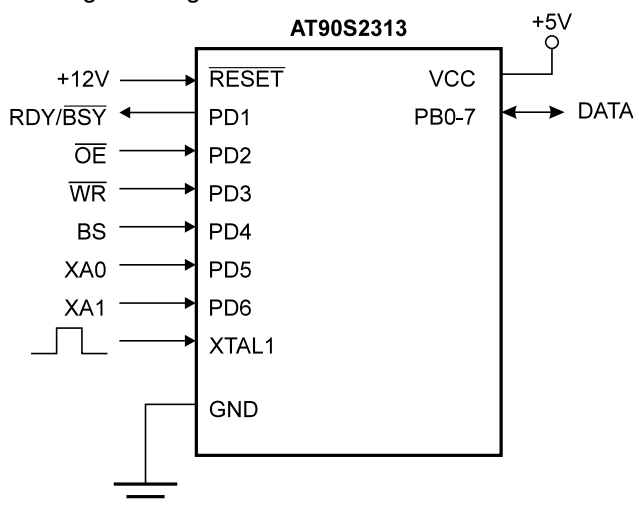
Figure 49. Parallel Programming

Table 23. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/$\overline{BSY}$	PD1	O	0: Device is busy programming, 1: Device is ready for new command
$\overline{OE}$	PD2	I	Output Enable (Active low)
$\overline{WR}$	PD3	I	Write Pulse (Active low)
BS	PD4	I	Byte Select ("0" selects low byte, "1" selects high byte)

5. Give $\overline{\text{WR}}$ a $t_{\text{WLWH\_CE}}$ wide negative pulse to execute Chip Erase. See Table 26 for $t_{\text{WLWH\_CE}}$ value. Chip Erase does not generate any activity on the RDY/$\overline{\text{BSY}}$ pin.

Programming the Flash

A: Load Command "Write Flash"

1. Set XA1, XA0 to "10". This enables command loading.
2. Set BS to "0".
3. Set DATA to "0001 0000". This is the command for Write Flash.
4. Give XTAL1 a positive pulse. This loads the command.

B: Load Address High Byte

1. Set XA1, XA0 to "00". This enables address loading.
2. Set BS to "1". This selects high byte.
3. Set DATA = Address high byte ($00 - $03).
4. Give XTAL1 a positive pulse. This loads the address high byte.

C: Load Address Low Byte

1. Set XA1, XA0 to "00". This enables address loading.
2. Set BS to "0". This selects low byte.
3. Set DATA = Address low byte ($00 - $FF).
4. Give XTAL1 a positive pulse. This loads the address low byte.

D: Load Data Low Byte

1. Set XA1, XA0 to "01". This enables data loading.
2. Set DATA = Data low byte ($00 - $FF).
3. Give XTAL1 a positive pulse. This loads the data low byte.

E: Write Data Low Byte

1. Set BS to "0". This selects low data.
2. Give $\overline{\text{WR}}$ a negative pulse. This starts programming of the data byte. RDY/$\overline{\text{BSY}}$ goes low.
3. Wait until RDY/$\overline{\text{BSY}}$ goes high to program the next byte.

(See Figure 50 for signal waveforms.)

F: Load Data High Byte

1. Set XA1, XA0 to "01". This enables data loading.
2. Set DATA = Data high byte ($00 - $FF).
3. Give XTAL1 a positive pulse. This loads the data high byte.

G: Write Data High Byte

1. Set BS to "1". This selects high data.
2. Give $\overline{\text{WR}}$ a negative pulse. This starts programming of the data byte. RDY/$\overline{\text{BSY}}$ goes low.
3. Wait until RDY/$\overline{\text{BSY}}$ goes high to program the next byte.

(See Figure 51 for signal waveforms.)

Serial Downloading

Both the program and data memory arrays can be programmed using the serial SPI bus while RESET is pulled to GND. The serial interface consists of pins SCK, MOSI (input) and MISO (output). See Figure 53. After RESET is set low, the Programming Enable instruction needs to be executed first before program/erase instructions can be executed.

Figure 53. Serial Programming and Verify
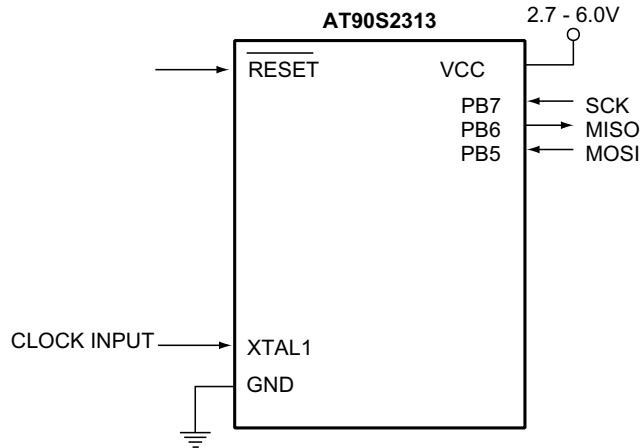
For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction and there is no need to first execute the Chip Erase instruction. The Chip Erase instruction turns the content of every memory location in both the program and EEPROM arrays into $FF.

The program and EEPROM memory arrays have separate address spaces: $0000 to $03FF for program Flash memory and $000 to $07F for EEPROM data memory.

Either an external clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low: > 2 XTAL1 clock cycle

High: > 2 XTAL1 clock cycles

Serial Programming Algorithm

When writing serial data to the AT90S2313, data is clocked on the rising edge of SCK.

When reading data from the AT90S2313, data is clocked on the falling edge of SCK. See Figure 54, Figure and Table 29 for timing details.

To program and verify the AT90S2313 in the Serial Programming mode, the following sequence is recommended (See 4-byte instruction formats in Table 28):

1. Power-up sequence:

    Apply power between V_{CC} and GND while RESET and SCK are set to "0". If a crystal is not connected across pins XTAL1 and XTAL2, apply a clock signal to the XTAL1 pin. In some systems, the programmer cannot guarantee that SCK is held low during Power-up. In this case, RESET must be given a positive pulse of at least two XTAL1 cycles duration after SCK has been set to "0".

2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to the MOSI (PB5) pin.

3. The serial programming instructions will not work if the communication is out of synchronization. When in sync, the second byte ($53) will echo back when issu-

Electrical Characteristics

Absolute Maximum Ratings*

Operating Temperature.................................. -55°C to +125°C
Storage Temperature .... -65°C to +150°C
Voltage on Any Pin Except $\overline{\text{RESET}}$ with Respect to Ground ....-1.0V to V_{CC}+0.5V
Voltage on $\overline{\text{RESET}}$ with Respect to Ground ....-1.0V to +13.0V
Maximum Operating Voltage 6.6V
DC Current per I/O Pin .... 40.0 mA
DC Current V_{CC} and GND Pins .... 200.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.7V to 6.0V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	(Except XTAL1)	-0.5		0.3 V_{CC}[(1)]	V
V_{IL1}	Input Low Voltage	(XTAL1)	-0.5		0.3 V_{CC}[(1)]	V
V_{IH}	Input High Voltage	(Except XTAL1, $\overline{\text{RESET}}$)	0.6 V_{CC}[(2)]		V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1)	0.7 V_{CC}[(2)]		V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	($\overline{\text{RESET}}$)	0.85 V_{CC}[(2)]		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage[(3)] (Ports B, D)	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.6 0.5	V V
V_{OH}	Output High Voltage[(4)] (Ports B, D)	I_{OH} = -3 mA, V_{CC} = 5V I_{OH} = -1.5 mA, V_{CC} = 3V	4.3 2.3			V V
I_{IL}	Input Leakage Current I/O pin	V_{CC} = 6V, pin low (absolute value)			1.5	µA
I_{IH}	Input Leakage Current I/O pin	V_{CC} = 6V, pin high (absolute value)			980.0	nA
RRST	Reset Pull-up Resistor		100.0		500.0	kΩ
$R_{I/O}$	I/O Pin Pull-up Resistor		35.0		120.0	kΩ
I_{CC}	Power Supply Current	Active Mode, V_{CC} = 3V, 4 MHz			3.0	mA
		Idle Mode V_{CC} = 3V, 4 MHz			1.0	mA
I_{CC}	Power-down Mode[(5)]	WDT enabled, V_{CC} = 3V		9.0	15.0	µA
		WDT disabled, V_{CC} = 3V		<1.0	2.0	µA
V_{ACIO}	Analog Comparator Input Offset Voltage	V_{CC} = 5V V_{in} = V_{CC}/2			40.0	mV
I_{ACLK}	Analog Comparator Input Leakage Current	V_{CC} = 5V V_{in} = V_{CC}/2	-50.0		50.0	nA
t_{ACPD}	Analog Comparator Propagation Delay	V_{CC} = 2.7V V_{CC} = 4.0V		750.0 500.0		ns

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Instruction Set Summary

Mnemonic	Operands	Description	Operation	Flags	# Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add Two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry Two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl, K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract Two Registers	Rd ← Rd – Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd – K	Z,C,N,V,H	1
SBIW	Rdl, K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl – K	Z,C,N,V,S	2
SBC	Rd, Rr	Subtract with Carry Two Registers	Rd ← Rd – Rr – C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd – K – C	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← $FF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← $00 – Rd	Z,C,N,V,H	1
SBR	Rd, K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd, K	Clear Bit(s) in Register	Rd ← Rd • ($FF – K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← $FF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd, Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2
CP	Rd, Rr	Compare	Rd – Rr	Z,N,V,C,H	1
CPC	Rd, Rr	Compare with Carry	Rd – Rr – C	Z,N,V,C,H	1
CPI	Rd, K	Compare Register with Immediate	Rd – K	Z,N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1/2
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1/2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b) = 0) PC ← PC + 2 or 3	None	1/2
SBIS	P, b	Skip if Bit in I/O Register is Set	if (R(b) = 1) PC ← PC + 2 or 3	None	1/2
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V = 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less than Zero, Signed	if (N ⊕ V = 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half-carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half-carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T-Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T-Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2

20S

20S, 20-lead, Plastic Gull Wing Small
Outline (SOIC), 0.300" body.
Dimensions in Millineters and (Inches)*
JEDEC STANDARD MS-013

0.51(0.020)
0.33(0.013)

PIN 1 ID

7.60 (0.2992)   10.65 (0.419)
7.40 (0.2914)   10.00 (0.394)

PIN 1

1.27 (0.050) BSC

13.00 (0.5118)
12.60 (0.4961)

2.65 (0.1043)
2.35 (0.0926)

0.30(0.0118)
0.10 (0.0040)

0º ~ 8º

0.32 (0.0125)
0.23 (0.0091)

1.27 (0.050)
0.40 (0.016)

*Controlling dimension: Inches

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