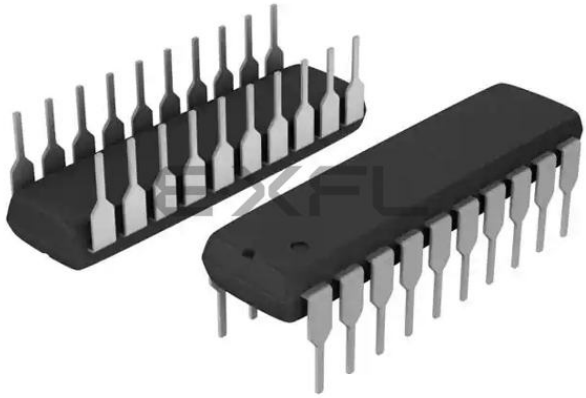

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

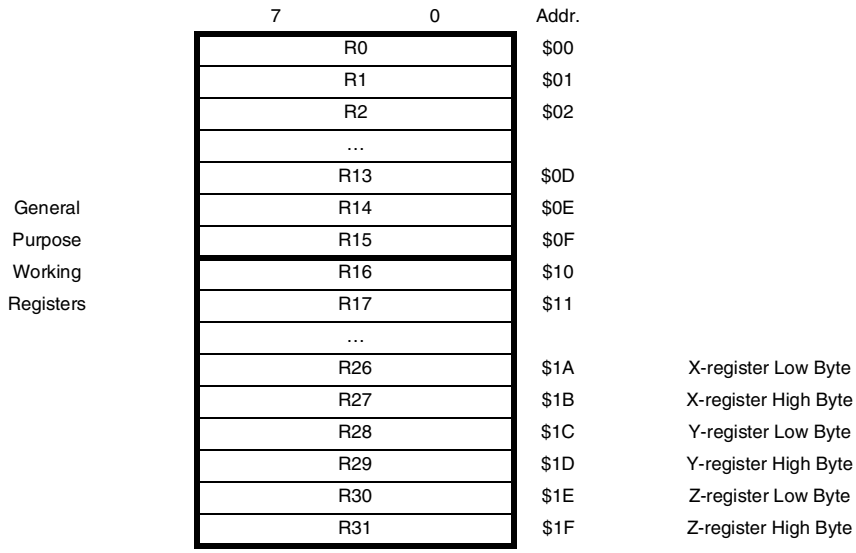
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 15 |
| Program Memory Size | 2KB (1K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 128 x 8 |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C |
| Mounting Type | Through Hole |
| Package / Case | 20-DIP (0.300", 7.62mm) |
| Supplier Device Package | 20-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at90s2313-4pc |

## General Purpose Register File

Figure 6 shows the structure of the 32 general purpose registers in the CPU.

**Figure 6.** AVR CPU General Purpose Working Registers



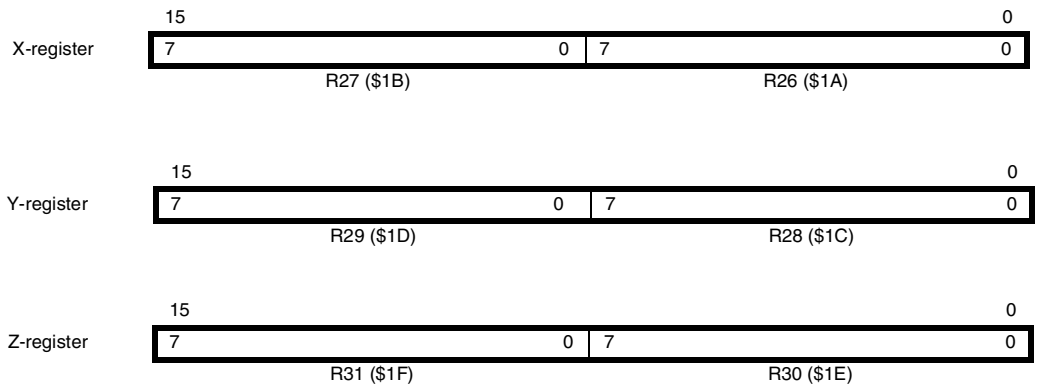

All the register operating instructions in the instruction set have direct and single-cycle access to all registers. The only exception is the five constant arithmetic and logic instructions SBCI, SUBI, CPI, ANDI, ORI between a constant and a register and the LDI instruction for load immediate constant data. These instructions apply to the second half of the registers in the Register File (R16..R31). The general SBC, SUB, CP, AND, OR, and all other operations between two registers or on a single register apply to the entire Register File.

As shown in Figure 6, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although the Register File is not physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-registers can be set to index any register in the file.

### X-register, Y-register, and Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are the address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y and Z are defined in Figure 7.

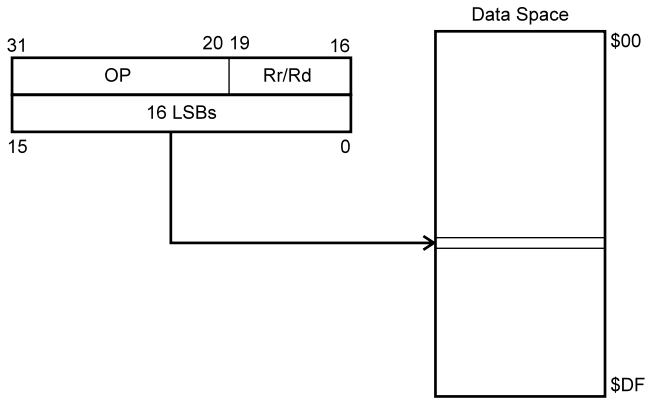
**Figure 7.** X-, Y-, and Z-Registers



Operand address is contained in 6 bits of the instruction word. n is the destination or source register address.

**Data Direct**

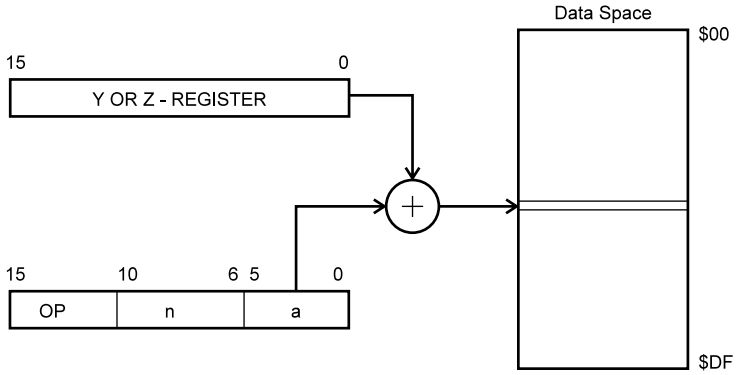
**Figure 12.** Direct Data Addressing




A 16-bit data address is contained in the 16 LSBs of a 2-word instruction. Rd/Rr specify the destination or source register.

**Data Indirect with Displacement**

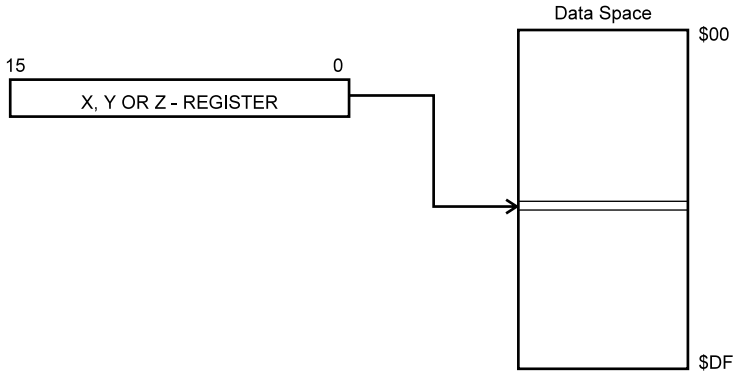
**Figure 13.** Data Indirect with Displacement




Operand address is the result of the Y- or Z-register contents added to the address contained in 6 bits of the instruction word.

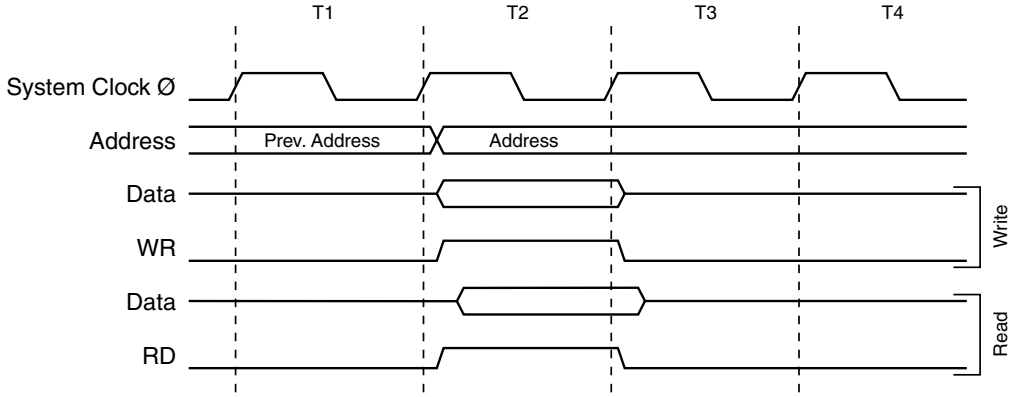
**Data Indirect**

**Figure 14.** Data Indirect Addressing




Operand address is the contents of the X-, Y-, or Z-register.

**Figure 22.** On-chip Data SRAM Access Cycles




## I/O Memory

The I/O space definition of the AT90S2313 is shown in Table 1.

**Table 1.** AT90S2313 I/O Space[1]

| Address Hex | Name | Function |
|---|---|---|
| $3F ($5F) | SREG | Status Register |
| $3D ($5D) | SPL | Stack Pointer Low |
| $3B ($5B) | GIMSK | General Interrupt MaSK Register |
| $3A ($5A) | GIFR | General Interrupt Flag Register |
| $39 ($59) | TIMSK | Timer/Counter Interrupt MaSK Register |
| $38 ($58) | TIFR | Timer/Counter Interrupt Flag Register |
| $35 ($55) | MCUCR | MCU general Control Register |
| $33 ($53) | TCCR0 | Timer/Counter 0 Control Register |
| $32 ($52) | TCNT0 | Timer/Counter 0 (8-bit) |
| $2F ($4F) | TCCR1A | Timer/Counter 1 Control Register A |
| $2E ($4E) | TCCR1B | Timer/Counter 1 Control Register B |
| $2D ($4D) | TCNT1H | Timer/Counter 1 High Byte |
| $2C ($4C) | TCNT1L | Timer/Counter 1 Low Byte |
| $2B ($4B) | OCR1AH | Output Compare Register 1 High Byte |
| $2A ($4A) | OCR1AL | Output Compare Register 1 Low Byte |
| $25 ($45) | ICR1H | T/C 1 Input Capture Register High Byte |
| $24 ($44) | ICR1L | T/C 1 Input Capture Register Low Byte |
| $21 ($41) | WDTCR | Watchdog Timer Control Register |
| $1E ($3E) | EEAR | EEPROM Address Register |
| $1D ($3D) | EEDR | EEPROM Data Register |
| $1C ($3C) | EECR | EEPROM Control Register |
| $18 ($38) | PORTB | Data Register, Port B |
| $17 ($37) | DDRB | Data Direction Register, Port B |
| $16 ($36) | PINB | Input Pins, Port B |

**Table 1.** AT90S2313 I/O Space[1] (Continued)

| Address Hex | Name | Function |
|---|---|---|
| $12 ($32) | PORTD | Data Register, Port D |
| $11 ($31) | DDRD | Data Direction Register, Port D |
| $10 ($30) | PIND | Input Pins, Port D |
| $0C ($2C) | UDR | UART I/O Data Register |
| $0B ($2B) | USR | UART Status Register |
| $0A ($2A) | UCR | UART Control Register |
| $09 ($29) | UBRR | UART Baud Rate Register |
| $08 ($28) | ACSR | Analog Comparator Control and Status Register |

Note: 1. Reserved and unused locations are not shown in the table.

All AT90S2313 I/O and peripherals are placed in the I/O space. The I/O locations are accessed by the IN and OUT instructions transferring data between the 32 general purpose working registers and the I/O space. I/O Registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set section for more details. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O Registers as SRAM, $20 must be added to this address. All I/O Register addresses throughout this document are shown with the SRAM address in parentheses.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the Status Flags are cleared by writing a logical “1” to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a “1” back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

The I/O and peripherals control registers are explained in the following sections.

### Status Register – SREG

The AVR Status Register (SREG) at I/O space location $3F ($5F) is defined as:

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $3F ($5F) | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** | **SREG** |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**• Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set (one) for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable bit is cleared (zero), none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts.

**• Bit 6 – T: Bit Copy Storage**

The Bit Copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source and destination for the operated bit. A bit from a register in the Register File can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the Register File by the BLD instruction.

### General Interrupt FLAG Register – GIFR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $3A ($5A) | INTF1 | INTF0 | – | – | – | – | – | – | GIFR |
| Read/Write | R/W | R/W | R | R | R | R | R | R | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**• Bit 7 – INTF1: External Interrupt Flag1**

When an edge on the INT1 pin triggers an interrupt request, the corresponding Interrupt Flag, INTF1, becomes set (one). If the I-bit in SREG and the corresponding interrupt enable bit, INT1 bit in GIMSK, are set (one), the MCU will jump to the Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical “1” to it. The flag is always cleared when INT1 is configured as level interrupt.

**• Bit 6 – INTF0: External Interrupt Flag0**

When an edge on the INT0 pin triggers an interrupt request, the corresponding Interrupt Flag, INTF0, becomes set (one). If the I-bit in SREG and the corresponding interrupt enable bit, INT0 bit in GIMSK, are set (one), the MCU will jump to the Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical “1” to it. The flag is always cleared when INT0 is configured as level interrupt.

**• Bits 5..0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S2313 and always read as zero.

Note that external level interrupt does not have a flag, and will only be remembered for as long as the interrupt condition is active.

### Timer/Counter Interrupt Mask Register – TIMSK

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $39 ($59) | TOIE1 | OCIE1A | – | – | TICIE1 | – | TOIE0 | – | TIMSK |
| Read/Write | R/W | R/W | R | R | R/W | R | R/W | R | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**• Bit 7 – TOIE1: Timer/Counter1 Overflow Interrupt Enable**

When the TOIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Overflow Interrupt is enabled. The corresponding interrupt (at vector $005) is executed if an overflow in Timer/Counter1 occurs (i.e., when the TOV1 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

**• Bit 6 – OCIE1A: Timer/Counter1 Output Compare Match Interrupt Enable**

When the OCIE1A bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Compare Match Interrupt is enabled. The corresponding interrupt (at vector $004) is executed if a compare match in Timer/Counter1 occurs (i.e., when the OCF1A bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

**• Bit 5,4 – Res: Reserved Bits**

These bits are reserved bits in the AT90S2313 and always read as zero.

**• Bit 2 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S2313 and always reads as zero.

**• Bit 1 – TOV0: Timer/Counter0 Overflow Flag**

The bit TOV0 is set (one) when an overflow occurs in Timer/Counter0. TOV0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV0 is cleared by writing a logical "1" to the flag. When the SREG I-bit and TOIE0 (Timer/Counter0 Overflow Interrupt Enable) and TOV0 are set (one), the Timer/Counter0 Overflow Interrupt is executed.

**• Bit 0 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S2313 and always reads as zero.

## External Interrupts

The External Interrupts are triggered by the INT1 and INT0 pins. Observe that, if enabled, the interrupts will trigger even if the INT0/INT1 pins are configured as outputs. This feature provides a way of generating a software interrupt. The External Interrupts can be triggered by a falling or rising edge or a low level. This is set up as indicated in the specification for the MCU Control Register (MCUCR). When the External Interrupt is enabled and is configured as level-triggered, the interrupt will trigger as long as the pin is held low.

The External Interrupts are set up as described in the specification for the MCU Control Register (MCUCR).

## Interrupt Response Time

The interrupt execution response for all the enabled AVR interrupts is four clock cycles, minimum. Four clock cycles after the Interrupt Flag has been set, the Program Vector address for the actual interrupt handling routine is executed. During this four clock cycle period, the Program Counter (two bytes) is pushed onto the Stack, and the Stack Pointer is decremented by two. The Power-down is normally a relative jump to the interrupt routine, and this jump takes two clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter (two bytes) is popped back from the Stack, the Stack Pointer is incremented by two, and the I-flag in SREG is set. When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

## MCU Control Register – MCUCR

The MCU Control Register contains control bits for general MCU functions.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $35 ($55) | – | – | SE | SM | ISC11 | ISC10 | ISC01 | ISC00 | MCUCR |
| Read/Write | R | R | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**• Bits 7, 6 – Res: Reserved Bits**

These bits are reserved bits in the AT90S2313 and always read as zero.

**• Bit 5 – SE: Sleep Enable**

The SE bit must be set (one) to make the MCU enter the sleep mode when the SLEEP instruction is executed. To avoid the MCU entering the sleep mode unless it is the programmer's purpose, it is recommended to set the Sleep Enable (SE) bit just before the execution of the SLEEP instruction.

**• Bit 4 – SM: Sleep Mode**

This bit selects between the two available sleep modes. When SM is cleared (zero), Idle mode is selected as sleep mode. When SM is set (one), Power-down mode is selected as sleep mode. For details, refer to the paragraph “Sleep Modes”.

**• Bits 3, 2 – ISC11, ISC10: Interrupt Sense Control 1 Bit 1 and Bit 0**

The External Interrupt 1 is activated by the external pin INT1 if the SREG I-flag and the corresponding interrupt mask in the GIMSK Register is set. The level and edges on the external INT1 pin that activate the interrupt are defined in Table 5.

**Table 5.** Interrupt 1 Sense Control

| ISC11 | ISC10 | Description |
|---|---|---|
| 0 | 0 | The low level of INT1 generates an interrupt request. |
| 0 | 1 | Reserved |
| 1 | 0 | The falling edge of INT1 generates an interrupt request. |
| 1 | 1 | The rising edge of INT1 generates an interrupt request. |

**• Bits 1, 0 – ISC01, ISC00: Interrupt Sense Control 0 Bit 1 and Bit 0**

The External Interrupt 0 is activated by the external pin INT0 if the SREG I-flag and the corresponding interrupt mask is set. The level and edges on the external INT0 pin that activate the interrupt are defined in Table 6.

**Table 6.** Interrupt 0 Sense Control

| ISC01 | ISC00 | Description |
|---|---|---|
| 0 | 0 | The low level of INT0 generates an interrupt request. |
| 0 | 1 | Reserved |
| 1 | 0 | The falling edge of INT0 generates an interrupt request. |
| 1 | 1 | The rising edge of INT0 generates an interrupt request. |

The value on the INTn pin is sampled before detecting edges. If edge interrupt is selected, pulses with a duration longer than one CPU clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low-level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt. If enabled, a level-triggered interrupt will generate an interrupt request as long as the pin is held low.

## Sleep Modes

To enter the sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU awakes, executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the Register File, SRAM and I/O memory are unaltered. If a Reset occurs during sleep mode, the MCU wakes up and executes from the Reset Vector.

### Idle Mode

When the SM bit is cleared (zero), the SLEEP instruction forces the MCU into the Idle mode, stopping the CPU but allowing Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like Timer Overflow interrupt and Watchdog Reset. If wake-up from the Analog Comparator Interrupt is not required, the Analog Comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status Register (ACSR). This will reduce power consumption in Idle mode. When the MCU wakes up from Idle mode, the CPU starts program execution immediately.

### Power-down Mode

When the SM bit is set (one), the SLEEP instruction forces the MCU into the Power-down mode. In this mode, the external Oscillator is stopped while the external interrupts and the Watchdog (if enabled) continue operating. Only an External Reset, a Watchdog Reset (if enabled), an external level interrupt on INT0 or INT1 can wake up the MCU.

Note that when a level-triggered interrupt is used for wake-up from Power-down, the low level must be held for a time longer than the reset delay Time-out period $t_{TOUT}$. Otherwise, the device will not wake up.

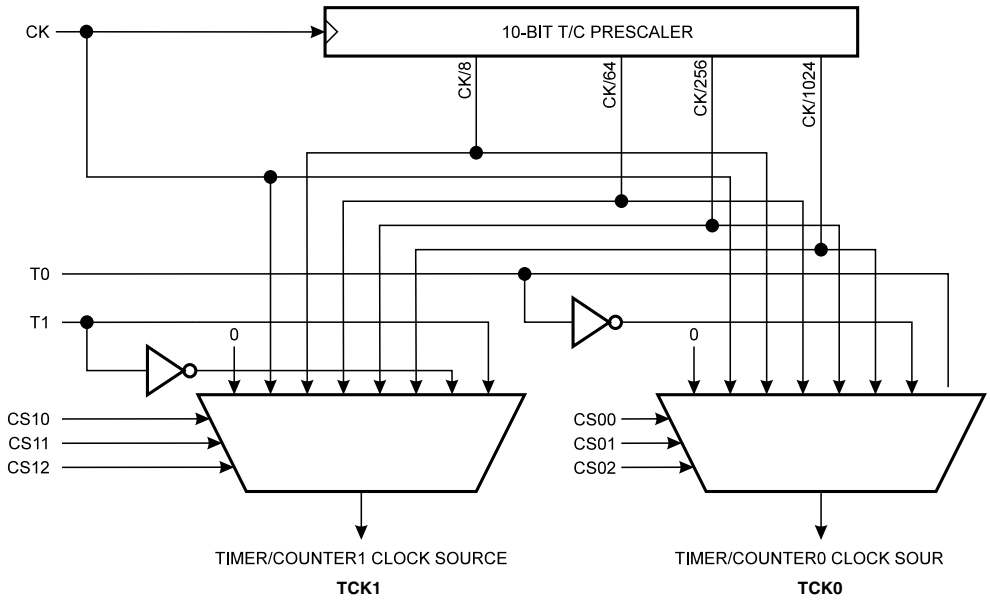
## Timer/Counters

The AT90S2313 provides two general purpose Timer/Counters – one 8-bit T/C and one 16-bit T/C. The Timer/Counters have individual prescaling selection from the same 10-bit prescaling timer. Both Timer/Counters can either be used as a timer with an internal clock time base or as a counter with an external pin connection that triggers the counting.

## Timer/Counter Prescaler

Figure 28 shows the general Timer/Counter prescaler.

**Figure 28.** Timer/Counter Prescaler



The TEMP Register is also used when accessing TCNT1 and OCR1A. If the main program and interrupt routines perform access to registers using TEMP, interrupts must be disabled during access from the main program or interrupts if interrupts are re-enabled.

### Timer/Counter1 in PWM Mode

When the PWM mode is selected, Timer/Counter1 and the Output Compare Register1 (OCR1A) form an 8-, 9-, or 10-bit, free-running, glitch-free and phase-correct PWM with output on the PB3(OC1) pin. Timer/Counter1 acts as an up/down counter, counting up from $0000 to TOP (see Table 11), where it turns and counts down again to zero before the cycle is repeated. When the counter value matches the contents of the 8, 9 or 10 least significant bits of OCR1A, the PB3(OC1) pin is set or cleared according to the settings of the COM1A1 and COM1A0 bits in the Timer/Counter1 Control Register (TCCR1). Refer to Table 12 for details.

**Table 11.** Timer TOP Values and PWM Frequency

| PWM Resolution | Timer TOP Value | Frequency |
|---|---|---|
| 8-bit | $00FF (255) | $f_{TC1}/510$ |
| 9-bit | $01FF (511) | $f_{TC1}/1022$ |
| 10-bit | $03FF(1023) | $f_{TC1}/2046$ |

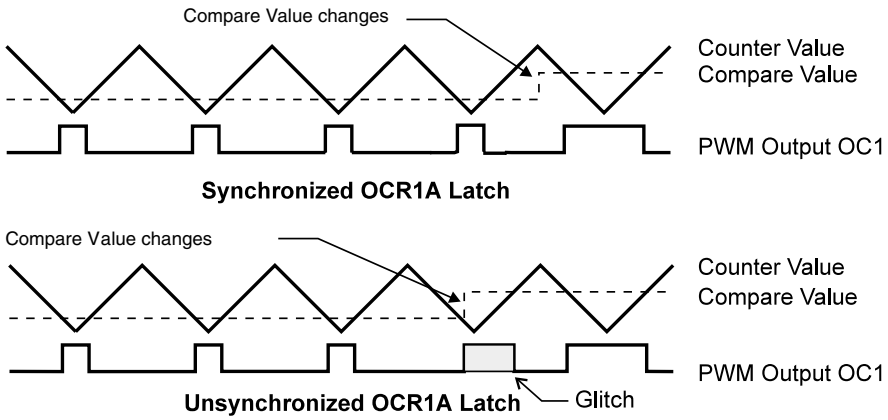
**Table 12.** Compare1 Mode Select in PWM Mode(1)

| COM1A1 | COM1A0 | Effect on OC1 |
|---|---|---|
| 0 | 0 | Not connected |
| 0 | 1 | Not connected |
| 1 | 0 | Cleared on compare match, upcounting. Set on compare match, down-counting (non-inverted PWM). |
| 1 | 1 | Cleared on compare match, downcounting. Set on compare match, up-counting (inverted PWM). |

Note: 1. The initial state of the OC1 output line is undefined.

Note that in the PWM mode, the 10 least significant OCR1A bits, when written, are transferred to a temporary location. They are latched when Timer/Counter1 reaches TOP. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR1A write. See Figure 32 for an example.

**Figure 32.** Effects on Unsynchronized OCR1 Latching



**• Bit 5 – ACO: Analog Comparator Output**

ACO is directly connected to the comparator output.

**• Bit 4 – ACI: Analog Comparator Interrupt Flag**

This bit is set (one) when a comparator output event triggers the interrupt mode defined by ACIS1 and ACIS0. The Analog Comparator Interrupt routine is executed if the ACIE bit is set (one) and the I-bit in SREG is set (one). ACI is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logical “1” to the flag. Observe, however, that if another bit in this register is modified using the SBI or CBI instruction, ACI will be cleared if it has become set before the operation.

**• Bit 3 – ACIE: Analog Comparator Interrupt Enable**

When the ACIE bit is set (one) and the I-bit in the Status Register is set (one), the Analog Comparator interrupt is activated. When cleared (zero), the interrupt is disabled.

**• Bit 2 – ACIC: Analog Comparator Input Capture Enable**

When set (one), this bit enables the Input Capture function in Timer/Counter1 to be triggered by the Analog Comparator. The comparator output is, in this case, directly connected to the Input Capture front-end logic, making the comparator utilize the noise canceler and edge-select features of the Timer/Counter1 Input Capture interrupt. When cleared (zero), no connection between the Analog Comparator and the Input Capture function is given. To make the comparator trigger the Timer/Counter1 Input Capture interrupt, the TICIE1 bit in the Timer Interrupt Mask Register (TIMSK) must be set (one).

**• Bits 1,0 – ACIS1, ACIS0: Analog Comparator Interrupt Mode Select**

These bits determine which comparator events trigger the Analog Comparator interrupt. The different settings are shown in Table 16.

**Table 16.** ACIS1/ACIS0 Settings[1]

| ACIS1 | ACIS0 | Interrupt Mode |
|---|---|---|
| 0 | 0 | Comparator Interrupt on Output Toggle |
| 0 | 1 | Reserved |
| 1 | 0 | Comparator Interrupt on Falling Output Edge |
| 1 | 1 | Comparator Interrupt on Rising Output Edge |

Note: 1. When changing the ACIS1/ACIS0 bits, the Analog Comparator Interrupt must be disabled by clearing its Interrupt Enable bit in the ACSR Register. Otherwise an interrupt can occur when the bits are changed.

## I/O Ports

All AVR ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

## Port B

Port B is an 8-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port B, one each for the Data Register – PORTB, $18 ($38), Data Direction Register – DDRB, $17($37) and the Port B Input Pins – PINB, $16($36). The Port B Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in Table 17.

**Table 17.** Port B Pin Alternate Functions

| Port Pin | Alternate Functions |
|---|---|
| PB0 | AIN0 (Analog Comparator positive input) |
| PB1 | AIN1 (Analog Comparator negative input) |
| PB3 | OC1 (Timer/Counter1 Output Compare Match output) |
| PB5 | MOSI (Data input line for memory downloading) |
| PB6 | MISO (Data output line for memory uploading) |
| PB7 | SCK (Serial clock input) |

When the pins are used for the alternate function, the DDRB and PORTB Registers have to be set according to the alternate function description.

### Port B Data Register – PORTB

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $18 ($38) | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | PORTB |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

### Port B Data Direction Register – DDRB

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $17 ($37) | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | DDRB |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

### Port B Input Pins Address – PINB

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $16 ($36) | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | PINB |
| Read/Write | R | R | R | R | R | R | R | R | |
| Initial value | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | |

**Port B Schematics**

Note that all port pins are synchronized. The synchronization latches are, however, not shown in the figures.

**Figure 38.** Port B Schematic Diagram (Pins PB0 and PB1)

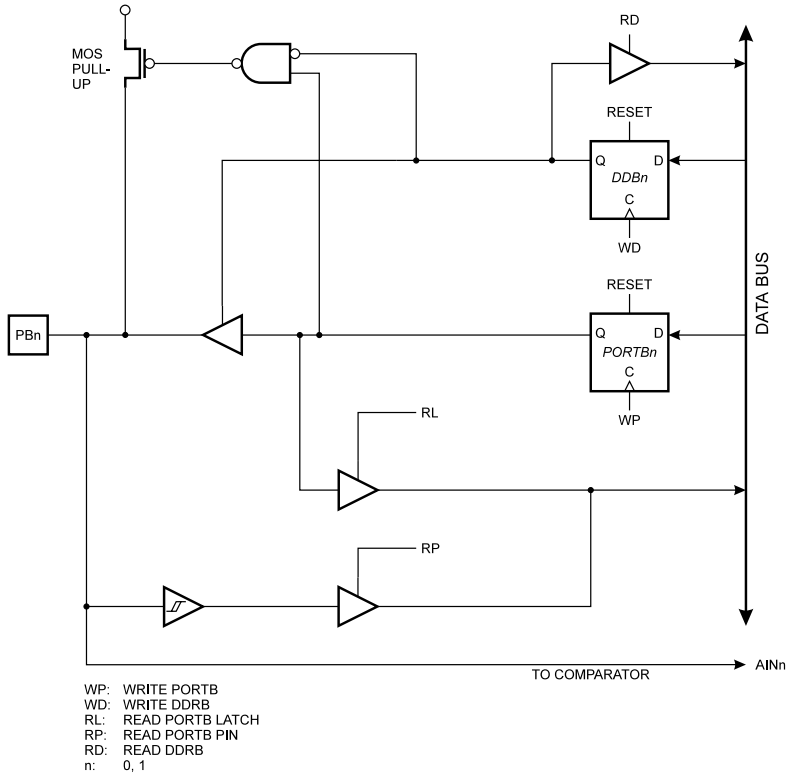


**Figure 47.** Port D Schematic Diagram (Pins PD4 and PD5)

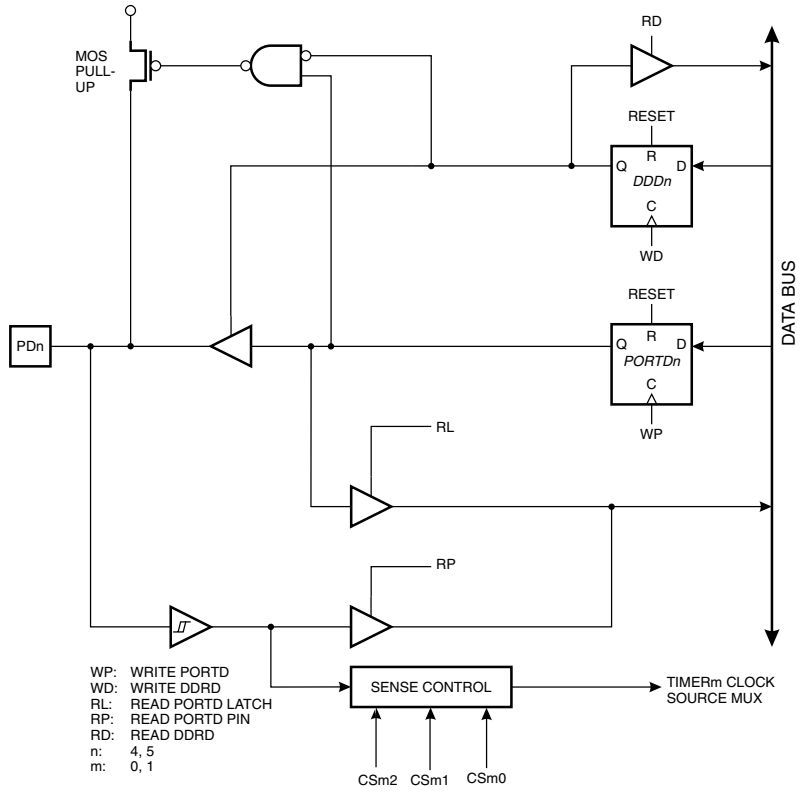
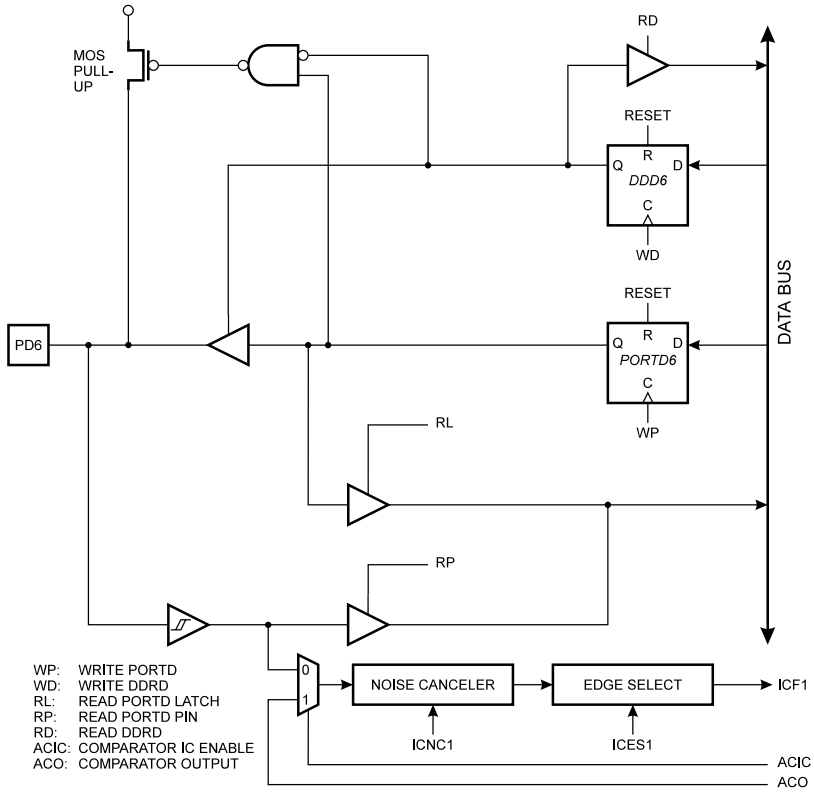



**Figure 48.** Port D Schematic Diagram (Pin PD6)



# Memory Programming

## Program and Data Memory Lock Bits

The AT90S2313 MCU provides two Lock bits that can be left unprogrammed ("1") or can be programmed ("0") to obtain the additional features listed in Table 21. The Lock bits can only be erased with the Chip Erase operation.

**Table 21.** Lock Bit Protection Modes

| Memory Lock Bits | | | |
|---|---|---|---|
| **Mode** | **LB1** | **LB2** | **Protection Type** |
| 1 | 1 | 1 | No memory lock features enabled. |
| 2 | 0 | 1 | Further programming of the Flash and EEPROM is disabled.(1) |
| 3 | 0 | 0 | Same as mode 2, and verify is also disabled. |

Note: 1. In the Parallel mode, further programming of the Fuse bits are also disabled. Program the Fuse bits before programming the Lock bits.

## Fuse Bits

The AT90S2313 has two Fuse bits: SPIEN and FSTRT.

- When the SPIEN Fuse is programmed ("0"), Serial Program and Data Downloading is enabled. The default value is programmed ("0").
- When the FSTRT Fuse is programmed ("0"), the short start-up time is selected. The default value is unprogrammed ("1"). Parts with this bit pre-programmed ("0") can be delivered on demand.

The Fuse bits are not accessible in Serial Programming mode. The status of the fuses are not affected by Chip Erase.

## Signature Bytes

All Atmel microcontrollers have a 3-byte signature code that identifies the device. This code can be read in both serial and parallel mode. The three bytes reside in a separate address space.

For the AT90S2313(1) they are:

1. $000: $1E (indicates manufactured by Atmel).
2. $001: $91 (indicates 2 Kb Flash memory).
3. $002: $01 (indicates AT90S2313 device when signature byte $001 is $91).

Note: 1. When both Lock bits are programmed (Lock mode 3), the signature bytes cannot be read in serial mode. Reading the signature bytes will return: $00, $01 and $02.

## Programming the Flash and EEPROM

Atmel's AT90S2313 offers 2K bytes of In-System Reprogrammable Flash Program memory and 128 bytes of EEPROM Data memory.

The AT90S2313 is shipped with the On-chip Flash Program and EEPROM Data memory arrays in the erased state (i.e., contents = $FF) and ready to be programmed. This device supports a high-voltage (12V) Parallel Programming mode and a low-voltage Serial Programming mode. The +12V is used for programming enable only, and no current of significance is drawn by this pin. The Serial Programming mode provides a convenient way to download program and data into the AT90S2313 inside the user's system.

The program and EEPROM memory arrays in the AT90S2313 are programmed byte-by-byte in either programming mode. For the EEPROM, an auto-erase cycle is provided

# Electrical Characteristics

## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin Except $\overline{\text{RESET}}$ with Respect to Ground | -1.0V to $V_{CC}$+0.5V |
| Voltage on $\overline{\text{RESET}}$ with Respect to Ground | -1.0V to +13.0V |
| Maximum Operating Voltage | 6.6V |
| DC Current per I/O Pin | 40.0 mA |
| DC Current $V_{CC}$ and GND Pins | 200.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

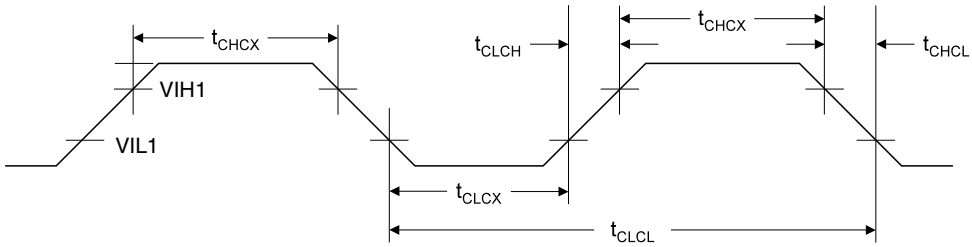
$T_A$ = -40°C to 85°C, $V_{CC}$ = 2.7V to 6.0V (unless otherwise noted)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | (Except XTAL1) | -0.5 | | 0.3 $V_{CC}$(1) | V |
| $V_{IL1}$ | Input Low Voltage | (XTAL1) | -0.5 | | 0.3 $V_{CC}$(1) | V |
| $V_{IH}$ | Input High Voltage | (Except XTAL1, $\overline{\text{RESET}}$) | 0.6 $V_{CC}$(2) | | $V_{CC}$ + 0.5 | V |
| $V_{IH1}$ | Input High Voltage | (XTAL1) | 0.7 $V_{CC}$(2) | | $V_{CC}$ + 0.5 | V |
| $V_{IH2}$ | Input High Voltage | ($\overline{\text{RESET}}$) | 0.85 $V_{CC}$(2) | | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage(3) (Ports B, D) | $I_{OL}$ = 20 mA, $V_{CC}$ = 5V<br>$I_{OL}$ = 10 mA, $V_{CC}$ = 3V | | | 0.6<br>0.5 | V<br>V |
| $V_{OH}$ | Output High Voltage(4) (Ports B, D) | $I_{OH}$ = -3 mA, $V_{CC}$ = 5V<br>$I_{OH}$ = -1.5 mA, $V_{CC}$ = 3V | 4.3<br>2.3 | | | V<br>V |
| $I_{IL}$ | Input Leakage Current I/O pin | $V_{CC}$ = 6V, pin low (absolute value) | | | 1.5 | µA |
| $I_{IH}$ | Input Leakage Current I/O pin | $V_{CC}$ = 6V, pin high (absolute value) | | | 980.0 | nA |
| RRST | Reset Pull-up Resistor | | 100.0 | | 500.0 | kΩ |
| $R_{I/O}$ | I/O Pin Pull-up Resistor | | 35.0 | | 120.0 | kΩ |
| $I_{CC}$ | Power Supply Current | Active Mode, $V_{CC}$ = 3V, 4 MHz | | | 3.0 | mA |
| | | Idle Mode $V_{CC}$ = 3V, 4 MHz | | | 1.0 | mA |
| $I_{CC}$ | Power-down Mode(5) | WDT enabled, $V_{CC}$ = 3V | | 9.0 | 15.0 | µA |
| | | WDT disabled, $V_{CC}$ = 3V | | <1.0 | 2.0 | µA |
| $V_{ACIO}$ | Analog Comparator Input Offset Voltage | $V_{CC}$ = 5V<br>$V_{in}$ = $V_{CC}$/2 | | | 40.0 | mV |
| $I_{ACLK}$ | Analog Comparator Input Leakage Current | $V_{CC}$ = 5V<br>$V_{in}$ = $V_{CC}$/2 | -50.0 | | 50.0 | nA |
| $t_{ACPD}$ | Analog Comparator Propagation Delay | $V_{CC}$ = 2.7V<br>$V_{CC}$ = 4.0V | | 750.0<br>500.0 | | ns |

Notes:
1. “Max” means the highest value where the pin is guaranteed to be read as low.
2. “Min” means the lowest value where the pin is guaranteed to be read as high.
3. Although each I/O port can sink more than the test conditions (20 mA at $V_{CC}$ = 5V, 10 mA at $V_{CC}$ = 3V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all $I_{OL}$, for all ports, should not exceed 200 mA
   2] The sum of all $II_{OL}$, for port D0 - D5 and XTAL2 should not exceed 100 mA.
   3] The sum of all $I_{OL}$, for ports B0 - B7 and D6 should not exceed 100 mA.
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
4. Although each I/O port can source more than the test conditions (3 mA at $V_{CC}$ = 5V, 1.5 mA at $V_{CC}$ = 3V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all $I_{OH}$, for all ports, should not exceed 200 mA
   2] The sum of all $I_{OH}$, for port D0 - D5 and XTAL2 should not exceed 100 mA.
   3] The sum of all $I_{OH}$, for ports B0 - B7 and D6 should not exceed 100 mA.
   If $I_{OH}$ exceeds the test condition, $V_{OH}$ may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
5. Minimum $V_{CC}$ for Power-down is 2V.

## External Clock Drive Waveforms

**Figure 56.** External Clock




## External Clock Drive

| Symbol | Parameter | $V_{CC}$ = 2.7V to 6.0V | | $V_{CC}$ = 4.0V to 6.0V | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 4 | 0 | 10.0 | MHz |
| $t_{CLCL}$ | Clock Period | 250.0 | | 100.0 | | ns |
| $t_{CHCX}$ | High Time | 100.0 | | 40.0 | | ns |
| $t_{CLCX}$ | Low Time | 100.0 | | 40.0 | | ns |
| $t_{CLCH}$ | Rise Time | | 1.6 | | 0.5 | µs |
| $t_{CHCL}$ | Fall Time | | 1.6 | | 0.5 | µs |

**Figure 62.** Power-down Supply Current vs. $V_{CC}$

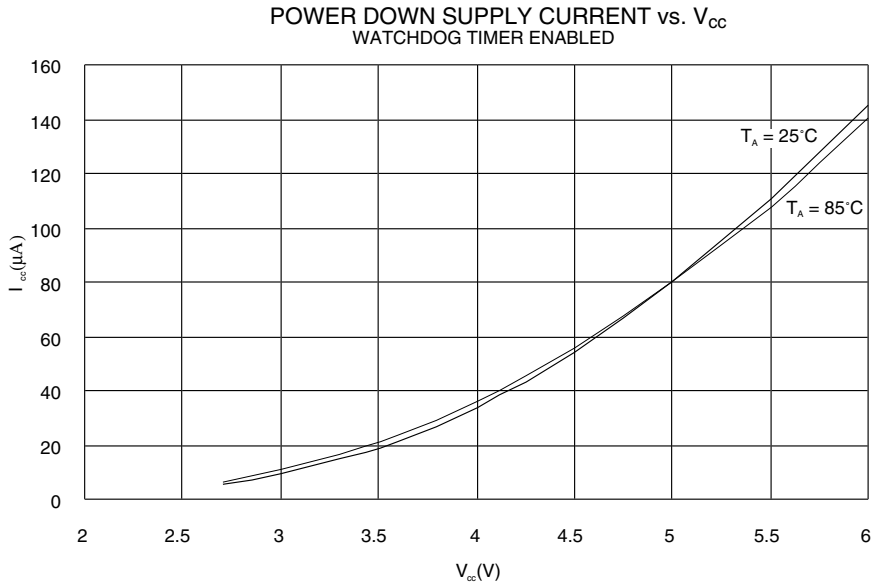
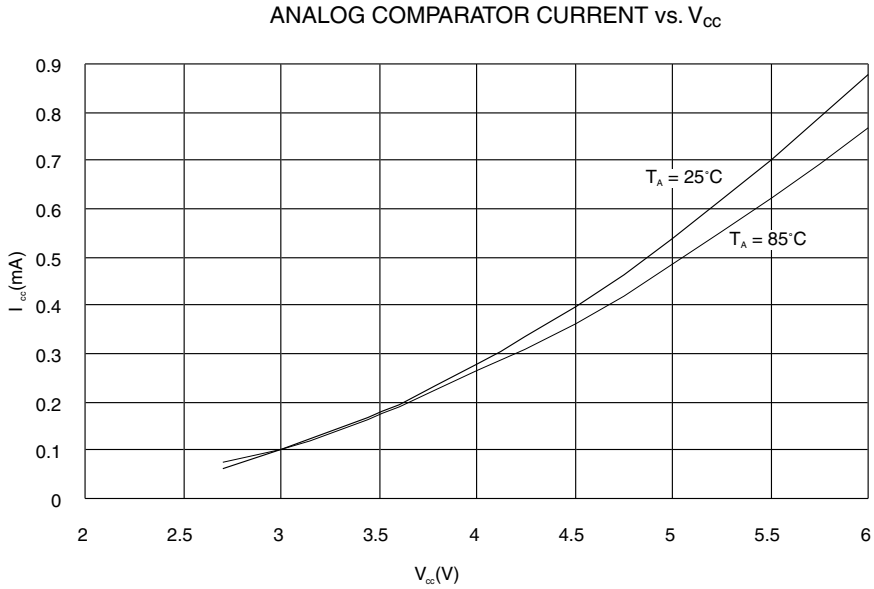



**Figure 63.** Analog Comparator Current vs. $V_{CC}$



Note: Sink and source capabilities of I/O ports are measured on one pin at a time.

**Figure 68.** Pull-up Resistor Current vs. Input Voltage

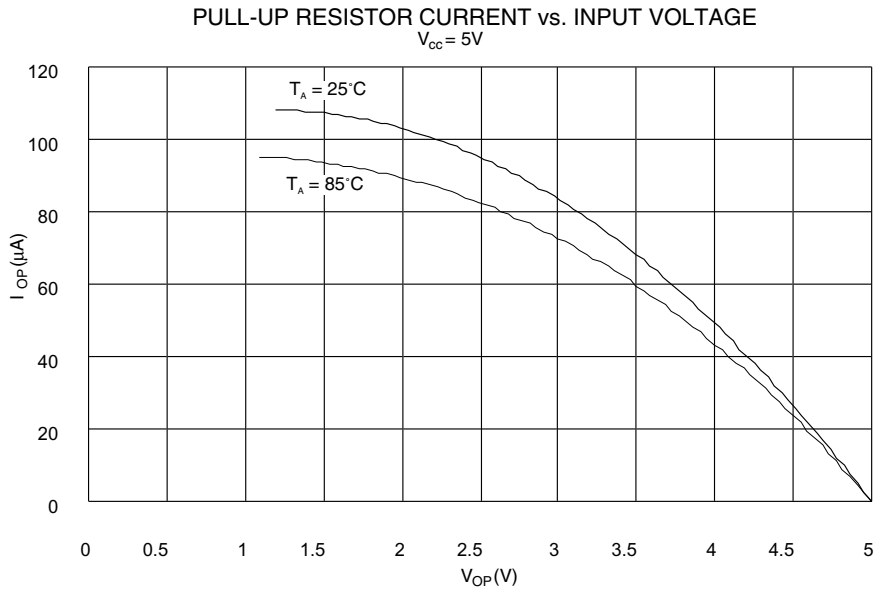
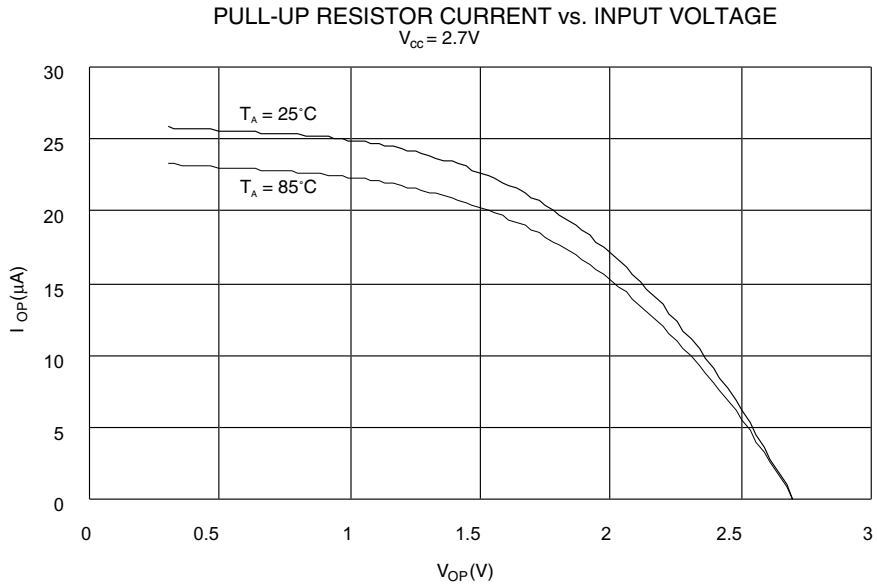



**Figure 69.** Pull-up Resistor Current vs. Input Voltage



## Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 4 | 2.7 - 6.0V | AT90S2313-4PC<br>AT90S2313-4SC | 20P3<br>20S | Commercial<br>(0°C to 70°C) |
| | | AT90S2313-4PI<br>AT90S2313-4SI | 20P3<br>20S | Industrial<br>(-40°C to 85°C) |
| 10 | 4.0 - 6.0V | AT90S2313-10PC<br>AT90S2313-10SC | 20P3<br>20S | Commercial<br>(0°C to 70°C) |
| | | AT90S2313-10PI<br>AT90S2313-10SI | 20P3<br>20S | Industrial<br>(-40°C to 85°C) |

| Package Type | |
|---|---|
| **20P3** | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| **20S** | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |

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