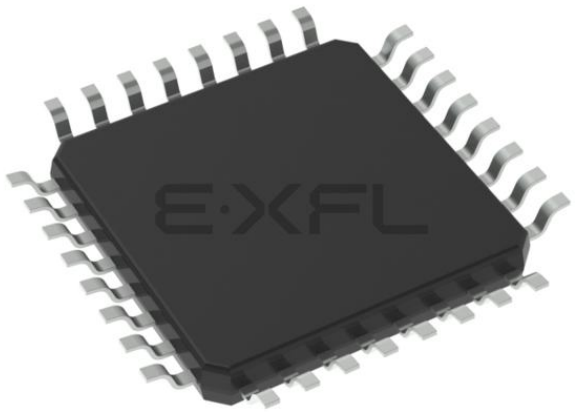

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml21e16b-aut

Important:
When an analog peripheral is enabled, the analog output of the peripheral will interfere with the alternative functions of the output pads. This is also true even when the peripheral is used for internal purposes.

Analog inputs do not interfere with alternative pad functions.

8.3. Reference Voltages

Some analog peripherals require a reference voltage for proper operation. Aside from external voltages (e.g., V_{DDANA}), the device provides has a DETREF module that provides two internal voltage references:

- BANDGAP: a stable voltage reference, fixed at 1V.
- INTREF: a variable voltage reference, configured by the Voltage References System Control register in the Supply Controller (SUPC.VREF).

The respective reference voltage source may be selected within the peripheral's registers:

- ADC: Reference Control register (ADC.REFCTRL)
- AC: Fixed to BANDGAP
- DAC: Reference Selection bits in the Control B register (DAC.CTRLB.REFSEL)

8.4. Analog ONDEMAND Function

General Function

The analog ONDEMAND feature allows other analog peripherals to request the OPAMP.
Note: The analog ONDEMAND is independent of the ONDEMAND bit located in each source clock controller, used for requesting source clocks.

The OPAMP can be enabled by requests from ADC or AC.

The request mechanism is activated by writing a '1' to the OPAMP.OPAMPCTRLx.ONDEMAND bit. When a request is sent by one of the peripherals to OPAMPx, the OPAMPx will start up and acknowledge the request as soon as it is fully enabled.

If the OPAMP.OPAMPCTRLx.ONDEMAND bit is '0' but OPAMPx is enabled already, a request will be immediately acknowledged. If OPAMPCTRLx.ONDEMAND=0 and the OPAMPx is disabled, requests will not be acknowledged: requests are handled only when the OPAMP output is active (OPAMPCTRLx.ANAOUT=1).

In Standby sleep mode, the ONDEMAND operation is still active if OPAMPCTRLx.ONDEMAND=1. If OPAMPCTRLx.ONDEMAND=0, the OPAMPx is disabled.

The OPAMP controller peripheral must be configured appropriately before being requested.

For the ADC peripheral, ONDEMAND requests to the OPAMP are enabled by writing the ADC.CTRLA.ONDEMAND bit to '1'.

For the AC peripheral,there is no explicit ONDEMAND bit in the registers. ONDEMAND requests to OPAMPx are issued either when the AC is used in single-shot mode, or when comparisons are triggered by events from the Event System. The OPAMP must be selected as input of the AC previously.

When the Negative Input MUX Selection bit field of the Comparator 1 Control register is set to DAC/OPAMP (AC.COMPCTRL1.MUXNEG=0x7), the AC will start issuing ONDEMAND requests to OPAMP.

Alternative Requests

When OPAMPx is set to accept ONDEMAND requests (OPAMP.OPAMCTRLx.ONDEMAND=1) but the ADC is not configured to issue requests to it (ADC.CTRLA.ONDEMAND=0), the ADC will send continuous requests to the receiver selected by ADC.INPUTCTRL.MUXPOS.

If ADC.INPUTCTRL.MUXPOS=0x1E, OPAMP0 and OPAMP1 will receive requests.

If ADC.INPUTCTRL.MUXPOS=0x1F, only OPAMP2 will receive requests.

When OPAMPx is set to accept ONDEMAND requests (OPAMP.OPAMCTRLx.ONDEMAND=1) but the AC is not configured to issue requests to it (AC.CTRLA.ONDEMAND=0), the AC will send continuous requests to the receiver selected by AC.COMPCTRLx.MUXNEG.

If AC.COMPCTRL1.MUXNEG=0x7, OPAMP2 will receive requests.

If AC.COMPCTRL0.MUXNEG=0x7, DAC0 will receive requests.

Related Links

OPAMP – Operational Amplifier Controller on page 1009
ADC – Analog-to-Digital Converter on page 1032
AC – Analog Comparators on page 1076

Table 12-9. HS SRAM Port Connections QoS

HS SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
MTB - Micro Trace Buffer	4	Direct	STATIC-3	0x3
USB - Universal Serial Bus	3	Direct	IP-QOSCTRL	0x3
HMATRIXLP - Low-Power Bus Matrix	2	Bus Matrix	0x44000934(1), bits[1:0]	0x2
DSU - Device Service Unit	1	Bus Matrix	0x4100201C(1)	0x2
CM0+ - Cortex M0+ Processor	0	Bus Matrix	0x41008114(1), bits[1:0]	0x3

Note:

1. Using 32-bit access only.

Table 12-10. LP SRAM Port Connections QoS

LP SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
DMAC - Direct Memory Access Controller - Write-Back Access	5, 6	Direct	IP-QOSCTRL.WRBQOS	0x2
DMAC - Direct Memory Access Controller - Fetch Access	3, 4	Direct	IP-QOSCTRL.FQOS	0x2
H2LBRIDGEM - HS to LP bus matrix AHB to AHB bridge	2	Bus Matrix	0x44000924(1), bits[1:0]	0x2
DMAC - Direct Memory Access Controller - Data Access	1	Bus Matrix	IP-QOSCTRL.DQOS	0x2

Note:

1. Using 32-bit access only.

18.8.12. APBE Mask

Name: APBEMASK
Offset: 0x24
Reset: 0x0000 000D
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	Reserved[30:23]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	Reserved[22:15]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	Reserved[14:7]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	Reserved[6:0]							PAC
Access	R	R	R	R	R	R	R	R/W
Reset	0	0	0	0	1	1	0	1

Bits 31:1 – Reserved[30:0]: For future use
Reserved bits are unused and reserved for future use. For compatibility with future devices, always write reserved bits to their reset value. If no reset value is given, write 0.

Bit 0 – PAC: PAC APBE Clock Enable

Value	Description
0	The APBE clock for the PAC is stopped.
1	The APBE clock for the PAC is enabled.

the internal memory for the active channel. For a new block transfer, the transfer descriptor will be fetched from the descriptor memory section (BASEADDR); For an ongoing block transfer, the descriptor will be fetched from the write-back memory section (WRBADDR). By using the data transfer bus, the DMAC will read the data from the current source address and write it to the current destination address. For further details on how the current source and destination addresses are calculated, refer to the section on Addressing.

The arbitration procedure is performed after each transfer. If the current DMA channel is granted access again, the block transfer counter (BTCNT) of the internal transfer descriptor will be decremented by the number of beats in a transfer, the optional output event Beat will be generated if configured and enabled, and the active channel will perform a new transfer. If a different DMA channel than the current active channel is granted access, the block transfer counter value will be written to the write-back section before the transfer descriptor of the newly granted DMA channel is fetched into the internal memory of the active channel.

When a block transfer has come to its end (BTCNT is zero), the Valid bit in the Block Transfer Control register will be cleared (BTCTRL.VALID=0) before the entire transfer descriptor is written to the write-back memory. The optional interrupts, Channel Transfer Complete and Channel Suspend, and the optional output event Block, will be generated if configured and enabled. After the last block transfer in a transaction, the Next Descriptor Address register (DESCADDR) will hold the value 0x00000000, and the DMA channel will either be suspended or disabled, depending on the configuration in the Block Action bit group in the Block Transfer Control register (BTCTRL.BLOCKACT). If the transaction has further block transfers pending, DESCADDR will hold the SRAM address to the next transfer descriptor to be fetched. The DMAC will fetch the next descriptor into the internal memory of the active channel and write its content to the write-back section for the channel, before the arbiter gets to choose the next active channel.

26.6.2.6. Transfer Triggers and Actions

A DMA transfer through a DMA channel can be started only when a DMA transfer request is detected, and the DMA channel has been granted access to the DMA. A transfer request can be triggered from software, from a peripheral, or from an event. There are dedicated Trigger Source selections for each DMA Channel Control B (CHCTRLB.TRIGSRC).

The trigger actions are available in the Trigger Action bit group in the Channel Control B register (CHCTRLB.TRIGACT). By default, a trigger generates a request for a block transfer operation. If a single descriptor is defined for a channel, the channel is automatically disabled when a block transfer has been completed. If a list of linked descriptors is defined for a channel, the channel is automatically disabled when the last descriptor in the list is executed. If the list still has descriptors to execute, the channel will be waiting for the next block transfer trigger. When enabled again, the channel will wait for the next block transfer trigger. The trigger actions can also be configured to generate a request for a beat transfer (CHCTRLB.TRIGACT=0x2) or transaction transfer (CHCTRLB.TRIGACT=0x3) instead of a block transfer (CHCTRLB.TRIGACT=0x0).

Figure 26-7 shows an example where triggers are used with two linked block descriptors.

AMODE[1:0]	Name	Description
0x0	MASK	ADDRMASK is used as a mask to the ADDR register
0x1	2_ADDRS	The slave responds to the two unique addresses in ADDR and ADDRMASK
0x2	RANGE	The slave responds to the range of addresses between and including ADDR and ADDRMASK. ADDR is the upper limit
0x3	-	Reserved

Bit 13 – MSSEN: Master Slave Select Enable
This bit enables hardware slave select ($\overline{SS}$) control.

Value	Description
0	Hardware $\overline{SS}$ control is disabled.
1	Hardware $\overline{SS}$ control is enabled.

Bit 9 – SSDE: Slave Select Low Detect Enable
This bit enables wake up when the slave select ($\overline{SS}$) pin transitions from high to low.

Value	Description
0	$\overline{SS}$ low detector is disabled.
1	$\overline{SS}$ low detector is enabled.

Bit 6 – PLOADEN: Slave Data Preload Enable
Setting this bit will enable preloading of the slave shift register when there is no transfer in progress. If the $\overline{SS}$ line is high when DATA is written, it will be transferred immediately to the shift register.

Bits 2:0 – CHSIZE[2:0]: Character Size

CHSIZE[2:0]	Name	Description
0x0	8BIT	8 bits
0x1	9BIT	9 bits
0x2-0x7	-	Reserved

Value	Description
0	Automatic transfer length disabled.
1	Automatic transfer length enabled.

Bits 10:8 – ADDR[2:0]: Address
When ADDR is written, the consecutive operation will depend on the bus state:

UNKNOWN: INTFLAG.MB and STATUS.BUSERR are set, and the operation is terminated.

BUSY: The I^2C master will await further operation until the bus becomes IDLE.

IDLE: The I^2C master will issue a start condition followed by the address written in ADDR. If the address is acknowledged, SCL is forced and held low, and STATUS.CLKHOLD and INTFLAG.MB are set.

OWNER: A repeated start sequence will be performed. If the previous transaction was a read, the acknowledge action is sent before the repeated start bus condition is issued on the bus. Writing ADDR to issue a repeated start is performed while INTFLAG.MB or INTFLAG.SB is set.

STATUS.BUSERR, STATUS.ARBLOST, INTFLAG.MB and INTFLAG.SB will be cleared when ADDR is written.

The ADDR register can be read at any time without interfering with ongoing bus activity, as a read access does not trigger the master logic to perform any bus protocol related operations.

The I^2C master control logic uses bit 0 of ADDR as the bus protocol's read/write flag (R/W); 0 for write and 1 for read.

Value	Name	Description
0x2	COUNT32	Counter in 32-bit mode
0x3	-	Reserved

Bit 1 – ENABLE: Enable
Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately, and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST: Software Reset
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

Bits 20, 21 – COPEN0, COPEN1: Capture On Pin x Enable [x = 1..0]
This bit selects the trigger source for capture operation, either events or I/O pin input.

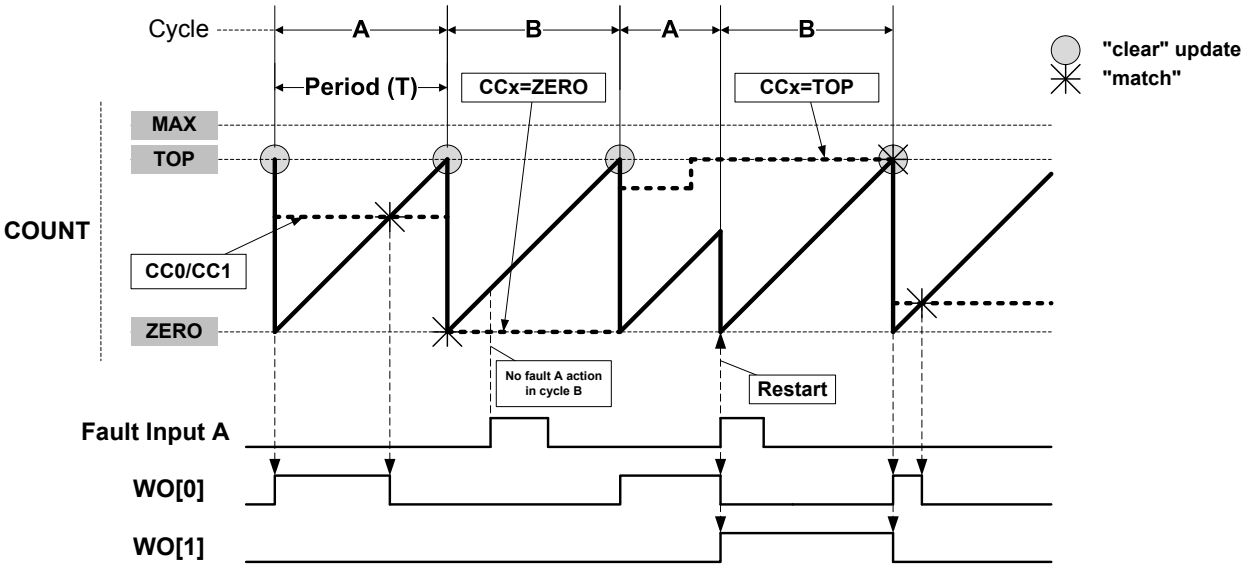
Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTEN0, CAPTEN1: Capture Channel x Enable [x = 1..0]
These bits are used to select whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTENx disables capture on channel x.
1	CAPTENx enables capture on channel x.

Figure 36-27. Waveform Generation in RAMP2 mode with Restart Action



Capture Action

Several capture actions can be selected by writing the Fault n Capture Action bits in the Fault n Control register (FCTRLn.CAPTURE). When one of the capture operations is selected, the counter value is captured when the fault occurs. These capture operations are available:

- CAPT - the equivalent to a standard capture operation, for further details refer to Capture Operations
- CAPTMIN - gets the minimum time stamped value: on each new local minimum captured value, an event or interrupt is issued.
- CAPTMAX - gets the maximum time stamped value: on each new local maximum captured value, an event or interrupt (IT) is issued, see Figure 36-28.
- LOCMIN - notifies by event or interrupt when a local minimum captured value is detected.
- LOCMAX - notifies by event or interrupt when a local maximum captured value is detected.
- DERIV0 - notifies by event or interrupt when a local extreme captured value is detected, see Figure 36-29.

CCx Content:

In CAPTMIN and CAPTMAX operations, CCx keeps the respective extremum captured values, see Figure 36-28. In LOCMIN, LOCMAX or DERIV0 operation, CCx follows the counter value at fault time, see Figure 36-29.

Before enabling CAPTMIN or CAPTMAX mode of capture, the user must initialize the corresponding CCx register value to a value different from zero (for CAPTMIN) top (for CAPTMAX). If the CCx register initial value is zero (for CAPTMIN) top (for CAPTMAX), no captures will be performed using the corresponding channel.

MCx Behaviour:

In LOCMIN and LOCMAX operation, capture is performed on each capture event. The MCx interrupt flag is set only when the captured value is upper or equal (for LOCMIN) or lower or equal (for LOCMAX) to the previous captured value. So interrupt flag is set when a new

39.8.2.5. Device Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Name: INTENCLR
Offset: 0x14
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
							LPMSUSP	LPMNYET
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RAMACER	UPRSM	EORSM	WAKEUP	EORST	SOF		SUSPEND
Access	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0		0

Bit 9 – LPMSUSP: Link Power Management Suspend Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Link Power Management Suspend Interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Link Power Management Suspend interrupt is disabled.
1	The Link Power Management Suspend interrupt is enabled and an interrupt request will be generated when the Link Power Management Suspend interrupt Flag is set.

Bit 8 – LPMNYET: Link Power Management Not Yet Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Link Power Management Not Yet interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Link Power Management Not Yet interrupt is disabled.
1	The Link Power Management Not Yet interrupt is enabled and an interrupt request will be generated when the Link Power Management Not Yet interrupt Flag is set.

Bit 7 – RAMACER: RAM Access Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the RAM Access interrupt Enable bit and disable the corresponding interrupt request.

39.8.5.9. Pipe Interrupt Summary

Name: PINTSMRY
Offset: 0x20
Reset: 0x00000000
Property: Read-only

Bit	15	14	13	12	11	10	9	8
	PINT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PINT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PINT[15:0]
The flag PINT[n] is set when an interrupt is triggered by the pipe n. See PINTFLAG register in the Host Pipe Register section.

This bit will be cleared when there are no interrupts pending for Pipe n.

Writing to this bit has no effect.

39.8.6. Host Registers - Pipe

39.8.7.4. Extended Register

Name: EXTREG
Offset: 0x08
Reset: 0xxxxxxxx
Property: NA

Bit	15	14	13	12	11	10	9	8
		VARIABLE[10:4]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VARIABLE[3:0]				SUBPID[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	x	0	0	0	x

Bits 14:4 – VARIABLE[10:0]: Extended variable
These bits define the VARIABLE field sent with extended token. See “Section 2.1.1 Protocol Extension Token in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum.”

To support the USB2.0 Link Power Management addition the VARIABLE field should be set as described below.

VARIABLE	Description
VARIABLE[3:0]	bLinkState(1)
VARIABLE[7:4]	BESL (See LPM ECN)(2)
VARIABLE[8]	bRemoteWake(1)
VARIABLE[10:9]	Reserved

(1) for a definition of LPM Token bRemoteWake and bLinkState fields, refer to "Table 2-3 in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum"
(2) for a definition of LPM Token BESL field, refer to "Table 2-3 in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum" and "Table X-X1 in Errata for ECN USB 2.0 Link Power Management.

Bits 3:0 – SUBPID[3:0]: SUBPID
These bits define the SUBPID field sent with extended token. See “Section 2.1.1 Protocol Extension Token in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum”.

To support the USB2.0 Link Power Management addition the SUBPID field should be set as described in “Table 2.2 SubPID Types in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum”.

Value	Name	Description
0x0	Mode 0	Minimum current consumption, but the slowest mode
0x1	Mode 1	Low current consumption, slow speed
0x2	Mode 2	High current consumption, fast speed
0x3	Mode 3	Maximum current consumption but the fastest mode

Bit 2 – ANAOUT: Analog Output
This bit controls a switch connected to the OPAMP output.

Value	Description
0	Swith open. No ADC or AC connection.
1	Switch closed. OPAMP output is connected to the ADC or AC input.

Bit 1 – ENABLE: Operational Amplifier Enable

Value	Description
0	The OPAMPx is disabled
1	The OPAMPx is enabled

Note: To perform the accumulation of two or more samples, the Conversion Result Resolution field in the Control C register (CTRLC.RESSEL) must be set.

Table 42-1. Accumulation

Number of Accumulated Samples	AVGCTRL. SAMPLENUM	Number of Automatic Right Shifts	Final Result Precision	Automatic Division Factor
1	0x0	0	12 bits	0
2	0x1	0	13 bits	0
4	0x2	0	14 bits	0
8	0x3	0	15 bits	0
16	0x4	0	16 bits	0
32	0x5	1	16 bits	2
64	0x6	2	16 bits	4
128	0x7	3	16 bits	8
256	0x8	4	16 bits	16
512	0x9	5	16 bits	32
1024	0xA	6	16 bits	64
Reserved	0xB –0xF		12 bits	0

42.6.2.10. Averaging

Averaging is a feature that increases the sample accuracy, at the cost of a reduced sampling rate. This feature is suitable when operating in noisy conditions.

Averaging is done by accumulating m samples, as described in Accumulation, and dividing the result by m. The averaged result is available in the RESULT register. The number of samples to be accumulated is specified by writing to AVGCTRL.SAMPLENUM as shown in Table 42-2.

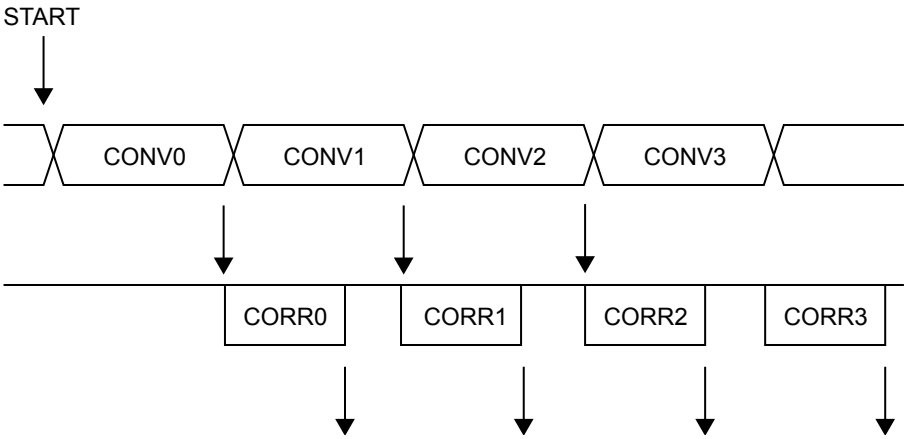
The division is obtained by a combination of the automatic right shift described above, and an additional right shift that must be specified by writing to the Adjusting Result/Division Coefficient field in AVGCTRL (AVGCTRL.ADJRES), as described in Table 42-2.

Note: To perform the averaging of two or more samples, the Conversion Result Resolution field in the Control C register (CTRLC.RESSEL) must be set.

Averaging AVGCTRL.SAMPLENUM samples will reduce the un-averaged sampling rate by a factor $\frac{1}{\text{AVGCTRL.SAMPLENUM}}$.

When the averaged result is available, the INTFLAG.RESRDY bit will be set.

Figure 42-8. ADC Timing Correction Enabled



42.6.3. Additional Features

42.6.3.1. Device Temperature Measurement

Principle

The device has an integrated temperature sensor which is part of the Supply Controller (SUPC). The analog signal of that sensor can be converted into a digital value by the ADC. The digital value can be converted into a temperature in °C by following the steps in this section.

Configuration and Conditions

In order to conduct temperature measurements, configure the device according to these steps.

1. Configure the clocks and device frequencies according to the Electrical Characteristics.
2. Configure the Voltage References System of the Supply Controller (SUPC):
   - 2.1. Enable the temperature sensor by writing a '1' to the Temperature Sensor Enable bit in the VREF Control register (SUPC.VREF.TSEN).
   - 2.2. Select the required voltage for the internal voltage reference INTREF by writing to the Voltage Reference Selection bits (SUPC.VREF.SEL). The required value can be found in the Electrical Characteristics.
   - 2.3. Enable routing INTREF to the ADC by writing a '1' to the Voltage Reference Output Enable bit (SUPC.VREF.VREFOE).
3. Configure the ADC:
   - 3.1. Select the internal voltage reference INTREF as ADC reference voltage by writing to the Reference Control register (ADC.REFCTRL.REFSEL).
   - 3.2. Select the temperature sensor vs. internal GND as input by writing TEMP and GND to the positive and negative MUX Input Selection bit fields (ADC.INPUTCTRL.MUXNEG and .MUXPOS, respectively).
   - 3.3. Configure the remaining ADC parameters according to the Electrical Characteristics.
   - 3.4. Enable the ADC and acquire a value, ADC_m.

Calculation Parameter Values

The temperature sensor behavior is linear, but it is sensitive to several parameters such as the internal voltage reference - which itself depends on the temperature. To take this into account, each device contains a Temperature Log row with individual calibration data measured and written during the

Table 42-4. ADC Sleep Behavior

CTRLA.RUNSTDBY	CTRLA.ONDEMAND	CTRLA.ENABLE	Description
x	x	0	Disabled
0	0	1	Run in all sleep modes except STANDBY.
0	1	1	Run in all sleep modes on request, except STANDBY.
1	0	1	Run in all sleep modes.
1	1	1	Run in all sleep modes on request.

42.6.8. Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in Control A register (CTRLA.SWRST)
- Enable bit in Control A register (CTRLA.ENABLE)

The following registers are synchronized when written:

- Input Control register (INPUTCTRL)
- Control C register (CTRLC)
- Average control register (AVGCTRL)
- Sampling time control register (SAMPCTRL)
- Window Monitor Lower Threshold register (WINLT)
- Window Monitor Upper Threshold register (WINUT)
- Gain correction register (GAINCORR)
- Offset Correction register (OFFSETCORR)
- Software Trigger register (SWTRIG)

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

Related Links

Register Synchronization on page 129

Value	Name	Description
0x2	CC12M	6MHz < GCLK_DAC ≤ 12MHz (1MSPS)
0x3	Reserved	

Bit 1 – ENABLE: Enable DAC0
This bit enables DAC0 when DAC Controller is enabled (CTRLA.ENABLE).

Value	Description
0	DAC0 is disabled.
1	DAC0 is enabled.

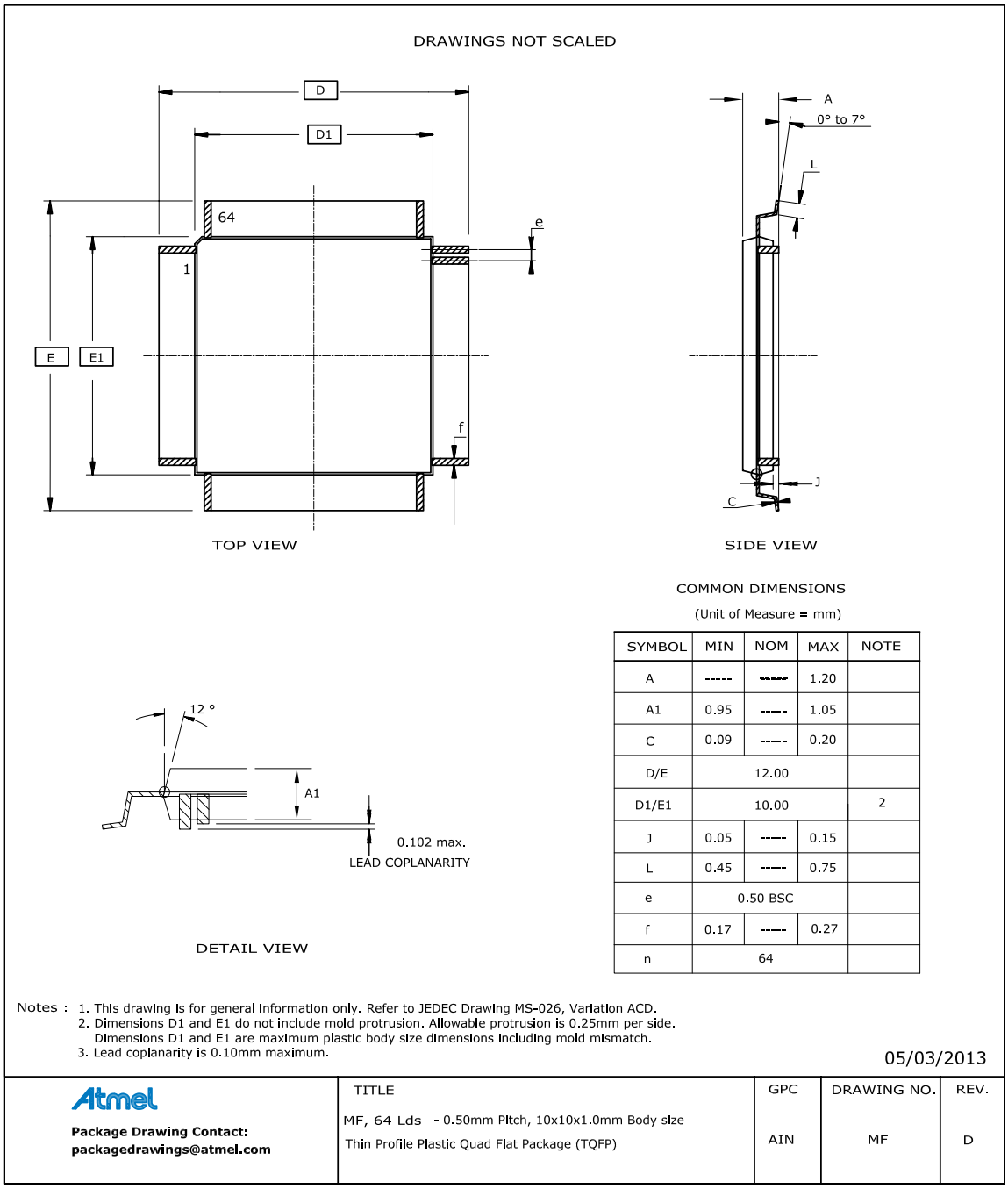
Bit 0 – LEFTADJ: Left Adjusted Data
This bit controls how the 12-bit conversion data is adjusted in the Data and Data Buffer registers.

Value	Description
0	DATA0 and DATABUF0 registers are right-adjusted.
1	DATA0 and DATABUF0 registers are left-adjusted.

Table 48-4. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

48.2.2. 64 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

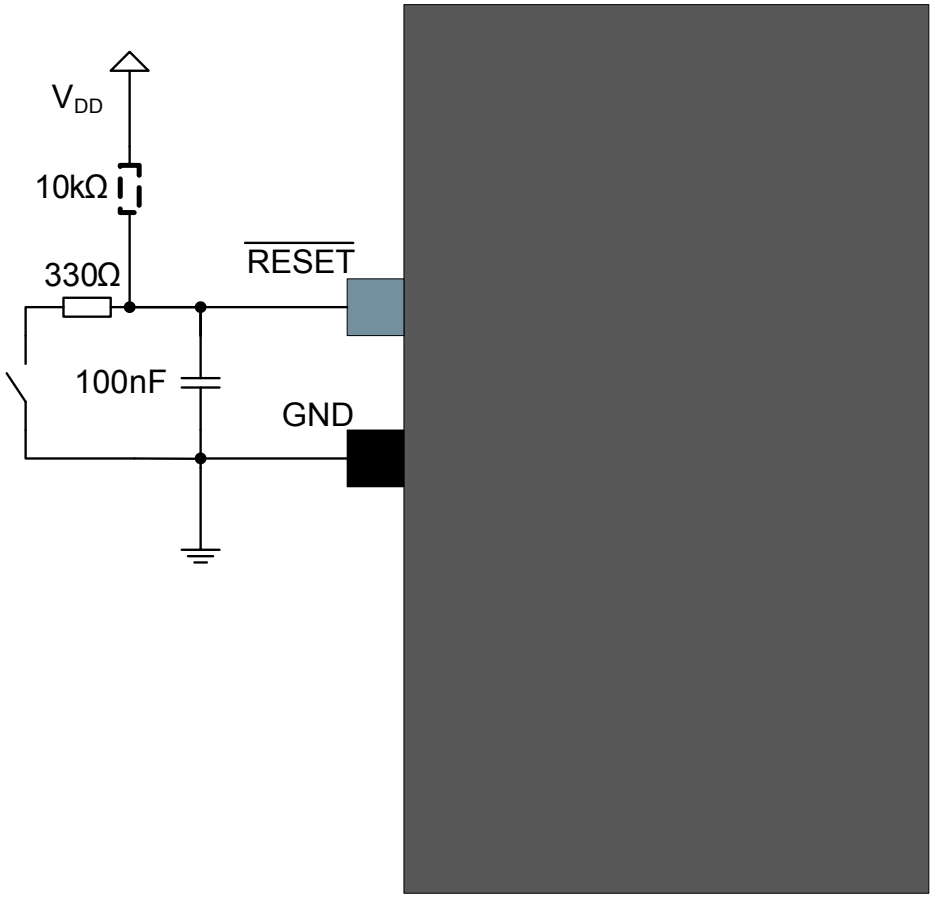
05/03/2013

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AIN	MF	D

Table 48-5. Device and Package Maximum Weight

300	mg

Figure 49-6. External Reset Circuit Schematic



A pull-up resistor makes sure that the reset does not go low and unintentionally causing a device reset. An additional resistor has been added in series with the switch to safely discharge the filtering capacitor, i.e. preventing a current surge when shorting the filtering capacitor which again can cause a noise spike that can have a negative effect on the system.

Table 49-3. Reset Circuit Connections

Signal Name	Recommended Pin Connection	Description
$\overline{\text{RESET}}$	Reset low level threshold voltage V_{DDIO} = 1.6V - 2.0V: Below 0.33 * V_{DDIO} V_{DDIO} = 2.7V - 3.6V: Below 0.36 * V_{DDIO} Decoupling/filter capacitor 100nF(1) Pull-up resistor 10kΩ(1)(2) Resistor in series with the switch 330Ω(1)	Reset pin

1. These values are only given as a typical example.

2. The SAM L21 features an internal pull-up resistor on the $\overline{\text{RESET}}$ pin, hence an external pull-up is optional.

Electrical Characteristics	• GPIO Cluster information moved to I/O Multiplexing and Considerations section. • Section IO Pin Characteristics consolidated.