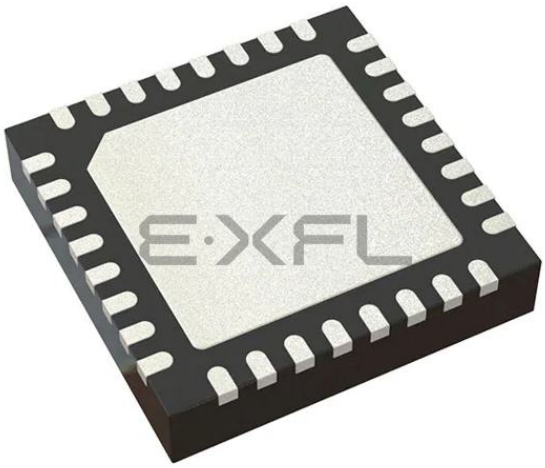


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml21e16b-mnt

Bit 3 – OSCCTRL: Peripheral OSCCTRL Write Protection Status

Bit 2 – RSTC: Peripheral RSTC Write Protection Status

Bit 1 – MCLK: Peripheral MCLK Write Protection Status

Bit 0 – PM: Peripheral ATW Write Protection Status

17.5.2. Power Management

The GCLK can operate in all sleep modes, if required.

Related Links

PM – Power Manager on page 192

17.5.3. Clocks

The GCLK bus clock (CLK_GCLK_APB) can be enabled and disabled in the Main Clock Controller.

Related Links

Peripheral Clock Masking on page 157

OSC32KCTRL – 32KHz Oscillators Controller on page 273

17.5.4. DMA

Not applicable.

17.5.5. Interrupts

Not applicable.

17.5.6. Events

Not applicable.

17.5.7. Debug Operation

When the CPU is halted in debug mode the GCLK continues normal operation. If the GCLK is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

17.5.8. Register Access Protection

All registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC).

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

When the CPU is halted in debug mode, all write-protection is automatically disabled. Write-protection does not apply for accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller on page 59

17.5.9. Analog Connections

Not applicable.

17.6. Functional Description

17.6.1. Principle of Operation

The GCLK module is comprised of nine Generic Clock Generators (Generators) sourcing up to 64 Peripheral Channels and the Main Clock signal GCLK_MAIN.

A clock source selected as input to a Generator can either be used directly, or it can be prescaled in the Generator. A generator output is used by one or more Peripheral Channels to provide a peripheral generic clock signal (GCLK_PERIPH) to the peripherals.

Value	Description
0	The APBC clock for the TC3 is stopped.
1	The APBC clock for the TC3 is enabled.

Bit 10 – TC2: TC2 APBC Mask Clock Enable

Value	Description
0	The APBC clock for the TC2 is stopped.
1	The APBC clock for the TC2 is enabled.

Bit 9 – TC1: TC1 APBC Mask Clock Enable

Value	Description
0	The APBC clock for the TC1 is stopped.
1	The APBC clock for the TC1 is enabled.

Bit 8 – TC0: TC0 APBC Mask Clock Enable

Value	Description
0	The APBC clock for the TC0 is stopped.
1	The APBC clock for the TC0 is enabled.

Bit 7 – TCC2: TCC2 APBC Mask Clock Enable

Value	Description
0	The APBC clock for the TCC2 is stopped.
1	The APBC clock for the TCC2 is enabled.

Bit 6 – TCC1: TCC1 APBC Mask Clock Enable

Value	Description
0	The APBC clock for the TCC1 is stopped.
1	The APBC clock for the TCC1 is enabled.

Bit 5 – TCC0: TCC0 APBC Mask Clock Enable

Value	Description
0	The APBC clock for the TCC0 is stopped.
1	The APBC clock for the TCC0 is enabled.

Bit 4 – SERCOM4: SERCOM4 APBC Mask Clock Enable

Value	Description
0	The APBC clock for the SERCOM4 is stopped.
1	The APBC clock for the SERCOM4 is enabled.

When entering standby mode, the power domains PD0, PD1, and PD2 are set in retention state. This allows for very low power consumption while retaining all the logic content of these power domains. When exiting standby mode, all power domains are set back to active state.

- Default operation - SleepWalking with static power gating (static SleepWalking)
  When a peripheral needs to remain running while the device is entering standby mode (e.g. to perform a sleepwalking task, or because of its RUNSTDBY bit written to '1') the power domain of the peripheral (PDn) remains in active state as well as the inferior power domains (PDm with m<n). This is an extension of the SleepWalking applied to the power domain. At the end of the sleepwalking task, the device can either be woken up or remain in standby mode.
- SleepWalking with dynamic power gating (dynamic SleepWalking)
  A power domain PDn that is in active state due to static SleepWalking can wake up a superior power domain (PDm, with m<n) in order to perform a sleepwalking task. PDm is then automatically set to active state. At the end of the sleepwalking task, either the device can be woken up, or PDm can be set again to retention state.

The static and dynamic power gated SleepWalking features are fully transparent for the user. Which power domains are powered or not can also be configured manually, refer to Linked Power Domains for details.

The table below illustrates these four cases to consider in standby mode:

1. SleepWalking is invoked on PD0,PD1, and PD2
2. SleepWalking is invoked on PD0 and PD1, while PD2 is in retention state
3. SleepWalking is invoked on PD0, while PD1 and PD2 are in retention state
4. This is the default mode where all PDs are in retention state

Table 20-3. Sleep Mode versus Power Domain State Overview

	Power Domain State				
Sleep Mode	**PD0**	**PD1**	**PD2**	**PDTOP**	**PDBACKUP**
Active	active	active	active	active	active
Idle	active	active	active	active	active
Standby - case 1	active	active	active	active	active
Standby - case 2	active	active	retention	active	active
Standby - case 3	active	retention	retention	active	active
Standby - case 4	retention	retention	retention	active	active
Backup	off	off	off	off	active
Off	off	off	off	off	off

20.6.3.7. Regulators, RAMs, and NVM State in Sleep Mode

By default, in standby sleep mode and backup sleep mode, the RAMs, NVM, and regulators are automatically set in low-power mode in order to reduce power consumption:

- The RAM is in low-power mode if its power domain is in retention or off state. Refer to *RAM Automatic Low Power Mode* for details.
- Non-Volatile Memory - the NVM is located in the power domain PD2 . By default, the NVM is automatically set in low power mode in these conditions:

  - When the power domain PD2 is in retention or off state.
  - When the device is in standby sleep mode and the NVM is not accessed. This behavior can be changed by software by configuring the SLEEPPRM bit group of the CTRLB register in the NVMCTRL peripheral.
  - When the device is in idle sleep mode and the NVM is not accessed. This behavior can be changed by software by configuring the SLEEPPRM bit group of the CTRLB register in the NVMCTRL peripheral.
- Regulators: by default, in standby sleep mode, the PM analyzes the device activity to use either the main or the low-power voltage regulator to supply the VDDCORE. Refer to the *Regulator Automatic Low Power Mode* section for details.

GCLK clocks, regulators and RAM are not affected in idle sleep mode and operate in normal mode.

Table 20-4. Regulators, RAMs, and NVM state in Sleep Mode

Sleep Mode	Switchable Power Domains			RAMs mode(1)		NVM	Regulators		
	PD0	PD1	PD2	LP SRAM	SRAM		VDDCORE		VDDBU
							main	ulp	
Active	active	active	active	normal	normal	normal	on	on	on
Idle	active	active	active	normal	auto(2)	on	on	on	on
Standby - case 1	active	active	active	normal	normal	auto(2)	auto(3)	on	on
Standby - case 2	active	active	retention	normal	low power	low power	auto(3)	on	on
Standby - case 3	active	retention	retention	low power	low power	low power	auto(3)	on	on
Standby - case 4	retention	retention	retention	low power	low power	low power	off	on	on
Backup	off	off	off	off	off	off	off	off	on
OFF	off	off	off	off	off	off	off	off	off

Note:

1. RAMs mode by default: STDBYCFG.BBIAS bits are set to their default value.
2. auto: by default, NVM is in low-power mode if not accessed.
3. auto: by default, the main voltage regulator is on if GCLK, APBx, or AHBx clock is running during SleepWalking.
4. For a description of the cases, see Power Domain Controller.

Related Links

RAM Automatic Low Power Mode on page 204

Regulator Automatic Low Power Mode on page 204

20.6.4. Advanced Features

20.6.4.1. Power Domain Configuration

When entering standby sleep mode, a power domain is set automatically to retention state if no activity is required in it, refer to Power Domain Controller for details. This behavior can be changed by writing the

20.8.4. Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Name: INTENCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								PLRDY
Access								R/W
Reset								0

Bit 0 – PLRDY: Performance Level Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Performance Ready Interrupt Enable bit and the corresponding interrupt request.

Value	Description
0	The Performance Ready interrupt is disabled.
1	The Performance Ready interrupt is enabled and will generate an interrupt request when the Performance Ready Interrupt Flag is set.

CPU Mode	XOSC32KCTRL.RUNSTDBY	XOSC32KCTRL.ONDEMAND	Sleep Behavior
Standby	1	1	Run if requested by peripheral
Standby	0	-	Run if requested by peripheral

As a crystal oscillator usually requires a very long start-up time, the 32KHz External Crystal Oscillator will keep running across resets when XOSC32K.ONDEMAND=0, except for power-on reset (POR). After a reset or when waking up from a sleep mode where the XOSC32K was disabled, the XOSC32K will need a certain amount of time to stabilize on the correct frequency. This start-up time can be configured by changing the Oscillator Start-Up Time bit group (XOSC32K.STARTUP) in the 32KHz External Crystal Oscillator Control register. During the start-up time, the oscillator output is masked to ensure that no unstable clock propagates to the digital logic.

Once the external clock or crystal oscillator is stable and ready to be used as a clock source, the XOSC32K Ready bit in the Status register is set (STATUS.XOSC32KRDY=1). The transition of STATUS.XOSC32KRDY from '0' to '1' generates an interrupt if the XOSC32K Ready bit in the Interrupt Enable Set register is set (INTENSET.XOSC32KRDY=1).

The XOSC32K can be used as a source for Generic Clock Generators (GCLK) or for the Real-Time Counter (RTC). Before enabling the GCLK or the RTC module, the corresponding oscillator output must be enabled (XOSC32K.EN32K or XOSC32K.EN1K) in order to ensure proper operation. In the same way, the GCLK or RTC modules must be disabled before the clock selection is changed. For details on RTC clock configuration, refer also to Real-Time Counter Clock Selection.

Related Links

GCLK - Generic Clock Controller on page 133
RTC – Real-Time Counter on page 347

22.6.3. 32KHz Internal Oscillator (OSC32K) Operation

The OSC32K provides a tunable, low-speed, and low-power clock source.

At reset, the OSC32K is disabled. It can be enabled by setting the Enable bit in the 32KHz Internal Oscillator Control register (OSC32K.ENABLE=1). The OSC32K is disabled by clearing the Enable bit in the 32KHz Internal Oscillator Control register (OSC32K.ENABLE=0).

The frequency of the OSC32K oscillator is controlled by OSC32K.CALIB, which is a calibration value in the 32KHz Internal Oscillator Calibration bits in the 32KHz Internal Oscillator Control register. The CALIB value must be must be loaded with production calibration values from the NVM Software Calibration Area. When writing the Calibration bits, the user must wait for the STATUS.OSC32KRDY bit to go high before the new value is committed to the oscillator.

The OSC32K has a 32.768kHz output which is enabled by setting the 32KHz Output Enable bit in the 32KHz Internal Oscillator Control register (OSC32K.EN32K=1). The OSC32K also has a 1.024kHz clock output. This is enabled by setting the 1KHz Output Enable bit in the 32KHz Internal Oscillator Control register (OSC32K.EN1K).

The OSC32K will behave differently in different sleep modes based on the settings of OSC32K.RUNSTDBY, OSC32K.ONDEMAND, and OSC32K.ENABLE. If OSC32KCTRL.ENABLE=0, the OSC32K will be always stopped. For OS32KCTRL.ENABLE=1, this table is valid:

22.8.3. Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x08
Reset: 0x00000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							OSC32KRDY	XOSC32KRDY
Access							R/W	R/W
Reset							0	0

Bit 1 – OSC32KRDY: OSC32K Ready
This flag is cleared by writing a '1' to it.

This flag is set by a zero-to-one transition of the OSC32K Ready bit in the Status register (STATUS.OSC32KRDY), and will generate an interrupt request if INTENSET.OSC32KRDY=1.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the OSC32K Ready interrupt flag.

Bit 0 – XOSC32KRDY: XOSC32K Ready
This flag is cleared by writing a '1' to it.

This flag is set by a zero-to-one transition of the XOSC32K Ready bit in the Status register (STATUS.XOSC32KRDY), and will generate an interrupt request if INTENSET.XOSC32KRDY=1.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the XOSC32K Ready interrupt flag.

23.8.2. Interrupt Enable Set

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Name: INTENSET
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						VCORERDY	APWSRDY	VREGRDY
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
						B33SRDY	BOD33DET	BOD33RDY
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 10 – VCORERDY: VDDCORE Voltage Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the VDDCORE Ready Interrupt Enable bit, which enables the VDDCORE Ready interrupt.

Value	Description
0	The VDDCORE Ready interrupt is disabled.
1	The VDDCORE Ready interrupt is enabled and an interrupt request will be generated when the VCORERDY Interrupt Flag is set.

Bit 9 – APWSRDY: Automatic Power Switch Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Automatic Power Switch Ready Interrupt Enable bit, which enables the Automatic Power Switch Ready interrupt.

25.8.2. Event Control in COUNT32 mode (CTRLA.MODE=0)

Name: EVCTRL
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	OVFEO							CMPEO0
Access	R/W							R/W
Reset	0							0

Bit	7	6	5	4	3	2	1	0
	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVFEO: Overflow Event Output Enable

Value	Description
0	Overflow event is disabled and will not be generated.
1	Overflow event is enabled and will be generated for every overflow.

Bit 8 – CMPEO0: Compare 0 Event Output Enable

Value	Description
0	Compare 0 event is disabled and will not be generated.
1	Compare 0 event is enabled and will be generated for every compare match.

Bits 7:0 – PEREOn: Periodic Interval n Event Output Enable [n = 7..0]

Value	Description
0	Periodic Interval n event is disabled and will not be generated.
1	Periodic Interval n event is enabled and will be generated.

25.12.12. General Purpose n

Name: GPn
Offset: 0x40 + n*0x04 [n=0..1]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	GP[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GP[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – GP[31:0]: General Purpose
These bits are for user-defined general purpose use.

27. EIC – External Interrupt Controller

27.1. Overview

The External Interrupt Controller (EIC) allows external pins to be configured as interrupt lines. Each interrupt line can be individually masked and can generate an interrupt on rising, falling, or both edges, or on high or low levels. Each external pin has a configurable filter to remove spikes. Each external pin can also be configured to be asynchronous in order to wake up the device from sleep modes where all clocks have been disabled. External pins can also generate an event.

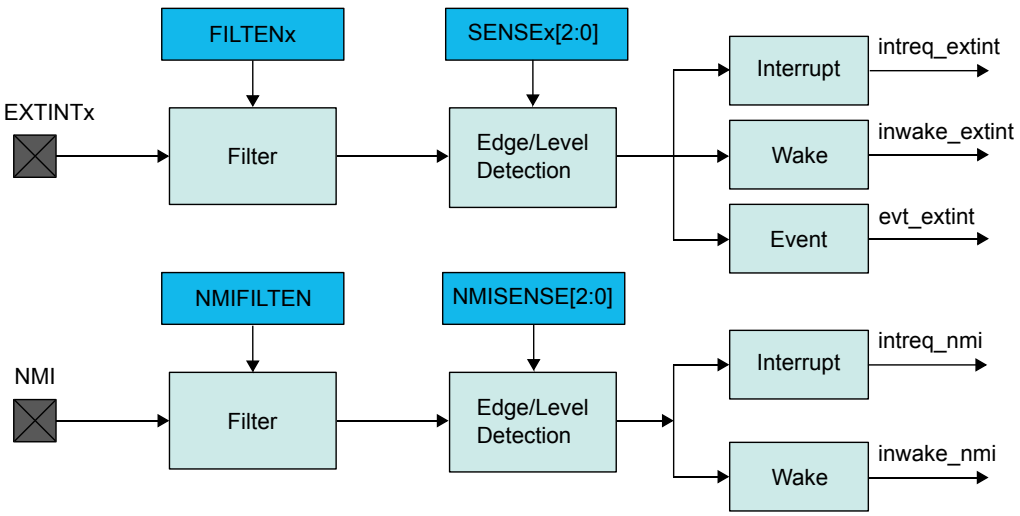
A separate non-maskable interrupt (NMI) is also supported. It has properties similar to the other external interrupts, but is connected to the NMI request of the CPU, enabling it to interrupt any other interrupt mode.

27.2. Features

- Up to 16 external pins, plus one non-maskable pin
- Dedicated, individually maskable interrupt for each pin
- Interrupt on rising, falling, or both edges
- synchronous or asynchronous edge detection mode
- Interrupt on high or low levels
- Asynchronous interrupts for sleep modes without clock
- Filtering of external pins
- Event generation

27.3. Block Diagram

Figure 27-1. EIC Block Diagram



If *even parity* is selected (CTRLB.PMODE=0), the parity bit of an outgoing frame is '1' if the data contains an odd number of bits that are '1', making the total number of '1' even.

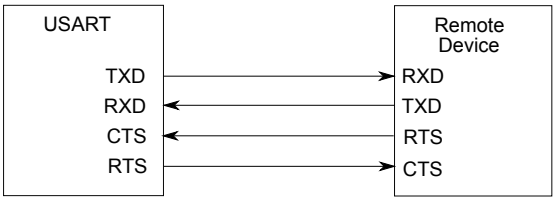
If *odd parity* is selected (CTRLB.PMODE=1), the parity bit of an outgoing frame is '1' if the data contains an even number of bits that are '0', making the total number of '1' odd.

When parity checking is enabled, the parity checker calculates the parity of the data bits in incoming frames and compares the result with the parity bit of the corresponding frame. If a parity error is detected, the Parity Error bit in the Status register (STATUS.PERR) is set.

32.6.3.2. Hardware Handshaking

The USART features an out-of-band hardware handshaking flow control mechanism, implemented by connecting the RTS and CTS pins with the remote device, as shown in the figure below.

Figure 32-7. Connection with a Remote Device for Hardware Handshaking

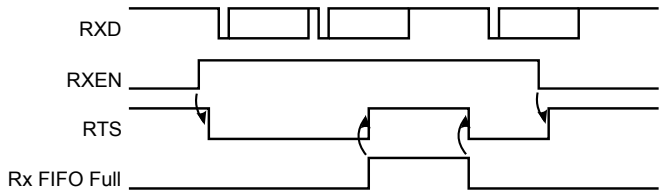


Hardware handshaking is only available in the following configuration:

- USART with internal clock (CTRLA.MODE=1),
- Asynchronous mode (CTRLA.CMODE=0),
- and Flow control pinout (CTRLA.TXPO=2).

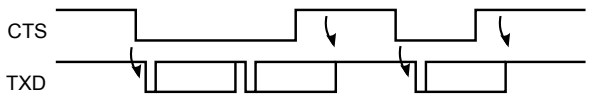
When the receiver is disabled or the receive FIFO is full, the receiver will drive the RTS pin high. This notifies the remote device to stop transfer after the ongoing transmission. Enabling and disabling the receiver by writing to CTRLB.RXEN will set/clear the RTS pin after a synchronization delay. When the receive FIFO goes full, RTS will be set immediately and the frame being received will be stored in the shift register until the receive FIFO is no longer full.

Figure 32-8. Receiver Behavior when Operating with Hardware Handshaking



The current CTS Status is in the STATUS register (STATUS.CTS). Character transmission will start only if STATUS.CTS=0. When CTS is set, the transmitter will complete the ongoing transmission and stop transmitting.

Figure 32-9. Transmitter Behavior when Operating with Hardware Handshaking



32.6.3.3. IrDA Modulation and Demodulation

Transmission and reception can be encoded IrDA compliant up to 115.2 kb/s. IrDA modulation and demodulation work in the following configuration:

- IrDA encoding enabled (CTRLB.ENC=1),
- Asynchronous mode (CTRLA.CMODE=0),

- Data Ready (DATARDY): Generated when a new random number is available in the DATA register.

Writing '1' to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables the corresponding output event. Writing a '0' to this bit disables the corresponding output event. Refer to *EVSYS – Event System* for details on configuring the Event System.

Related Links

EVSYS – Event System on page 544

37.6.5. Sleep Mode Operation

The Run in Standby bit in Control A register (CTRLA.RUNSTDBY) controls the behavior of the TRNG during standby sleep mode:

When this bit is '0', the TRNG is disabled during sleep, but maintains its current configuration.

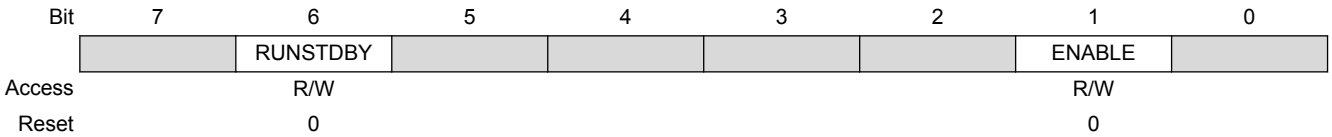
When this bit is '1', the TRNG continues to operate during sleep and any enabled TRNG interrupt source can wake up the CPU.

37.6.6. Synchronization

Not applicable.

37.8.1. Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection



Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	
Access		R/W					R/W	
Reset		0					0	

Bit 6 – RUNSTDBY: Run in Standby
This bit controls how the ADC behaves during standby sleep mode:

Value	Description
0	The TRNG is halted during standby sleep mode.
1	The TRNG is not stopped in standby sleep mode.

Bit 1 – ENABLE: Enable

Value	Description
0	The TRNG is disabled.
1	The TRNG is enabled.

Bit 6 – UPRSM: Upstream Resume Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Upstream Resume Enable bit and enable the corresponding interrupt request.

Value	Description
0	The Upstream Resume interrupt is disabled.
1	The Upstream Resume interrupt is enabled.

Bit 5 – EORSM: End Of Resume Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the End Of Resume interrupt Enable bit and enable the corresponding interrupt request.

Value	Description
0	The End Of Resume interrupt is disabled.
1	The End Of Resume interrupt is enabled.

Bit 4 – WAKEUP: Wake-Up Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Wake Up interrupt Enable bit and enable the corresponding interrupt request.

Value	Description
0	The Wake Up interrupt is disabled.
1	The Wake Up interrupt is enabled.

Bit 3 – EORST: End of Reset Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the End of Reset interrupt Enable bit and enable the corresponding interrupt request.

Value	Description
0	The End of Reset interrupt is disabled.
1	The End of Reset interrupt is enabled.

Bit 2 – SOF: Start-of-Frame Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Start-of-Frame interrupt Enable bit and enable the corresponding interrupt request.

Value	Description
0	The Start-of-Frame interrupt is disabled.
1	The Start-of-Frame interrupt is enabled.

39.8.5.1. Control B

Name: CTRLB
Offset: 0x08
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
					L1RESUME	VBUSOK	BUSRESET	SOFE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
					SPDCONF[1:0]		RESUME	
Access					R/W	R/W	R/W	
Reset					0	0	0	

Bit 11 – L1RESUME: Send USB L1 Resume
Writing 0 to this bit has no effect.
1: Generates a USB L1 Resume on the USB bus. This bit should only be set when the Start-of-Frame generation is enabled (SOFE bit set). The duration of the USB L1 Resume is defined by the EXTREG.VARIABLE[7:4] bits field also known as BESL (See LPM ECN).See also EXTREG Register.

This bit is cleared when the USB L1 Resume has been sent or when a USB reset is requested.

Bit 10 – VBUSOK: VBUS is OK
This notifies the USB HOST that USB operations can be started. When this bit is zero and even if the USB HOST is configured and enabled, HOST operation is halted. Setting this bit will allow HOST operation when the USB is configured and enabled.

Value	Description
0	The USB module is notified that the VBUS on the USB line is not powered.
1	The USB module is notified that the VBUS on the USB line is powered.

Bit 9 – BUSRESET: Send USB Reset

Value	Description
0	Reset generation is disabled. It is written to zero when the USB reset is completed or when a device disconnection is detected. Writing zero has no effect.
1	Generates a USB Reset on the USB bus.

Bit 8 – SOFE: Start-of-Frame Generation Enable

Value	Description
0	The SOF generation is disabled and the USB bus is in suspend state.
1	Generates SOF on the USB bus in full speed and keep it alive in low speed mode. This bit is automatically set at the end of a USB reset (INTFLAG.RST) or at the end of a downstream resume (INTFLAG.DNRSM) or at the end of L1 resume.

44.8.2. Control B

Name: CTRLB
Offset: 0x01
Reset: 0x02
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
						REFSEL[1:0]		DIFF
Access						R/W	R/W	R/W
Reset						0	1	0

Bits 2:1 – REFSEL[1:0]: Reference Selection
This bit field selects the Reference Voltage for both DACs.

Value	Name	Description
0x0	VREFAU	Unbuffered external voltage reference (not buffered in DAC, direct connection)
0x1	VDDANA	Voltage supply
0x2	VREFAB	Buffered external voltage reference (buffered in DAC)
0x3	INTREF	Internal bandgap reference

Bit 0 – DIFF: Differential Mode Enable
This bit defines the conversion mode for both DACs.

Value	Description
0	Single mode
1	Differential mode

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
	Integrated Noise, BW=[0.1Hz-1MHz], 16X gain - V_{OUT}=1V	Mode 3	-	262	-	µVrms
		Mode 2	-	247	-	
		Mode 1	-	235	-	
		Mode 0	-	235	-	

Note: 1.These values are based on simulation. They are not covered by production test limits or characterization.

46.11. NVM Characteristics

Table 46-39. NVM Max Speed Characteristics

	Conditions	CPU Fmax (MHz)			
		0WS	1WS	2WS	3WS
PL0 (-40/85°C)	V_{DDIN}>1.6 V	6	12	12	12
	V_{DDIN}>2.7 V	7.5	12	12	12
PL2 (-40/85°C)	V_{DDIN}>1.6 V	14	28	42	48
	V_{DDIN}>2.7 V	24	45	48	48

Table 46-40. NVM Timing Characteristics

Symbol	Timings	Max	Units
t_{FPP}	Page Write(1)	2.5	ms
t_{FRE}	Row erase(1)	6	

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.
2. For this Flash technology, a maximum number of 8 consecutive writes is allowed per row. Once this number is reached, a row erase is mandatory.

Table 46-41. NVM Reliability Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ret_{NVM25k}	Retention after up to 25k	Average ambient 55°C	10	50	-	Years
$Ret_{NVM2.5k}$	Retention after up to 2.5k	Average ambient 55°C	20	100	-	Years
Ret_{NVM100}	Retention after up to 100	Average ambient 55°C	25	>100	-	Years
Cyc_{NVM}	Cycling Endurance(1)	-40°C < Ta < 85°C	25K	100K	-	Cycles

Note: 1. An endurance cycle is a write and an erase operation.

6 – The SUPC/OUT pins toggle on the RTC Periodic Interval 0 (PER0) event only.
Errata reference: 14151
Fix/Workaround:
None

7 – In IDLE sleep mode, the APB and AHB clocks are not stopped if the DFLL is running as a GCLK clock source.
Errata reference: 13384
Fix/Workaround:
Disable the DFLL before entering IDLE sleep mode.

8 – The default TC selection as CCL input is not TC0 but TC4. Thus the TC selection is TC4/TC0/TC1/TC2 instead of TC0/TC1/TC2/TC3. And the TC alternate selection is TC0/TC1/TC2/TC3 instead of TC1/TC2/TC3/TC4.
Errata reference: 13406
Fix/Workaround:
Use the TC input mapping described above.

9 – Pulldown functionality is not available on GPIO pin PA24 and PA25
Errata reference: 13915
Fix/Workaround:
None

10 – When BOD12 is configured to run in continuous mode (BOD12.STDBYCFG=0) in standby sleep mode, and configured to run in sampling mode (BOD12.ACTCFG=1) in active mode, the BOD12 detection does not work in standby sleep mode.
Errata reference: 14150
Fix/Workaround:
Any other combination of BOD12.STDBYCFG and BOD12.ACTCFG works as expected.

11 – When internal voltage reference (SUPC.VREF.SEL) is selected as an input for the ADC and when SUPC.VREF.SEL > 0x4, then this reference is statically enabled and SUPC.VREF.ONDEMAND has no effect.
Errata reference: 14588
Fix/Workaround :
None

12 – In I2C Slave mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.
Errata reference: 13574
Fix/Workaround:
Write CTRLB.ACKACT to 0 using the following sequence:
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
// Re-enable interrupts if applicable.
Write CTRLB.ACKACT to 1 using the following sequence:
// If higher priority interrupts exist, then disable so that the