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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atsaml21e18b-mnt">https://www.e-xfl.com/product-detail/microchip-technology/atsaml21e18b-mnt</a>

**Note:** Once the DFLL48M is enabled in on-demand mode (DFLLCTRL.ONDEMAND=1), the STATUS.DFLLRDY bit will keep to '0' until the DFLL48M is requested by a peripheral.

Before writing to any of the DFLL48M control registers, the user must check that the DFLL Ready bit (STATUS.DFLLRDY) is set to '1'. When this bit is set, the DFLL48M can be configured and CLK\_DFLL48M is ready to be used. Any write to any of the DFLL48M control registers while DFLLRDY is '0' will be ignored.

In order to read from the DFLLVAL register in closed loop mode, the user must request a read synchronization by writing a '1' to the Read Request bit in the DFLL Synchronization register (DFLLSYNC.READREQ). This is required because the DFLL controller may change the content of the DFLLVAL register any time. If a read operation is issued while the DFLL controller is updating the DFLLVAL content, a zero will be returned.

**Note:** Issuing a read on any register while a write-synchronization is still on-going will return a zero.

Read-Synchronized registers using DFLLSYNC.READREQ:

- DFLL48M Value register (DFLLVAL)

Write-Synchronized registers:

- DFLL48M Control register (DFLLCTRL)
- DFLL48M Value register (DFLLVAL)
- DFLL48M Multiplier register (DFLLMUL)

## DPLL96M

Due to the multiple clock domains, some registers in the DPLL96M must be synchronized when accessed.

When executing an operation that requires synchronization, the relevant synchronization bit in the Synchronization Busy register (DPLLSYNCBUSY) will be set immediately, and cleared when synchronization is complete.

The following bits need synchronization when written:

- Enable bit in control register A (DPLLCTRLA.ENABLE)
- DPLL Ratio register (DPLLRATIO)
- DPLL Prescaler register (DPLLPRESC)

## Related Links

[Register Synchronization](#) on page 129

Value	Description
0	XOSC is not switched and provides the external clock or crystal oscillator clock.
1	XOSC is switched and provides the safe clock.

**Bit 1 – CLKFAIL: XOSC Clock Failure**

Value	Description
0	No XOSC failure detected.
1	A XOSC failure was detected.

**Bit 0 – XOSCRDY: XOSC Ready**

Value	Description
0	XOSC is not ready.
1	XOSC is stable and ready to be used as a clock source.

**Bit 1 – ENABLE: DFLL Enable**

Due to synchronization, there is delay from updating the register until the peripheral is enabled/disabled. The value written to DFLLCTRL.ENABLE will read back immediately after written.

Value	Description
0	The DFLL oscillator is disabled.
1	The DFLL oscillator is enabled.

Value	Name	Description
0x8	DIV512	Divide clock by 512
0x9	DIV1024	Divide clock by 1024
0xA	DIV2048	Divide clock by 2048
0xB	DIV4096	Divide clock by 4096
0xC	DIV8192	Divide clock by 8192
0xD	DIV16384	Divide clock by 16384
0xE	DIV32768	Divide clock by 32768
0xF	DIV65536	Divide clock by 65536

#### Bit 8 – ACTCFG: BOD12 Configuration in Active Sleep Mode

This field is not synchronized.

Value	Description
0	In active mode, the BOD12 operates in continuous mode.
1	In active mode, the BOD12 operates in sampling mode.

#### Bit 6 – RUNSTDBY: Run in Standby

This bit is not synchronized.

Value	Description
0	In standby sleep mode, the BOD12 is disabled.
1	In standby sleep mode, the BOD12 is enabled.

#### Bit 5 – STDBYCFG: BOD12 Configuration in Standby Sleep Mode

If the RUNSTDBY bit is set to 1, the STDBYCFG bit sets the BOD12 configuration in standby sleep mode.

This field is not synchronized.

Value	Description
0	In standby sleep mode, the BOD12 is enabled and configured in continuous mode.
1	In standby sleep mode, the BOD12 is enabled and configured in sampling mode.

#### Bits 4:3 – ACTION[1:0]: BOD12 Action

These bits are used to select the BOD12 action when the supply voltage crosses below the BOD12 threshold.

These bits are loaded from NVM User Row at start-up.

This field is not synchronized.

Value	Name	Description
0x0	NONE	No action.
0x1	RESET	The BOD12 generates a reset.

Writing a '1' to this bit will enable the destination address incrementation. By default, the destination address is incremented by 1. If the STEPSEL bit is cleared, flexible step-size settings are available in the STEPSIZE register.

Value	Description
0	The Destination Address Increment is disabled.
1	The Destination Address Increment is enabled.

#### Bit 10 – SRCINC: Source Address Increment Enable

Writing a '0' to this bit will disable the source address incrementation. The address will be kept fixed during the data transfer.

Writing a '1' to this bit will enable the source address incrementation. By default, the source address is incremented by 1. If the STEPSEL bit is set, flexible step-size settings are available in the STEPSIZE register.

Value	Description
0	The Source Address Increment is disabled.
1	The Source Address Increment is enabled.

#### Bits 9:8 – BEATSIZE[1:0]: Beat Size

These bits define the size of one beat. A beat is the size of one data transfer bus access, and the setting apply to both read and write accesses.

BEATSIZE[1:0]	Name	Description
0x0	BYTE	8-bit bus transfer
0x1	WORD	16-bit bus transfer
0x2	WORD	32-bit bus transfer
0x3		Reserved

#### Bits 4:3 – BLOCKACT[1:0]: Block Action

These bits define what actions the DMAC should take after a block transfer has completed.

BLOCKACT[1:0]	Name	Description
0x0	NOACT	Channel will be disabled if it is the last block transfer in the transaction
0x1	INT	Channel will be disabled if it is the last block transfer in the transaction and block interrupt
0x2	SUSPEND	Channel suspend operation is completed
0x3	BOTH	Both channel suspend operation and block interrupt

#### Bits 2:1 – EVOSEL[1:0]: Event Output Selection

These bits define the event output selection.

### 29.8.1. Data Direction

This register allows the user to configure one or more I/O pins as an input or output. This register can be manipulated without doing a read-modify-write operation by using the Data Direction Toggle (DIRTGL), Data Direction Clear (DIRCLR) and Data Direction Set (DIRSET) registers.

**Name:** DIR

**Offset:** 0x00

**Reset:** 0x00000000

**Property:** PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	DIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	DIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	DIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	DIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 – DIR[31:0]: Port Data Direction

These bits set the data direction for the individual I/O pins in the PORT group.

Value	Description
0	The corresponding I/O pin in the PORT group is configured as an input.
1	The corresponding I/O pin in the PORT group is configured as an output.

### 32.6.4. DMA, Interrupts and Events

Table 32-4. Module Request for SERCOM USART

Condition	Request		
	DMA	Interrupt	Event
Data Register Empty (DRE)	Yes (request cleared when data is written)	Yes	NA
Receive Complete (RXC)	Yes (request cleared when data is read)	Yes	
Transmit Complete (TXC)	NA	Yes	
Receive Start (RXS)	NA	Yes	
Clear to Send Input Change (CTSIC)	NA	Yes	
Receive Break (RXBRK)	NA	Yes	
Error (ERROR)	NA	Yes	

#### 32.6.4.1. DMA Operation

The USART generates the following DMA requests:

- Data received (RX): The request is set when data is available in the receive FIFO. The request is cleared when DATA is read.
- Data transmit (TX): The request is set when the transmit buffer (TX DATA) is empty. The request is cleared when DATA is written.

#### 32.6.4.2. Interrupts

The USART has the following interrupt sources. These are asynchronous interrupts, and can wake up the device from any sleep mode:

- Data Register Empty (DRE)
- Receive Complete (RXC)
- Transmit Complete (TXC)
- Receive Start (RXS)
- Clear to Send Input Change (CTSIC)
- Received Break (RXBRK)
- Error (ERROR)

Each interrupt source has its own interrupt flag. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) will be set when the interrupt condition is met. Each interrupt can be individually enabled by writing '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR).

An interrupt request is generated when the interrupt flag is set and if the corresponding interrupt is enabled. The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled, or the USART is reset. For details on clearing interrupt flags, refer to the INTFLAG register description.

The USART has one common interrupt request line for all the interrupt sources. The value of INTFLAG indicates which interrupt is executed. Note that interrupts must be globally enabled for interrupt requests. Refer to *Nested Vector Interrupt Controller* for details.



AMODE[1:0]	Name	Description
0x0	MASK	ADDRMASK is used as a mask to the ADDR register
0x1	2_ADDRS	The slave responds to the two unique addresses in ADDR and ADDRMASK
0x2	RANGE	The slave responds to the range of addresses between and including ADDR and ADDRMASK. ADDR is the upper limit
0x3	-	Reserved

#### Bit 13 – MSSEN: Master Slave Select Enable

This bit enables hardware slave select ( $\overline{SS}$ ) control.

Value	Description
0	Hardware $\overline{SS}$ control is disabled.
1	Hardware $\overline{SS}$ control is enabled.

#### Bit 9 – SSDE: Slave Select Low Detect Enable

This bit enables wake up when the slave select ( $\overline{SS}$ ) pin transitions from high to low.

Value	Description
0	$\overline{SS}$ low detector is disabled.
1	$\overline{SS}$ low detector is enabled.

#### Bit 6 – PLOADEN: Slave Data Preload Enable

Setting this bit will enable preloading of the slave shift register when there is no transfer in progress. If the  $\overline{SS}$  line is high when DATA is written, it will be transferred immediately to the shift register.

#### Bits 2:0 – CHSIZE[2:0]: Character Size

CHSIZE[2:0]	Name	Description
0x0	8BIT	8 bits
0x1	9BIT	9 bits
0x2-0x7	-	Reserved

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Value	Description
0	The Stop Received interrupt is disabled.
1	The Stop Received interrupt is enabled.

Writing '0' to this bit has no effect.

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

### 39.8.2.6. Device Interrupt Enable Set

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

**Name:** INTENSET

**Offset:** 0x18

**Reset:** 0x0000

**Property:** PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
							LPMSUSP	LPMNYET
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RAMACER	UPRSM	EORSM	WAKEUP	EORST	SOF		SUSPEND
Access	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0		0

#### Bit 9 – LPMSUSP: Link Power Management Suspend Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will set the Link Power Management Suspend Enable bit and enable the corresponding interrupt request.

Value	Description
0	The Link Power Management Suspend interrupt is disabled.
1	The Link Power Management Suspend interrupt is enabled.

#### Bit 8 – LPMNYET: Link Power Management Not Yet Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will set the Link Power Management Not Yet interrupt bit and enable the corresponding interrupt request.

Value	Description
0	The Link Power Management Not Yet interrupt is disabled.
1	The Link Power Management Not Yet interrupt is enabled.

#### Bit 7 – RAMACER: RAM Access Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will set the RAM Access Enable bit and enable the corresponding interrupt request.

Value	Description
0	The RAM Access interrupt is disabled.
1	The RAM Access interrupt is enabled.

### Bit 7 – EDGESEL: Edge Selection

Value	Description
0	Edge detector is disabled.
1	Edge detector is enabled.

### Bits 5:4 – FILTSEL[1:0]: Filter Selection

These bits select the LUT output filter options:

Filter Selection

Value	Name	Description
0x0	DISABLE	Filter disabled
0x1	SYNCH	Synchronizer enabled
0x2	FILTER	Filter enabled
0x3	-	Reserved

### Bit 1 – ENABLE: LUT Enable

Value	Description
0	The LUT is disabled.
1	The LUT is enabled.

### Bits 19:16,15:12,11:8 – INSELx: LUT Input x Source Selection

These bits select the LUT input x source:

Value	Name	Description
0x0	MASK	Masked input
0x1	FEEDBACK	Feedback input source
0x2	LINK	Linked LUT input source
0x3	EVENT	Event input source
0x4	IO	I/O pin input source
0x5	AC	AC input source
0x6	TC	TC input source
0x7	ALTTC	Alternative TC input source
0x8	TCC	TCC input source
0x9	SERCOM	SERCOM input source
0xA - 0xF	-	Reserved

## 42.8.9. Input Control

**Name:** INPUTCTRL

**Offset:** 0x08

**Reset:** 0x0000

**Property:** PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
				MUXNEG[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				MUXPOS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

### Bits 12:8 – MUXNEG[4:0]: Negative MUX Input Selection

These bits define the MUX selection for the negative ADC input.

Value	Name	Description
0x00	AIN0	ADC AIN0 pin
0x01	AIN1	ADC AIN1 pin
0x02	AIN2	ADC AIN2 pin
0x03	AIN3	ADC AIN3 pin
0x04	AIN4	ADC AIN4 pin
0x05	AIN5	ADC AIN5 pin
0x18	GND	Internal ground
0x19 - 0x1F	-	Reserved

### Bits 4:0 – MUXPOS[4:0]: Positive MUX Input Selection

These bits define the MUX selection for the positive ADC input. If the internal bandgap voltage or temperature sensor input channel is selected, then the Sampling Time Length bit group in the Sampling Control register must be written with a corresponding value.

Value	Name	Description
0x00	AIN0	ADC AIN0 pin
0x01	AIN1	ADC AIN1 pin
0x02	AIN2	ADC AIN2 pin
0x03	AIN3	ADC AIN3 pin
0x04	AIN4	ADC AIN4 pin
0x05	AIN5	ADC AIN5 pin



#### 42.8.11. Average Control

**Name:** AVGCTRL

**Offset:** 0x0C

**Reset:** 0x00

**Property:** PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
		ADJRES[2:0]				SAMPLENUM[3:0]		
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

##### Bits 6:4 – ADJRES[2:0]: Adjusting Result / Division Coefficient

These bits define the division coefficient in  $2^n$  steps.

##### Bits 3:0 – SAMPLENUM[3:0]: Number of Samples to be Collected

These bits define how many samples are added together. The result will be available in the Result register (RESULT). Note: if the result width increases, CTRLC.RESSEL must be changed.

Value	Description
0x0	1 sample
0x1	2 samples
0x2	4 samples
0x3	8 samples
0x4	16 samples
0x5	32 samples
0x6	64 samples
0x7	128 samples
0x8	256 samples
0x9	512 samples
0xA	1024 samples
0xB - 0xF	Reserved

### 43.6.13. Events

The AC can generate the following output events:

- Comparator (COMP0, COMP1): Generated as a copy of the comparator status
- Window (WIN0): Generated as a copy of the window inside/outside status

Writing a one to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables the corresponding output event. Writing a zero to this bit disables the corresponding output event. Refer to the Event System chapter for details on configuring the event system.

The AC can take the following action on an input event:

- Start comparison (START0, START1): Start a comparison.

Writing a one to an Event Input bit into the Event Control register (EVCTRL.COMPEIx) enables the corresponding action on input event. Writing a zero to this bit disables the corresponding action on input event. Note that if several events are connected to the AC, the enabled action will be taken on any of the incoming events. Refer to the Event System chapter for details on configuring the event system.

When EVCTRL.COMPEIx is one, the event will start a comparison on COMPx after the start-up time delay. In normal mode, each comparator responds to its corresponding input event independently. For a pair of comparators in window mode, either comparator event will trigger a comparison on both comparators simultaneously.

### 43.6.14. Sleep Mode Operation

The Run in Standby bits in the Comparator x Control registers (COMPCTRLx.RUNSTDBY) control the behavior of the AC during standby sleep mode. Each RUNSTDBY bit controls one comparator. When the bit is zero, the comparator is disabled during sleep, but maintains its current configuration. When the bit is one, the comparator continues to operate during sleep. Note that when RUNSTDBY is zero, the analog blocks are powered off for the lowest power consumption. This necessitates a start-up time delay when the system returns from sleep.

For Window Mode operation, both comparators in a pair must have the same RUNSTDBY configuration.

When RUNSTDBY is one, any enabled AC interrupt source can wake up the CPU. The AC can also be used during sleep modes where the clock used by the AC is disabled, provided that the AC is still powered (not in shutdown). In this case, the behavior is slightly different and depends on the measurement mode, as listed in [Table 43-1](#).

**Table 43-1. Sleep Mode Operation**

COMPCTRLx.MODE	RUNSTDBY=0	RUNSTDBY=1
0 (Continuous)	COMPx disabled	GCLK_AC stopped, COMPx enabled
1 (Single-shot)	COMPx disabled	GCLK_AC stopped, COMPx enabled only when triggered by an input event

#### 43.6.14.1. Continuous Measurement during Sleep

When a comparator is enabled in continuous measurement mode and GCLK\_AC is disabled during sleep, the comparator will remain continuously enabled and will function asynchronously. The current state of the comparator is asynchronously monitored for changes. If an edge matching the interrupt condition is found, GCLK\_AC is started to register the interrupt condition and generate events. If the interrupt is enabled in the Interrupt Enable registers (INTENCLR/SET), the AC can wake up the device;

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t <sub>STARTUP</sub>	Startup time	f=32.768kHz, C <sub>L</sub> =12.5pF	-	25k	82k	Cycles
P <sub>on</sub>	Drive Level <sup>(1)</sup>	-	-	-	0.1	μW

**Note:**

1. These values are based on simulation. They are not covered by production test limits or characterization.
2. For device revision A, see Erratum 13425.

**Table 46-49. Power Consumption<sup>(1)</sup>**

Symbol	Parameter	Conditions	T <sub>a</sub>	Min.	Typ.	Max.	Units
I <sub>DD</sub>	Current consumption	VCC=3.3V	Max 85°C Typ 25°C	-	311	723	nA

**Note:** (1) These values are based on characterization.

### 46.12.3. 32.768kHz Internal Oscillator (OSC32K) Characteristics

**Table 46-50. 32KHz RC Oscillator Electrical Characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output frequency	at 25°C, at V <sub>DDIO</sub> =3.3V	32.572	32.768	33.044	kHz
		at 25°C, over [1.62, 3.63]V	31.425	32.768	33.603	kHz
		over[-40,+85]°C, over [1.62, 3.63]V	28.581	32.768	34.716	kHz
I <sub>OSC32k</sub>	Current consumption		-	0.54		μA
T <sub>STARTUP</sub>	Startup time		-	1	2	cycles
Duty	Duty Cycle		-	50	-	%

**Note:** 1. These values are based on characterization.

**Table 46-51. Power Consumption<sup>(1)</sup>**

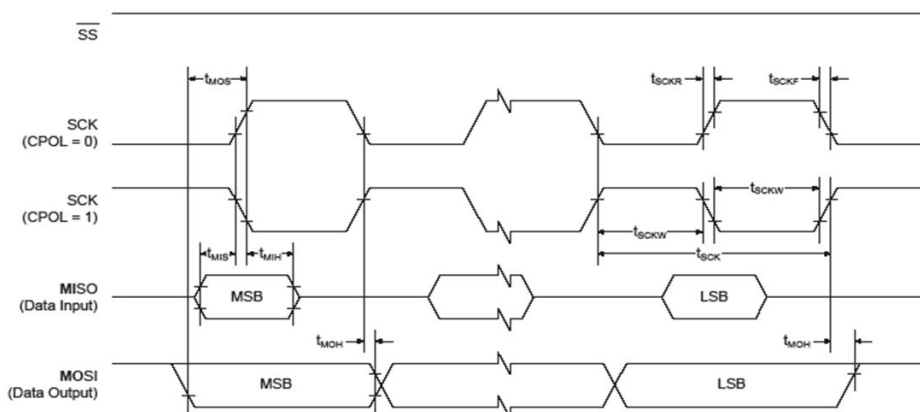
Symbol	Parameter	Conditions	T <sub>a</sub>	Min.	Typ.	Max.	Units
I <sub>DD</sub>	Current consumption	VCC=3.3V	Max 85°C Typ 25°C	-	0.54	1.10	μA

**Note:** (1) These values are based on characterization.

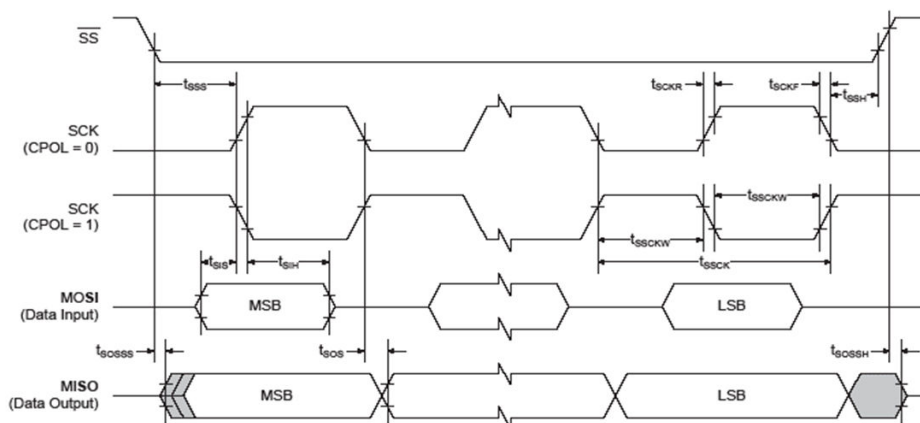
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SOS}$	MISO setup before SCK	Slave, VDD>2.70V	-	-	36.9	ns
		Slave, VDD>1.62V	-	-	47.5	
$t_{SOH}$	MISO hold after SCK	Slave, VDD>2.70V	11.5	-	-	
		Slave, VDD>1.62V	11.5	-	-	
$t_{SOSS}$	MISO setup after SS low	Slave, VDD>2.70V	-	-	31	
		Slave, VDD>1.62V	-	-	41.3	
$t_{SOSH}$	MISO hold after SS high	Slave, VDD>2.70V	6.2	-	-	
		Slave, VDD>1.62V	6.2	-	-	

**Note:** 1. These values are based on simulation. They are not covered by production test limits or characterization.

**Figure 46-7. SPI Timing Requirements in Master Mode**



**Figure 46-8. SPI Timing Requirements in Slave Mode**



### Maximum SPI Frequency

- Master Mode  
 $f_{SCKmax} = 1/2 * (t_{MIS} + t_{valid})$ , where  $t_{valid}$  is the slave time response to output data after detecting an SCK edge. For a non-volatile memory with  $t_{valid} = 12ns$  Max,  $f_{SPCKMax} = 9.8MHz$  @ VDDIO > 2.7V
- Slave Mode

DMAC – Direct Memory Access Controller	<ul style="list-style-type: none"> <li>Block diagram re-added.</li> <li>Editorial updates.</li> </ul>
PORT - I/O Pin Controller	<ul style="list-style-type: none"> <li>Editorial updates.</li> </ul>
OSCCTRL – Oscillators Controller	<ul style="list-style-type: none"> <li>Register DFLLCTRL: bit field descriptions added for BPLCKC and WAITLOCK.</li> <li>Editorial updates.</li> </ul>
SUPC – Supply Controller	Editorial updates.
NVMCTRL – Non-Volatile Memory Controller	BOOTPROT default value is 0x7 (0x3 for WLCSP64 package).
EVSYS – Event System	Editorial updates.
SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter	Recommended max. Rx Error explanation added to 'Asynchronous Operational Range'.
TC – Timer/Counter	<ul style="list-style-type: none"> <li>Registers PERBUF, CCBUFx are write-synchronized.</li> <li>Editorial updates.</li> </ul>
TCC – Timer/Counter for Control Applications	<ul style="list-style-type: none"> <li>In CAPTMIN mode, value 0 can be captured only in down-counting mode.</li> <li>In <a href="#">Counter Operation</a>: Section 'Stop Command and Event Action' split into 'Stop Command' and 'Pause Event Action'.</li> <li>RAMP2C Operation: figures added.</li> <li>COUNT register to be read-synchronized by user.</li> <li>Register presentation updated.</li> <li>Editorial updates.</li> </ul>
TRNG – True Random Number Generator	<ul style="list-style-type: none"> <li>Block diagram updated</li> </ul>
USB – Universal Serial Bus	<ul style="list-style-type: none"> <li>Editorial updates.</li> </ul>
ADC – Analog-to-Digital Converter	Editorial updates.
DAC – Digital-to-Analog Converter	Editorial updates.
PTC - Peripheral Touch Controller	Editorial updates.
Maximum Clock Frequencies	Unit for maximum clock frequency $f_{GCLK\_DFLL48M\_REF}$ is kHz.