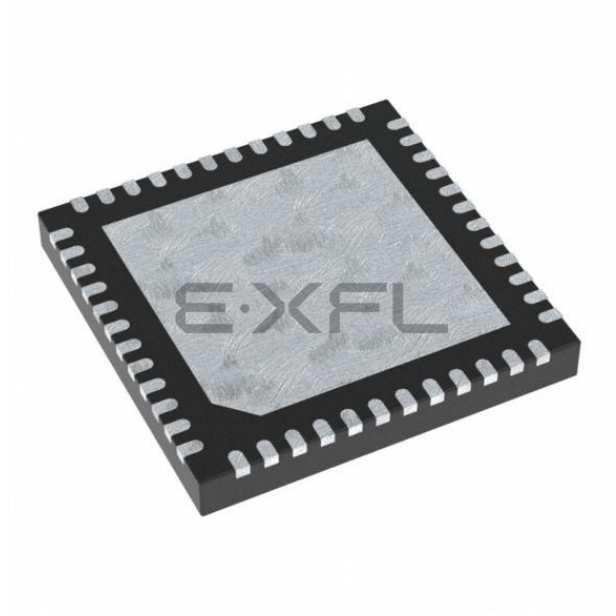

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml21g16b-mnt

3.2. SAM L21G

Table 3-2. SAM L21G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML21G16B-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML21G16B-MUT			QFN48	
ATSAML21G17B-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML21G17B-MUT			QFN48	
ATSAML21G18B-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML21G18B-MUT			QFN48	

3.3. SAM L21E

Table 3-3. SAM L21E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML21E15B-AUT	32K	4K	TQFP32	Tape & Reel
ATSAML21E15B-MUT			QFN32	
ATSAML21E16B-AUT	64K	8K	TQFP32	Tape & Reel
ATSAML21E16B-MUT			QFN32	
ATSAML21E17B-AUT	128K	16K	TQFP32	Tape & Reel
ATSAML21E17B-MUT			QFN32	
ATSAML21E18B-AUT	256K	32K	TQFP32	Tape & Reel
ATSAML21E18B-MUT			QFN32	

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L21 variants have a reset value of DID=0x1081drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 3-4. SAM L21 Device Identification Values

DEVSEL (DID[7:0])	Device
0x00	SAML21J18A
0x01	SAML21J17A
0x02	SAML21J16A
0x03-0x04	Reserved
0x05	SAML21G18A

Table 11-3. RWW Section Parameters[1]

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML21x18	8	128	64
SAML21x17	4	64	64
SAML21x16	2	32	64
SAML21E15	1	16	64

Note: 1. x = G, J, or E.

11.3. NVM User Row Mapping

The Non Volatile Memory (NVM) User Row contains calibration data that are automatically read at device power-on.

The NVM User Row can be read at address 0x00804000.

To write the NVM User Row refer to the documentation of the NVMCTRL - Non-Volatile Memory Controller.

Note: When writing to the User Row, the new values do not get loaded by the other peripherals on the device until a device Reset occurs.

Table 11-4. NVM User Row Mapping

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
2:0	BOOTPROT	Used to select one of eight different bootloader sizes.	0x7	NVMCTRL
3	Reserved	—	0x1	—
6:4	EEPROM	Used to select one of eight different EEPROM sizes.	0x7	NVMCTRL
7	Reserved	—	0x1	—
13:8	BOD33 Level	BOD33 threshold level at power-on.	0x06	SUPC.BOD33
14	BOD33 Disable	BOD33 Disable at power-on.	0x0	SUPC.BOD33
16:15	BOD33 Action	BOD33 Action at power-on.	0x1	SUPC.BOD33
25:17	Reserved	Factory settings - do not change.	0x08F	-
26	WDT Enable	WDT Enable at power-on.	0x0	WDT.CTRLA
27	WDT Always-On	WDT Always-On at power-on.	0x0	WDT.CTRLA
31:28	WDT Period	WDT Period at power-on.	0xB	WDT.CONFIG
35:32	WDT Window	WDT Window mode time-out at power-on.	0xB	WDT.CONFIG
39:36	WDT EWOFFSET	WDT Early Warning Interrupt Time Offset at power-on.	0xB	WDT.EWCTRL

12.2. Nested Vector Interrupt Controller

12.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM L21 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (http://www.arm.com).

12.2.2. Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

An interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a 1 to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing 1 to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

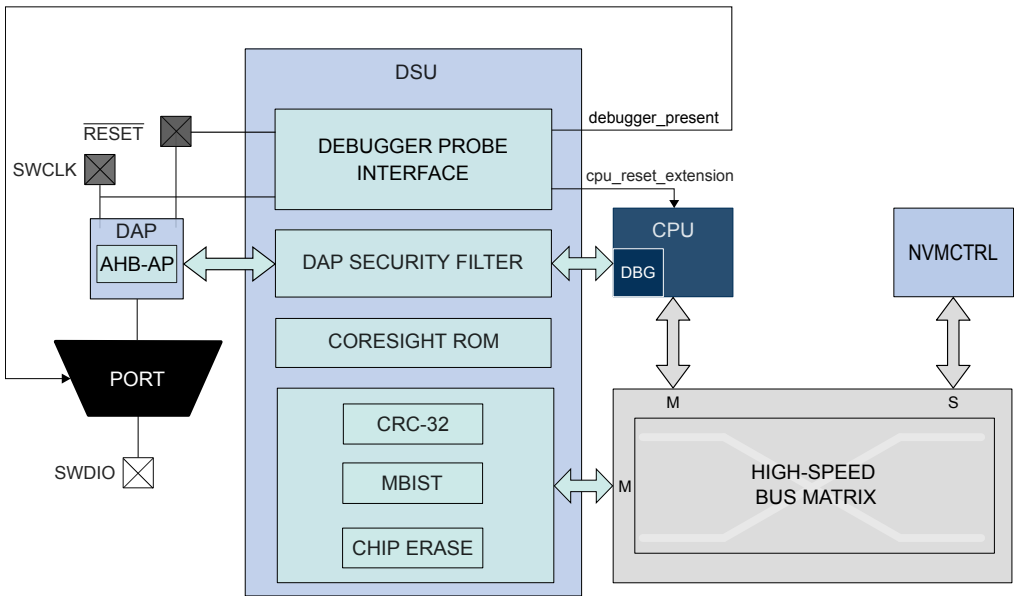
For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 12-3. Interrupt Line Mapping

Peripheral source	NVIC line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager MCLK - Main Clock OSCCTRL - Oscillators Controller OSC32KCTRL - 32KHz Oscillators Controller SUPC - Supply Controller PAC - Protecion Access Controller	0
WDT – Watchdog Timer	1
RTC – Real Time Counter	2
EIC – External Interrupt Controller	3
NVMCTRL – Non-Volatile Memory Controller	4
DMAC - Direct Memory Access Controller	5
USB - Universal Serial Bus	6
EVSYS – Event System	7

15.3. Block Diagram

Figure 15-1. DSU Block Diagram



15.4. Signal Description

The DSU uses three signals to function.

Signal Name	Type	Description
$\overline{\text{RESET}}$	Digital Input	External reset
SWCLK	Digital Input	SW clock
SWDIO	Digital I/O	SW bidirectional data pin

Related Links

I/O Multiplexing and Considerations on page 30

15.5. Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

15.5.1. IO Lines

The SWCLK pin is by default assigned to the DSU module to allow debugger probe detection and to stretch the CPU reset phase. For more information, refer to Debugger Probe Detection. The Hot-Plugging feature depends on the PORT configuration. If the SWCLK pin function is changed in the PORT or if the PORT_MUX is disabled, the Hot-Plugging feature is disabled until a power-reset or an external reset.

15.5.2. Power Management

The DSU will continue to operate in any sleep mode where the selected source clock is running.

Related Links

PM – Power Manager on page 192

23.6.2.2. Enabling, Disabling, and Resetting

The voltage reference output is enabled/disabled by setting/clearing the Voltage Reference Output Enable bit in the Voltage Reference register (VREF.VREFOE).

The temperature sensor is enabled/disabled by setting/clearing the Temperature Sensor Enable bit in the Voltage Reference register (VREF.TSEN).

Note: When VREF.ONDEMAND=0, it is not recommended to enable both voltage reference output and temperature sensor at the same time - only the voltage reference output will be present at both ADC inputs.

23.6.2.3. Selecting a Voltage Reference

The Voltage Reference Selection bit field in the VREF register (VREF.SEL) selects the voltage of INTREF to be applied to analog modules, e.g. the ADC.

23.6.2.4. Sleep Mode Operation

The Voltage Reference output and the Temperature Sensor output behavior during sleep mode can be configured using the Run in Standby bit and the On Demand bit in the Voltage Reference register (VREF.RUNSTDBY, VREF.ONDEMAND), see the following table:

Table 23-2. VREF Sleep Mode Operation

VREF.ONDEMAND	VREF.RUNSTDBY	Voltage Reference Sleep behavior
-	-	Disable
0	0	Always run in all sleep modes *except* standby sleep mode
0	1	Always run in all sleep modes *including* standby sleep mode
1	0	Only run if requested by the ADC, in all sleep modes *except* standby sleep mode
1	1	Only run if requested by the ADC, in all sleep modes *including* standby sleep mode

23.6.3. Battery Backup Power Switch

23.6.3.1. Initialization

The Battery Backup Power Switch (BBPS) is disabled at power-up, and the backup domain is supplied by main power.

23.6.3.2. Forced Battery Backup Power Switch

The Backup domain is always supplied by the VBAT supply pin when the Configuration bit field in the Battery Backup Power Switch Control register (BBPS.CONF) is written to 0x2 (FORCED).

23.6.3.3. Automatic Battery Backup Power Switch

The supply of the backup domain can be switched automatically to VBAT supply pin by the Automatic Power Switch or by using the BOD33.

The supply of the backup domain can be switched automatically to VDD supply pin either by the Automatic Power Switch or the Main Power Pin when VDD and VDDCORE are restored.

Automatic Power Switch (APWS)

When the Configuration bit field in the Battery Backup Power Switch register (BBPS.CONF) is selecting the APWS, the Automatic Power Switch will function as Battery Backup Power Switch.

The Automatic Power switch allows to switch the supply of the backup domain from VDD to VBAT power and vice-versa.

25.10.3. Interrupt Enable Clear in COUNT16 mode (CTRLA.MODE=1)

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Name: INTENCLR
Offset: 0x08
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
	OVF						CMP1	CMP0
Access	R/W						R/W	R/W
Reset	0						0	0

Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF: Overflow Interrupt Enable
Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bits 9:8 – CMPn: Compare n Interrupt Enable [n = 1..0]
Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Compare n Interrupt Enable bit, which disables the Compare n interrupt.

Value	Description
0	The Compare n interrupt is disabled.
1	The Compare n interrupt is enabled.

Bits 7:0 – PERn: Periodic Interval n Interrupt Enable [n = 7..0]
Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Periodic Interval n Interrupt Enable bit, which disables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

26.8.3. CRC Data Input

Name: CRCDATAIN
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	CRCDATAIN[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CRCDATAIN[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CRCDATAIN[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCDATAIN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CRCDATAIN[31:0]: CRC Data Input
These bits store the data for which the CRC checksum is computed. A new CRC Checksum is ready (CRCBEAT+ 1) clock cycles after the CRCDATAIN register is written.

26.8.19. Channel Control B

This register affects the DMA channel that is selected in the Channel ID register (CHID.ID).

Name: CHCTRLB
Offset: 0x44
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
							CMD[1:0]	
Access							R/W	R/W
Reset							0	0

Bit	23	22	21	20	19	18	17	16
	TRIGACT[1:0]							
Access	R/W	R/W						
Reset	0	0						

Bit	15	14	13	12	11	10	9	8
			TRIGSRC[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		LVL[1:0]		EVOE	EVIE	EVACT[2:0]		
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 25:24 – CMD[1:0]: Software Command
These bits define the software commands. Refer to Channel Suspend and Channel Resume and Next Suspend Skip.

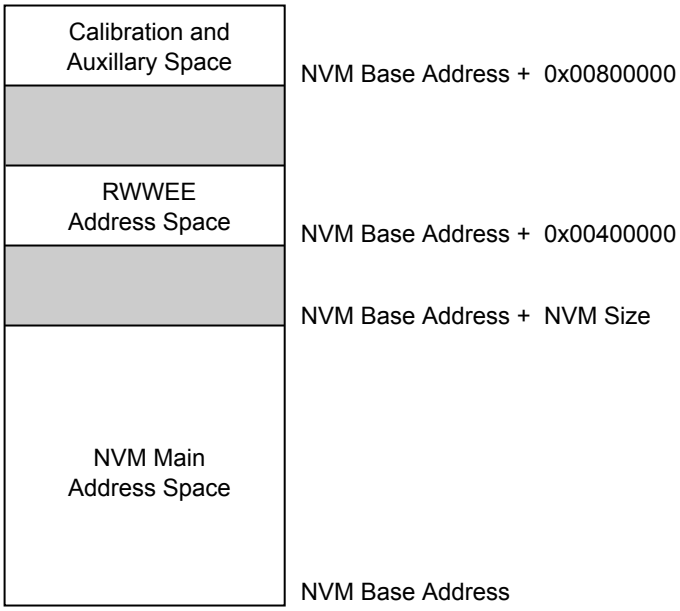
These bits are not enable-protected.

CMD[1:0]	Name	Description
0x0	NOACT	No action
0x1	SUSPEND	Channel suspend operation
0x2	RESUME	Channel resume operation
0x3	-	Reserved

Bits 23:22 – TRIGACT[1:0]: Trigger Action
These bits define the trigger action used for a transfer.

TRIGACT[1:0]	Name	Description
0x0	BLOCK	One trigger required for each block transfer
0x1	-	Reserved

Figure 28-3. NVM Memory Organization



The lower rows in the NVM main address space can be allocated as a boot loader section by using the BOOTPROT fuses, and the upper rows can be allocated to EEPROM, as shown in the figure below.

The boot loader section is protected by the lock bit(s) corresponding to this address space and by the BOOTPROT[2:0] fuse. The EEPROM rows can be written regardless of the region lock status.

The number of rows protected by BOOTPROT is given in Boot Loader Size, the number of rows allocated to the EEPROM are given in EEPROM Size.

32.7. Register Summary

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
0x01		15:8	SAMPR[2:0]							IBON
0x02		23:16	SAMPA[1:0]		RXPO[1:0]				TXPO[1:0]	
0x03		31:24		DORD	CPOL	CMODE	FORM[3:0]			
0x04	CTRLB	7:0		SBMODE				CHSIZE[2:0]		
0x05		15:8			PMODE			ENC	SFDE	COLDEN
0x06		23:16							RXEN	TXEN
0x07		31:24								
0x08 ... 0x0B	Reserved									
0x0C	BAUD	7:0	BAUD[7:0]							
0x0D		15:8	BAUD[15:8]							
0x0E	RXPL	7:0	RXPL[7:0]							
0x0F ... 0x13	Reserved									
0x14	INTENCLR	7:0	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
0x15	Reserved									
0x16	INTENSET	7:0	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
0x19	Reserved									
0x1A	STATUS	7:0			COLL	ISF	CTS	BUFOVF	FERR	PERR
0x1B		15:8								
0x1C	SYNCBUSY	7:0						CTRLB	ENABLE	SWRST
0x1D		15:8								
0x1E		23:16								
0x1F		31:24								
0x20 ... 0x27	Reserved									
0x28	DATA	7:0	DATA[7:0]							
0x29		15:8								DATA[8:8]
0x2A ... 0x2F	Reserved									
0x30	DBGCTRL	7:0								DBGSTOP

32.8. Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

DOPO	DO	SCK	Slave $\overline{SS}$	Master $\overline{SS}$
0x0	PAD[0]	PAD[1]	PAD[2]	System configuration
0x1	PAD[2]	PAD[3]	PAD[1]	System configuration
0x2	PAD[3]	PAD[1]	PAD[2]	System configuration
0x3	PAD[0]	PAD[3]	PAD[1]	System configuration

Bit 8 – IBON: Immediate Buffer Overflow Notification
This bit controls when the buffer overflow status bit (STATUS.BUFOVF) is set when a buffer overflow occurs.

This bit is not synchronized.

Value	Description
0	STATUS.BUFOVF is set when it occurs in the data stream.
1	STATUS.BUFOVF is set immediately upon buffer overflow.

Bit 7 – RUNSTDBY: Run In Standby
This bit defines the functionality in standby sleep mode.

These bits are not synchronized.

RUNSTDBY	Slave	Master
0x0	Disabled. All reception is dropped, including the ongoing transaction.	Generic clock is disabled when ongoing transaction is finished. All interrupts can wake up the device.
0x1	Ongoing transaction continues, wake on Receive Complete interrupt.	Generic clock is enabled while in sleep modes. All interrupts can wake up the device.

Bits 4:2 – MODE[2:0]: Operating Mode
These bits must be written to 0x2 or 0x3 to select the SPI serial communication interface of the SERCOM.

0x2: SPI slave operation

0x3: SPI master operation

These bits are not synchronized.

Bit 1 – ENABLE: Enable
Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the Synchronization Enable Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

Related Links

PM – Power Manager on page 192

34.5.3. Clocks

The SERCOM bus clock (CLK_SERCOMx_APB) is enabled by default, and can be enabled and disabled in the Main Clock Controller and the Power Manager.

Two generic clocks ared used by SERCOM, GCLK_SERCOMx_CORE and GCLK_SERCOM_SLOW. The core clock (GCLK_SERCOMx_CORE) can clock the I^2C when working as a master. The slow clock (GCLK_SERCOM_SLOW) is required only for certain functions, e.g. SMBus timing. These clocks must be configured and enabled in the Generic Clock Controller (GCLK) before using the I^2C.

These generic clocks are asynchronous to the bus clock (CLK_SERCOMx_APB). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

GCLK - Generic Clock Controller on page 133

Peripheral Clock Masking on page 157

PM – Power Manager on page 192

34.5.4. DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first. Refer to *DMAC – Direct Memory Access Controller* for details.

Related Links

DMAC – Direct Memory Access Controller on page 406

34.5.5. Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller on page 52

34.5.6. Events

Not applicable.

34.5.7. Debug Operation

When the CPU is halted in debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

Refer to the DBGCTRL register for details.

34.5.8. Register Access Protection

Registers with write-access can be write-protected optionally by the peripheral access controller (PAC).

PAC Write-Protection is not available for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)

Table 34-2. Module Request for SERCOM I²C Master

Condition	Request		
	DMA	Interrupt	Event
Data needed for transmit (TX) (Master transmit mode)	Yes (request cleared when data is written)		NA
Data needed for transmit (RX) (Master transmit mode)	Yes (request cleared when data is read)		
Master on Bus (MB)		Yes	
Stop received (SB)		Yes	
Error (ERROR)		Yes	

34.6.4.1. DMA Operation

Smart mode must be enabled for DMA operation in the Control B register by writing CTRLB.SMEN=1.

Slave DMA

When using the I²C slave with DMA, an address match will cause the address interrupt flag (INTFLAG.ADDRMATCH) to be raised. After the interrupt has been serviced, data transfer will be performed through DMA.

The I²C slave generates the following requests:

- Write data received (RX): The request is set when master write data is received. The request is cleared when DATA is read.
- Read data needed for transmit (TX): The request is set when data is needed for a master read operation. The request is cleared when DATA is written.

Master DMA

When using the I²C master with DMA, the ADDR register must be written with the desired address (ADDR.ADDR), transaction length (ADDR.LEN), and transaction length enable (ADDR.LENEN). When ADDR.LENEN is written to 1 along with ADDR.ADDR, ADDR.LEN determines the number of data bytes in the transaction from 0 to 255. DMA is then used to transfer ADDR.LEN bytes followed by an automatically generated NACK (for master reads) and a STOP.

If a NACK is received by the slave for a master write transaction before ADDR.LEN bytes, a STOP will be automatically generated and the length error (STATUS.LENERR) will be raised along with the INTFLAG.ERROR interrupt.

The I²C master generates the following requests:

- Read data received (RX): The request is set when master read data is received. The request is cleared when DATA is read.
- Write data needed for transmit (TX): The request is set when data is needed for a master write operation. The request is cleared when DATA is written.

34.6.4.2. Interrupts

The I²C slave has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any sleep mode:

- Error (ERROR)

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Offset	Name	Bit Pos.								
0x1C	INTFLAG	7:0	RAMACER	UPRSM	DNRSM	WAKEUP	RST	HSOF		
0x1D		15:8							DDISC	DCONN
0x1E	Reserved									
0x1F	Reserved									
0x20	PINTSMRY	7:0	PINT[7:0]							
0x21		15:8	PINT[15:8]							
0x22	Reserved									
0x23										

Table 39-6. Host Pipe Register n

Offset	Name	Bit Pos.								
0x1m0	PCFGn	7:0			PTYPE[2:0]			BK	PTOKEN[1:0]	
0x1m1	Reserved									
0x1m2	Reserved									
0x1m3	BINTERVAL	7:0	BINTERVAL[7:0]							
0x1m4	PSTATUSCLRn	7:0	BK1RDY	BK0RDY		PFREEZE		CURBK		DTGL
0x1m5	PSTATUSETn	7:0	BK1RDY	BK0RDY		PFREEZE		CURBK		DTGL
0x1m6	PSTATUSn	7:0	BK1RDY	BK0RDY		PFREEZE		CURBK		DTGL
0x1m7	PINTFLAGn	7:0			STALL	TXSTP	PERR	TRFAIL	TRCPT1	TRCPT0
0x1m8	PINTENCLRn	7:0			STALL	TXSTP	PERR	TRFAIL	TRCPT1	TRCPT0
0x1m9	PINTENSETn	7:0			STALL	TXSTP	PERR	TRFAIL	TRCPT1	TRCPT0
0x1mA	Reserved									
0x1mB	Reserved									

Table 39-7. Host Pipe n Descriptor Bank 0

Offset 0x n0 + index	Name	Bit Pos.								
0x00	ADDR	7:0	ADD[7:0]							
0x01		15:8	ADD[15:8]							
0x02		23:16	ADD[23:16]							
0x03		31:24	ADD[31:24]							
0x04	PCKSIZE	7:0	BYTE_COUNT[7:0]							
0x05		15:8	MULTI_PACKET_SIZE[1:0]		BYTE_COUNT[13:8]					
0x06		23:16	MULTI_PACKET_SIZE[9:2]							
0x07		31:24	AUTO_ZLP	SIZE[2:0]			MULTI_PACKET_SIZE[13:10]			
0x08	EXTREG	7:0	VARIABLE[3:0]				SUBPID[3:0]			
0x09		15:8		VARIABLE[10:4]						
0x0A	STATUS_BK	7:0							ERRORFLOW	CRCERR
0x0B		15:8								
0x0C	CTRL_PIPE	7:0		PDADDR[6:0]						
0x0D		15:8	PEPMAX[3:0]				PEPNUM[3:0]			
0x0E	STATUS_PIPE	7:0	ERCNT[2:0]			CRC16ER	TOUTER	PIDER	DAPIDER	DTGLER
0x0F		15:8								

39.8.2.6. Device Interrupt Enable Set

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Name: INTENSET
Offset: 0x18
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
							LPMSUSP	LPMNYET
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RAMACER	UPRSM	EORSM	WAKEUP	EORST	SOF		SUSPEND
Access	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0		0

Bit 9 – LPMSUSP: Link Power Management Suspend Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Link Power Management Suspend Enable bit and enable the corresponding interrupt request.

Value	Description
0	The Link Power Management Suspend interrupt is disabled.
1	The Link Power Management Suspend interrupt is enabled.

Bit 8 – LPMNYET: Link Power Management Not Yet Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Link Power Management Not Yet interrupt bit and enable the corresponding interrupt request.

Value	Description
0	The Link Power Management Not Yet interrupt is disabled.
1	The Link Power Management Not Yet interrupt is enabled.

Bit 7 – RAMACER: RAM Access Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the RAM Access Enable bit and enable the corresponding interrupt request.

Value	Description
0	The RAM Access interrupt is disabled.
1	The RAM Access interrupt is enabled.

Signal	Description	Type
OA1NEG	OPAMP1 negative input	Analog input
OA2POS	OPAMP2 positive input	Analog input
OA2NEG	OPAMP2 negative input	Analog input
OA0OUT	OPAMP0 output	Analog output
OA1OUT	OPAMP1 output	Analog output
OA2OUT	OPAMP2 output	Analog output

One signal can be mapped on several pins.

Important:
When an analog peripheral is enabled, the analog output of the peripheral will interfere with the alternative functions of the output pads. This is also true even when the peripheral is used for internal purposes.

Analog inputs do not interfere with alternative pad functions.

Related Links

I/O Multiplexing and Considerations on page 30

41.5. Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

41.5.1. I/O Lines

Using the OPAMP I/O lines requires the I/O pins to be configured. Refer to the *PORT - I/O Pin Controller* chapter for details.

41.5.2. Power Management

The OPAMP can operate in idle and standby sleep mode, according to the settings of the Run in Standby and On Demand bits in the OPAMP Control x registers (OPAMPCTRLx.RUNSTDBY and OPAMPCTRLx.ONDEMAND), as well as the Enable bit in the Control A register (CTRLA.ENABLE). Refer to *PM – Power Manager* for details on the different sleep modes.

Related Links

PM – Power Manager on page 192

41.5.3. Clocks

The OPAMP bus clock (CLK_OPAMP_APB) can be enabled and disabled in the Power Manager, and the default state of CLK_OPAMP_APB can be found in the *Peripheral Clock Masking*.

A clock (CLK_ULP32K) is required by the voltage doubler for low voltage operation (VCC < 2.5V). The CLK_ULP32K is a 32KHz clock which is provided by the OSCULP32K oscillator in the OSC32KCTRL module.

Related Links

Peripheral Clock Masking on page 157

Bits 18:16 – MUXPOS[2:0]: Positive Input Mux Selection
Selection on positive input for operational amplifier x.

Value	OPAMPx	Name	Description
0x0	x=0,1,2	OAxPOS	Positive I/O pin
0x1	x=0,1,2	OAxTAP	Resistor ladder x taps
0x2	x=0	DAC	DAC output
	x=1	OA0OUT	OPAMP0 output
	x=2	OA1OUT	OPAMP1 output
0x3	x=0,1,2	GND	Ground
0x4	x=0,1	Reserved	
	x=2	OA0POS	Positive I/O pin OPA0
0x5	x=0,1	Reserved	
	x=2	OA1POS	Positive I/O pin OPA1
0x6	x=0,1	Reserved	
	x=2	OA0TAP	Resistor ladder 0 taps
0x7	x=0,1,2	Reserved	

Bits 15:13 – POTMUX[2:0]: Potentiometer selection
Resistor selection bits control a numeric potentiometer with eight fixed values.

Value	R1	R2	Gain = R2/R1
0x0	14R	2R	1/7
0x1	12R	4R	1/3
0x2	8R	8R	1
0x3	6R	10R	1 + 2/3
0x4	4R	12R	3
0x5	3R	13R	4 + 1/3
0x6	2R	14R	7
0x7	R	15R	15

Bits 12:11 – RES1MUX[1:0]: Resistor 1 Mux
These bits select the connection of R1 resistor of the potentiometer.

Value	OPAMPx	Name	Description
0x0	x=0,1,2	OAxPOS	Positive inout of OPAMPx
0x1	x=0,1,2	OAxNEG	Negative input of OPAMPx

44.8.6. Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					EMPTY1	EMPTY0	UNDERRUN1	UNDERRUN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – EMPTY1: Data Buffer 1 Empty
This flag is cleared by writing a '1' to it or by writing new data to DATA1 or DATABUF1.

This flag is set when the data buffer for DAC1 is empty and will generate an interrupt request if INTENCLR/INTENSET.EMPTY1=1.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Data Buffer 1 Empty interrupt flag.

Bit 2 – EMPTY0: Data Buffer 0 Empty
This flag is cleared by writing a '1' to it or by writing new data to DATA0 or DATABUF0.

This flag is set when the data buffer for DAC0 is empty and will generate an interrupt request if INTENCLR/INTENSET.EMPTY0=1.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Data Buffer 0 Empty interrupt flag.

Bit 1 – UNDERRUN1: DAC1 Underrun
This flag is cleared by writing a '1' to it.

This flag is set when a start conversion event (START1) occurred before new data is copied/written to the DAC1 data buffer and will generate an interrupt request if INTENCLR/INTENSET.UNDERRUN1=1.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the DAC1 Underrun interrupt flag.

Bit 0 – UNDERRUN0: DAC0 Underrun
This flag is cleared by writing a '1' to it.

This flag is set when a start conversion event (START0) occurred before new data is copied/written to the DAC) data buffer and will generate an interrupt request if INTENCLR/INTENSET.UNDERRUN0=1.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the DAC0 Underrun interrupt flag.

Symbol	Parameters	Conditions	Min.	Typ	Max.	Unit
V_{scale}(2)	INL			0.34		LSB
	DNL			0.06		
	Offset Error			0.1		
	Gain Error			1.22		

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.
2. These values are based on characterization.

Table 46-31. Power Consumption(1)

Symbol	Parameters	Conditions	Ta	Min.	Typ	Max.	Unit
I_{DDANA}	Current consumption $V_{CM}=V_{DDANA}/2$, +/-100mV overdrive from V_{CM}, voltage scaler disabled	COMPCTRLn.SPEED=0x0, V_{DDANA}=3.3V	Max.85°C Typ.25°C	-	50	1973	nA
		COMPCTRLn.SPEED=0x1, V_{DDANA}=3.3V		-	156	2082	
		COMPCTRLn.SPEED=0x2, V_{DDANA}=3.3V		-	289	2223	
		COMPCTRLn.SPEED=0x3, V_{DDANA}=3.3V		-	549	2495	
	Current consumption Voltage Scaler only	V_{DDANA}=3.3V		-	13	17	µA

Note:

1. These values are based on characterization.