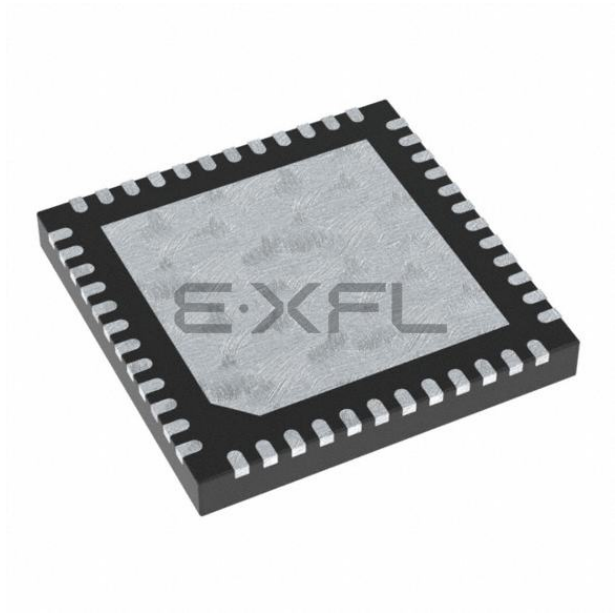

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml21g16b-mut

19.8.1. Reset Cause

When a Reset occurs, the bit corresponding to the Reset source is set to '1' and all other bits are written to '0'.

Name: RCAUSE
Offset: 0x00
Reset: Latest Reset Source
Property: –

Bit	7	6	5	4	3	2	1	0
	BACKUP	SYST	WDT	EXT		BOD33	BOD12	POR
Access	R	R	R	R		R	R	R
Reset	x	x	x	x		x	x	x

Bit 7 – BACKUP: Backup Reset
This bit is set if a Backup Reset has occurred. Refer to BKUPEXIT register to identify the source of the Backup Reset.

Bit 6 – SYST: System Reset Request
This bit is set if a System Reset Request has occurred. Refer to the Cortex processor documentation for more details.

Bit 5 – WDT: Watchdog Reset
This bit is set if a Watchdog Timer Reset has occurred.

Bit 4 – EXT: External Reset
This bit is set if an external Reset has occurred.

Bit 2 – BOD33: Brown Out 33 Detector Reset
This bit is set if a BOD33 Reset has occurred.

Bit 1 – BOD12: Brown Out 12 Detector Reset
This bit is set if a BOD12 Reset has occurred.

Bit 0 – POR: Power On Reset
This bit is set if a POR has occurred.

19.8.2. Backup Exit Source

When a Backup Reset occurs, the bit corresponding to the exit condition is set to '1', the other bits are written to '0'.

In some specific cases, the RTC and BBPS bits can be set together, e.g. when the device leaves the battery Backup Mode caused by a BBPS condition, and a RTC event was generated during the Battery Backup Mode period.

Name: BKUPEXIT
Offset: 0x02
Reset: Latest Backup Exit Source
Property: –

Bit	7	6	5	4	3	2	1	0
						BBPS	RTC	EXTWAKE
Access						R	R	R
Reset						x	x	x

Bit 2 – BBPS: Battery Backup Power Switch
This bit is set if the Battery Backup Power Switch of the Supply Controller changes back from battery mode to main power mode.

Bit 1 – RTC: Real Timer Counter Interrupt
This bit is set if an RTC interrupt flag is set in Backup Mode.

Bit 0 – EXTWAKE: External Wake-up
This bit is set if the wake-up detector has detected an external wake-up condition in Backup Mode.

Note: Once the DFLL48M is enabled in on-demand mode (DFLLCTRL.ONDEMAND=1), the STATUS.DFLLRDY bit will keep to '0' until the DFLL48M is requested by a peripheral.

Before writing to any of the DFLL48M control registers, the user must check that the DFLL Ready bit (STATUS.DFLLRDY) is set to '1'. When this bit is set, the DFLL48M can be configured and CLK_DFLL48M is ready to be used. Any write to any of the DFLL48M control registers while DFLLRDY is '0' will be ignored.

In order to read from the DFLLVAL register in closed loop mode, the user must request a read synchronization by writing a '1' to the Read Request bit in the DFLL Synchronization register (DFLLSYNC.READREQ). This is required because the DFLL controller may change the content of the DFLLVAL register any time. If a read operation is issued while the DFLL controller is updating the DFLLVAL content, a zero will be returned.

Note: Issuing a read on any register while a write-synchronization is still on-going will return a zero.

Read-Synchronized registers using DFLLSYNC.READREQ:

- DFLL48M Value register (DFLLVAL)

Write-Synchronized registers:

- DFLL48M Control register (DFLLCTRL)
- DFLL48M Value register (DFLLVAL)
- DFLL48M Multiplier register (DFLLMUL)

DPLL96M

Due to the multiple clock domains, some registers in the DPLL96M must be synchronized when accessed.

When executing an operation that requires synchronization, the relevant synchronization bit in the Synchronization Busy register (DPLLSYNCBUSY) will be set immediately, and cleared when synchronization is complete.

The following bits need synchronization when written:

- Enable bit in control register A (DPLLCTRLA.ENABLE)
- DPLL Ratio register (DPLLRATIO)
- DPLL Prescaler register (DPLLPRESC)

Related Links

Register Synchronization on page 129

22.8.1. Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Name: INTENCLR
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							OSC32KRDY	XOSC32KRDY
Access							R/W	R/W
Reset							0	0

Bit 1 – OSC32KRDY: OSC32K Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the OSC32K Ready Interrupt Enable bit, which disables the OSC32K Ready interrupt.

Value	Description
0	The OSC32K Ready interrupt is disabled.
1	The OSC32K Ready interrupt is enabled.

Bit 0 – XOSC32KRDY: XOSC32K Ready Interrupt Enable
Writing a '0' to this bit has no effect.

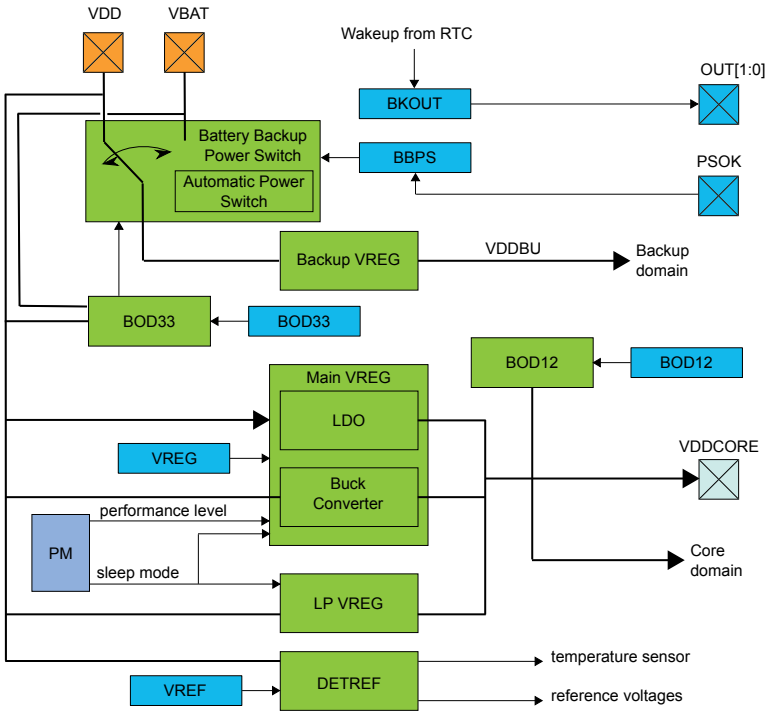
Writing a '1' to this bit will clear the XOSC32K Ready Interrupt Enable bit, which disables the XOSC32K Ready interrupt.

Value	Description
0	The XOSC32K Ready interrupt is disabled.
1	The XOSC32K Ready interrupt is enabled.

        - Sampled mode for low power applications with programmable sample frequency
    - Hysteresis value from Flash User Calibration
    - Monitor VDD or VBAT
- 1.2V Brown-Out Detector (BOD12)
    - Internal non-configurable Brown-Out Detector
- Output pins
    - Pin toggling on RTC event

23.3. Block Diagram

Figure 23-1. SUPC Block Diagram



23.4. Signal Description

Signal Name	Type	Description
OUT[1:0]	Digital Output	SUPC Outputs
PSOK	Digital Input	Main Power Supply OK

One signal can be mapped on several pins.

Related Links

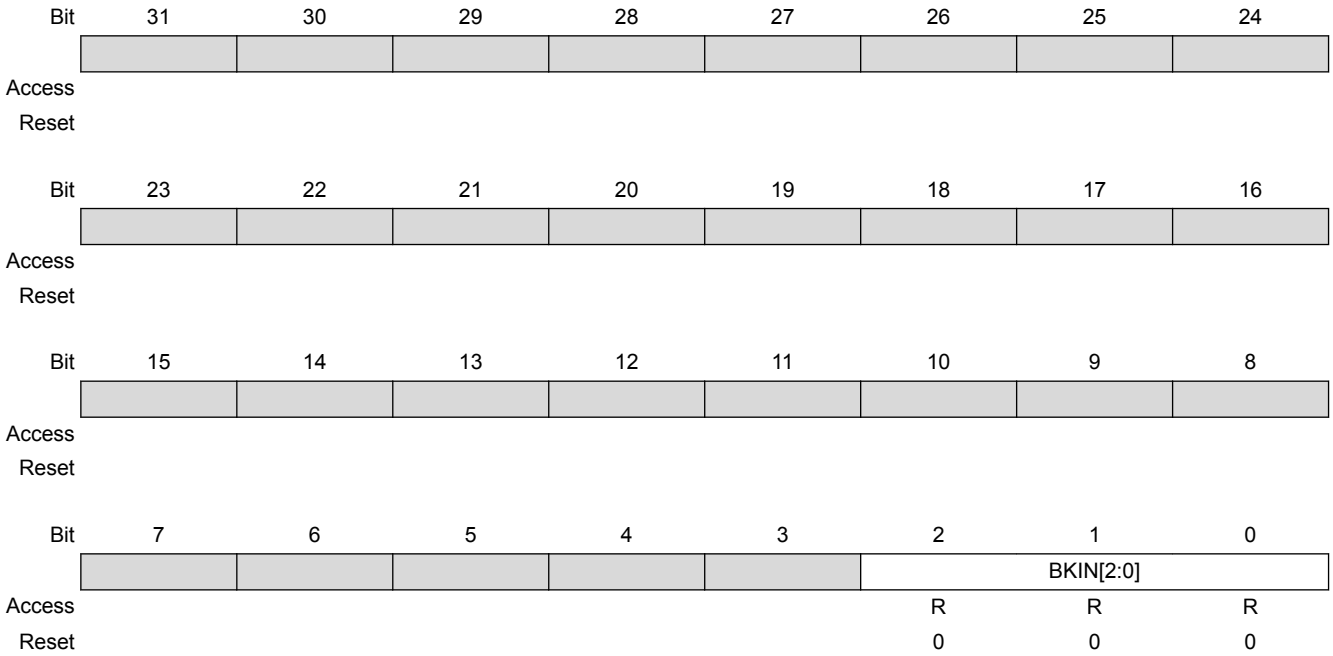
I/O Multiplexing and Considerations on page 30

23.5. Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

23.8.11. Backup Input (BKIN) Value

Name: BKIN
Offset: 0x28
Reset: 0x0000
Property: -



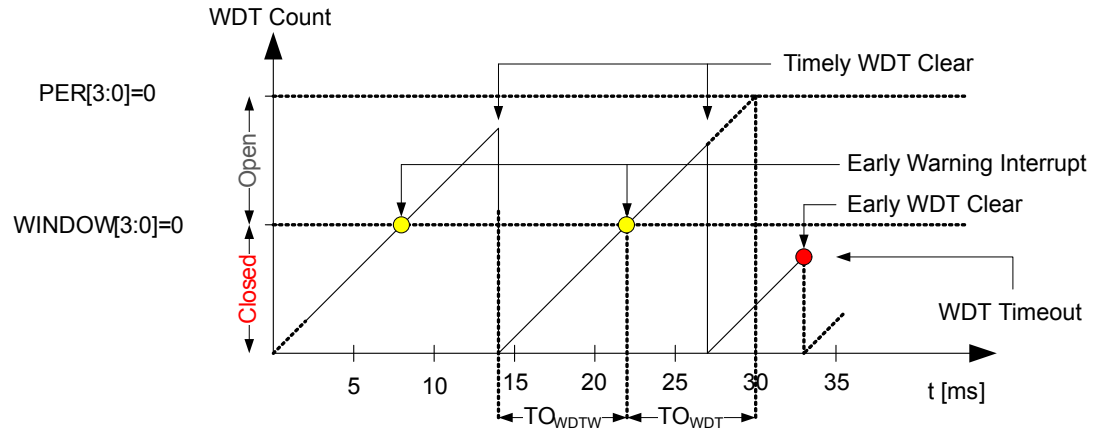
Bits 2:0 – BKIN[2:0]: Backup I/O Data Input Value
These bits are cleared when the corresponding backup I/O pin detects a logical low level on the input pin or when the backup I/O is not enabled.

These bits are set when the corresponding backup I/O pin detects a logical high level on the input pin when the backup I/O is enabled.

BKIN[2:0]	PAD	Description
BKIN[0]	PSOK	If BBPS.PSOKEN=1, BKIN[0] will give the input value of the PSOK pin
BKIN[1]	OUT[0]	If BKOUT.EN[0]=1, BKIN[1] will give the input value of the OUT[0] pin
BKIN[2]	OUT[1]	If BKOUT.EN[1]=1, BKIN[2] will give the input value of the OUT[1] pin

If the Early Warning interrupt is enabled in Window mode, the interrupt is generated at the start of the open window period, i.e. after TO_{WDTW}. The Window mode operation is illustrated in figure Window-Mode Operation.

Figure 24-3. Window-Mode Operation



24.6.3. DMA Operation

Not applicable.

24.6.4. Interrupts

The WDT has the following interrupt source:

- Early Warning (EW): Indicates that the counter is approaching the time-out condition.
  - This interrupt is an asynchronous wake-up source.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs.

Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the WDT is reset. See the INTFLAG register description for details on how to clear interrupt flags. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the INTFLAG register to determine which interrupt condition is present.

Note: Interrupts must be globally enabled for interrupt requests to be generated.

Related Links

Nested Vector Interrupt Controller on page 52

Overview on page 52

PM – Power Manager on page 192

Sleep Mode Controller on page 198

24.6.5. Events

Not applicable.

Value	Description
0	Read/write synchronization for COUNT register is complete.
1	Read/write synchronization for COUNT register is ongoing.

Bit 2 – FREQCORR: Frequency Correction Synchronization Busy Status

Value	Description
0	Read/write synchronization for FREQCORR register is complete.
1	Read/write synchronization for FREQCORR register is ongoing.

Bit 1 – ENABLE: Enable Synchronization Busy Status

Value	Description
0	Read/write synchronization for CTRLA.ENABLE bit is complete.
1	Read/write synchronization for CTRLA.ENABLE bit is ongoing.

Bit 0 – SWRST: Software Reset Synchronization Busy Status

Value	Description
0	Read/write synchronization for CTRLA.SWRST bit is complete.
1	Read/write synchronization for CTRLA.SWRST bit is ongoing.

26.8.5. CRC Status

Name: CRCSTATUS
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
							CRCZERO	CRCBUSY
Access							R	R/W
Reset							0	0

Bit 1 – CRCZERO: CRC Zero
This bit is cleared when a new CRC source is selected.

This bit is set when the CRC generation is complete and the CRC Checksum is zero.

When running CRC-32 and appending the checksum at the end of the packet (as little endian), the final checksum should be 0x2144df1c, and not zero. However, if the checksum is complemented before it is appended (as little endian) to the data, the final result in the checksum register will be zero. See the description of CRCCHKSUM to read out different versions of the checksum.

Bit 0 – CRCBUSY: CRC Module Busy
This flag is cleared by writing a one to it when used with I/O interface. When used with a DMA channel, the bit is set when the corresponding DMA channel is enabled, and cleared when the corresponding DMA channel is disabled. This register bit cannot be cleared by the application when the CRC is used with a DMA channel.

This bit is set when a source configuration is selected and as long as the source is using the CRC module.

26.8.17. Channel ID

Name: CHID
Offset: 0x3F
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					ID[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – ID[3:0]: Channel ID
These bits define the channel number that will be affected by the channel registers (CH*). Before reading or writing a channel register, the channel ID bit group must be written first.

26.8.20. Channel Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Channel Interrupt Enable Set (CHINTENSET) register.
This register affects the DMA channel that is selected in the Channel ID register (CHID.ID).

Name: CHINTENCLR
Offset: 0x4C
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						SUSP	TCMPL	TERR
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SUSP: Channel Suspend Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Channel Suspend Interrupt Enable bit, which disables the Channel Suspend interrupt.

Value	Description
0	The Channel Suspend interrupt is disabled.
1	The Channel Suspend interrupt is enabled.

Bit 1 – TCMPL: Channel Transfer Complete Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Channel Transfer Complete Interrupt Enable bit, which disables the Channel Transfer Complete interrupt.

Value	Description
0	The Channel Transfer Complete interrupt is disabled. When block action is set to none, the TCMPL flag will not be set when a block transfer is completed.
1	The Channel Transfer Complete interrupt is enabled.

Bit 0 – TERR: Channel Transfer Error Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Channel Transfer Error Interrupt Enable bit, which disables the Channel Transfer Error interrupt.

Value	Description
0	The Channel Transfer Error interrupt is disabled.
1	The Channel Transfer Error interrupt is enabled.

34.8.4. Interrupt Enable Set

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Name: INTENSET
Offset: 0x16
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	ERROR					DRDY	AMATCH	PREC
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0

Bit 7 – ERROR: Error Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 2 – DRDY: Data Ready Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Data Ready bit, which enables the Data Ready interrupt.

Value	Description
0	The Data Ready interrupt is disabled.
1	The Data Ready interrupt is enabled.

Bit 1 – AMATCH: Address Match Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Address Match Interrupt Enable bit, which enables the Address Match interrupt.

Value	Description
0	The Address Match interrupt is disabled.
1	The Address Match interrupt is enabled.

Bit 0 – PREC: Stop Received Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Stop Received Interrupt Enable bit, which enables the Stop Received interrupt.

34.8.9. Data

Name: DATA
Offset: 0x28
Reset: 0x0000
Property: Write-Synchronized, Read-Synchronized

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – DATA[7:0]: Data
The slave data register I/O location (DATA.DATA) provides access to the master transmit and receive data buffers. Reading valid data or writing data to be transmitted can be successfully done only when SCL is held low by the slave (STATUS.CLKHOLD is set). An exception occurs when reading the last data byte after the stop condition has been received.

Accessing DATA.DATA auto-triggers I^2C bus operations. The operation performed depends on the state of CTRLB.ACKACT, CTRLB.SMEN and the type of access (read/write).

Writing or reading DATA.DATA when not in smart mode does not require synchronization.

Offset	Name	Bit Pos.								
0x28	INTENSET	7:0					ERR	CNT	TRG	OVF
0x29		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS			
0x2A		23:16					MC3	MC2	MC1	MC0
0x2B	Reserved									
0x2C	INTFLAG	7:0					ERR	CNT	TRG	OVF
0x2D		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS			
0x2E		23:16					MC3	MC2	MC1	MC0
0x2F	Reserved									
0x30	STATUS	7:0	PERBUFV		PATTBUFV		DFS		IDX	STOP
0x31		15:8	FAULT1	FAULT0	FAULTB	FAULTA	FAULT1IN	FAULT0IN	FAULTBIN	FAULTAIN
0x32		23:16					CCBUFV3	CCBUFV2	CCBUFV1	CCBUFV0
0x33		31:24					CMP3	CMP2	CMP1	CMP0
0x34	COUNT	7:0	COUNT[7:0]							
0x35		15:8	COUNT[15:8]							
0x36		23:16	COUNT[23:16]							
0x37		31:24	COUNT[31:24]							
0x38	PATT	7:0	PGE7	PGE6	PGE5	PGE4	PGE3	PGE2	PGE1	PGE0
0x39		15:8	PGV7	PGV6	PGV5	PGV4	PGV3	PGV2	PGV1	PGV0
0x3A ... 0x3B	Reserved									
0x3C	WAVE	7:0	CIPEREN		RAMP[1:0]			WAVEGEN[2:0]		
0x3D		15:8					CICCEN3	CICCEN2	CICCEN1	CICCEN0
0x3E		23:16					POL3	POL2	POL1	POL0
0x3F		31:24					SWAP3	SWAP2	SWAP1	SWAP0
0x40	PER	7:0	PER[1:0]		DITHER[5:0]					
0x41		15:8	PER[9:2]							
0x42		23:16	PER[17:10]							
0x43		31:24	PER[25:18]							
0x44	CC0	7:0	CC[1:0]		DITHER[5:0]					
0x45		15:8	CC[9:2]							
0x46		23:16	CC[17:10]							
0x47		31:24	CC[25:18]							
0x48	CC1	7:0	CC[1:0]		DITHER[5:0]					
0x49		15:8	CC[9:2]							
0x4A		23:16	CC[17:10]							
0x4B		31:24	CC[25:18]							
0x4C	CC2	7:0	CC[1:0]		DITHER[5:0]					
0x4D		15:8	CC[9:2]							
0x4E		23:16	CC[17:10]							
0x4F		31:24	CC[25:18]							
0x50	CC3	7:0	CC[1:0]		DITHER[5:0]					
0x51		15:8	CC[9:2]							
0x52		23:16	CC[17:10]							
0x53		31:24	CC[25:18]							

36.8.6. Waveform Extension Control

Name: WEXCTRL
Offset: 0x14
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
	DTHS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DTLS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
					DTIEN3	DTIEN2	DTIEN1	DTIEN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
							OTMX[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 31:24 – DTHS[7:0]: Dead-Time High Side Outputs Value
This register holds the number of GCLK_TCC clock cycles for the dead-time high side.

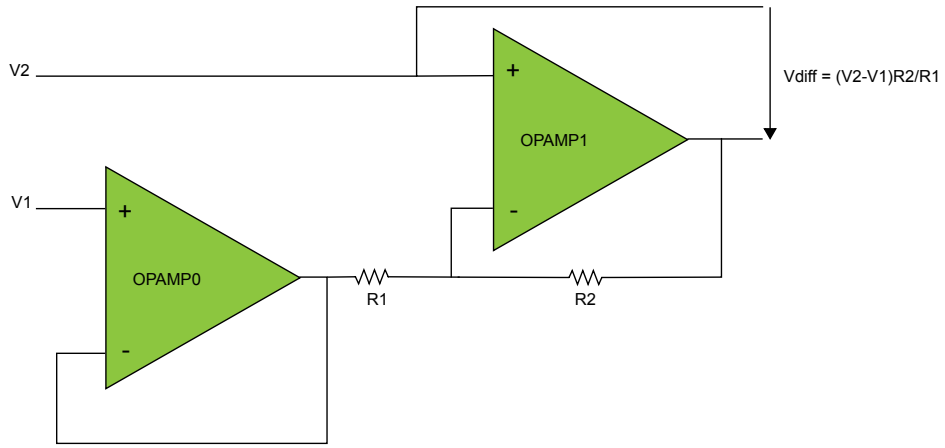
Bits 23:16 – DTLS[7:0]: Dead-time Low Side Outputs Value
This register holds the number of GCLK_TCC clock cycles for the dead-time low side.

Bits 1:0 – OTMX[1:0]: Output Matrix
These bits define the matrix routing of the TCC waveform generation outputs to the port pins, according to Table 36-4.

Bits 11,10,9,8 – DTIENx : Dead-time Insertion Generator x Enable
Setting any of these bits enables the dead-time insertion generator for the corresponding output matrix. This will override the output matrix [x] and [x+WO_NUM/2], with the low side and high side waveform respectively.

Value	Description
0	No dead-time insertion override.
1	Dead time insertion override on signal outputs[x] and [x+WO_NUM/2], from matrix outputs[x] signal.

Figure 41-7. OPAMP0 OPAMP1 Differential Amplifier



41.6.10.7. Instrumentation Amplifier

In this mode, OPAMP0 and OPAMP1 are configured as voltage followers. The OPAMPCTRLx register can be configured as follows:

Table 41-9. Instrumentation Amplifier Configuration

	MUXPOS	MUXNEG	RES1MUX	POTMUX	RES2VCC	RES2OUT	RES1EN	ANAOUT
OPAMP0	000	010	11	010	0	1	1	0
OPAMP1	000	010	11	000	0	0	0	0
OPAMP2	110	001	10	010	0	1	1	0

The resistor ladders associated with OPAMP0 and OPAMP2 must be configured as follows in order to select the appropriate gain:

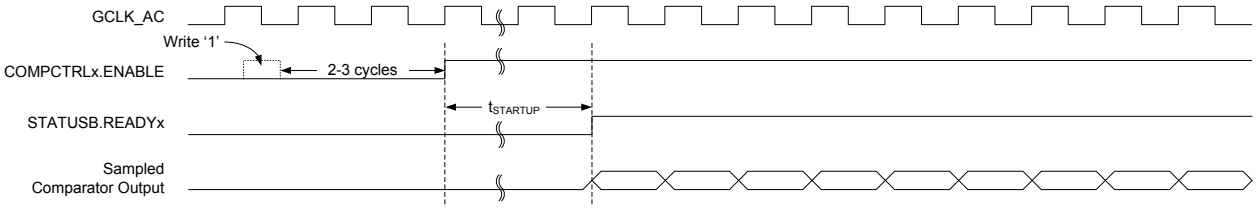
Table 41-10. Instrumentation Amplifier Gain Selection

OPAMPCTRL0.POTMUX	OPAMPCTRL2.POTMUX	GAIN
0x7	Reserved	Reserved
0x6	0x0	1/7
0x5	Reserved	Reserved
0x4	0x1	1/3
0x3	Reserved	Reserved
0x2	0x2	1
0x1	0x4	3
0x0	0x6	7

Note: Either the DAC or GND must be the reference, selected by the OPAMPCTRL0.RES1MUX bits. Refer to OPAMPCTRL0, OPAMPCTRL1 and OPAMPCTRL2 for details.

otherwise GCLK_AC is disabled until the next edge detection. Filtering is not possible with this configuration.

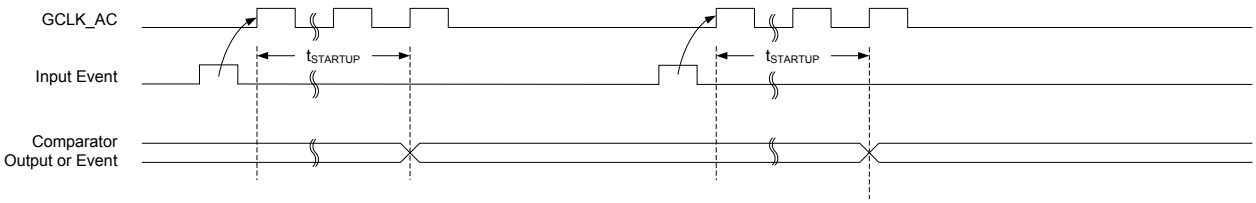
Figure 43-9. Continuous Mode SleepWalking



43.6.14.2. Single-Shot Measurement during Sleep

For low-power operation, event-triggered measurements can be performed during sleep modes. When the event occurs, the Power Manager will start GCLK_AC. The comparator is enabled, and after the start-up time has passed, a comparison is done, with filtering if desired, and the appropriate peripheral events and interrupts are also generated, as shown in Figure 43-10. The comparator and GCLK_AC are then disabled again automatically, unless configured to wake the system from sleep. Filtering is allowed with this configuration.

Figure 43-10. Single-Shot SleepWalking



43.6.15. Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in control register (CTRLA.SWRST)
- Enable bit in control register (CTRLA.ENABLE)
- Enable bit in Comparator Control register (COMPCTRLn.ENABLE)

The following registers are synchronized when written:

- Window Control register (WINCTRL)

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

Related Links

Register Synchronization on page 129

Conditions for V_{DD}: 3V<V_{DD}≤3.6V.

If V_{pin} is lower than GND-0.6V, a current limiting resistor is required. The negative DC injection current limiting resistor *R* is calculated as $R = |(GND-0.6V - V_{pin})/I_{inj1}|$.

If V_{pin} is greater than V_{DD}+0.6V, a current limiting resistor is required. The positive DC injection current limiting resistor *R* is calculated as $R = (V_{pin}-(V_{DD}+0.6))/I_{inj1}$.

4. Conditions for V_{pin}: V_{pin} < GND-0.6V or V_{pin}≤3.6V.

   Conditions for V_{DD}: V_{DD}≤3V.

   If V_{pin} is lower than GND-0.6V, a current limiting resistor is required. The negative DC injection current limiting resistor *R* is calculated as $R = |(GND-0.6V - V_{pin})/I_{inj2}|$.

   If V_{pin} is greater than V_{DD}+0.6V, a current limiting resistor is required. The positive DC injection current limiting resistor *R* is calculated as $R = (V_{pin}-(V_{DD}+0.6))/I_{inj2}$.

46.10. Analog Characteristics

46.10.1. Voltage Regulator Characteristics

46.10.1.1. Buck Converter

Table 46-14. Buck Converter Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_{EFF}	Power Efficiency(2)	I_{OUT} = 5mA	-	86	-	%
		I_{OUT} = 50mA	-	85	-	%
VREGSCAL	Voltage scaling(1)	min step size for PLx to PLy transition	-	5	-	mV
		Voltage Scaling Period	-	1	-	µs

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.
2. These values are based on characterization.

Table 46-15. External Components Requirements in Switching Mode(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input regulator capacitor		-	4.7	-	µF
		Ceramic dielectric	-	100	-	nF
C_{OUT}	Output regulator capacitor		-	1	-	µF
		Ceramic dielectric	-	100	-	nF
L_{EXT}	External inductance	Murata LQH3NPN100MJ0	-	10	-	µH
R_{SERIE_LEXT}	Serial resistance of Lext	-	-	-	0.7	Ω
I_{SAT_LEXT}	Saturation current	-	275	-	-	mA

Note:

Figure 47-2. Power Consumption over Temperature in Standby Sleep Mode with RTC

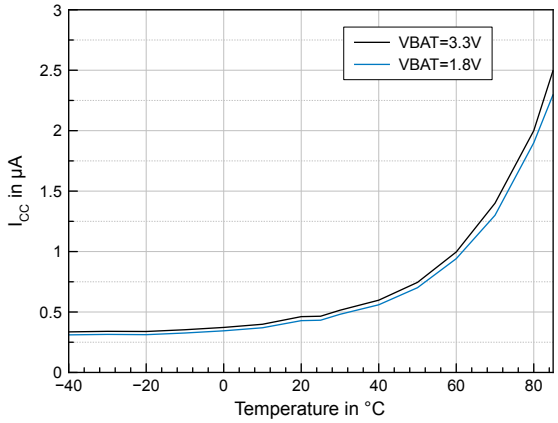


Figure 49-1. Power Supply Connection for Switching/Linear Mode

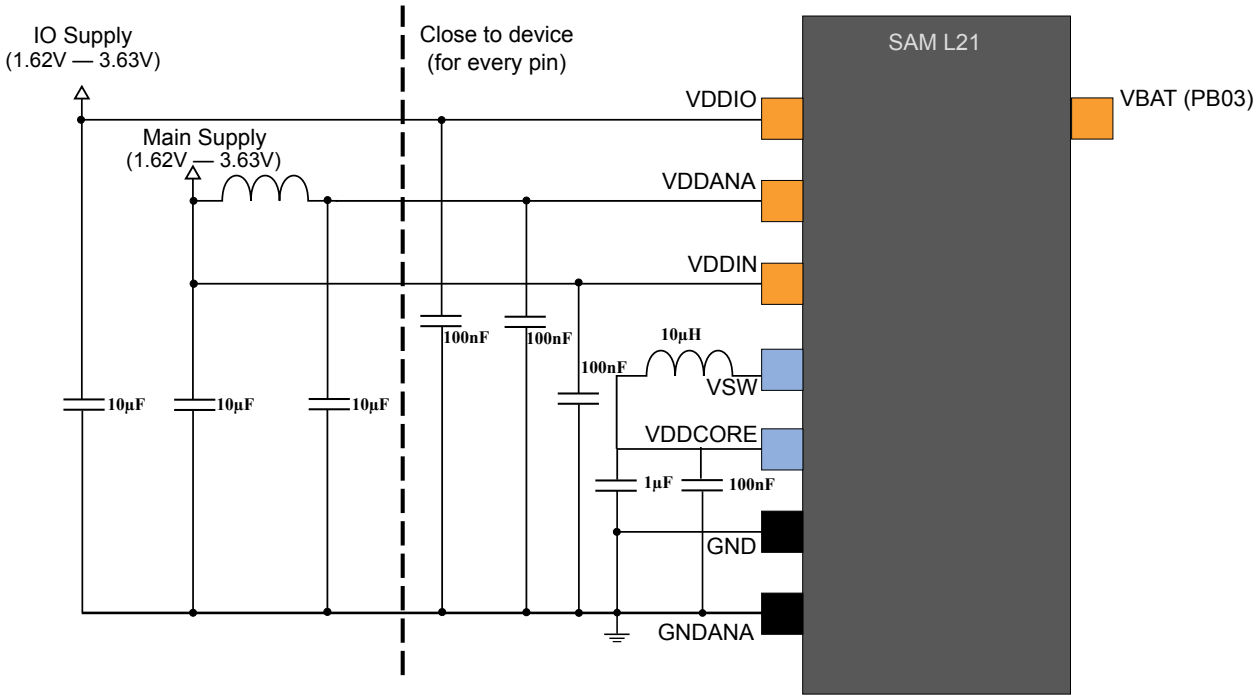


Figure 49-2. Power Supply Connection for Linear Mode Only